

INTERNAL BLOCK DIAGRAM

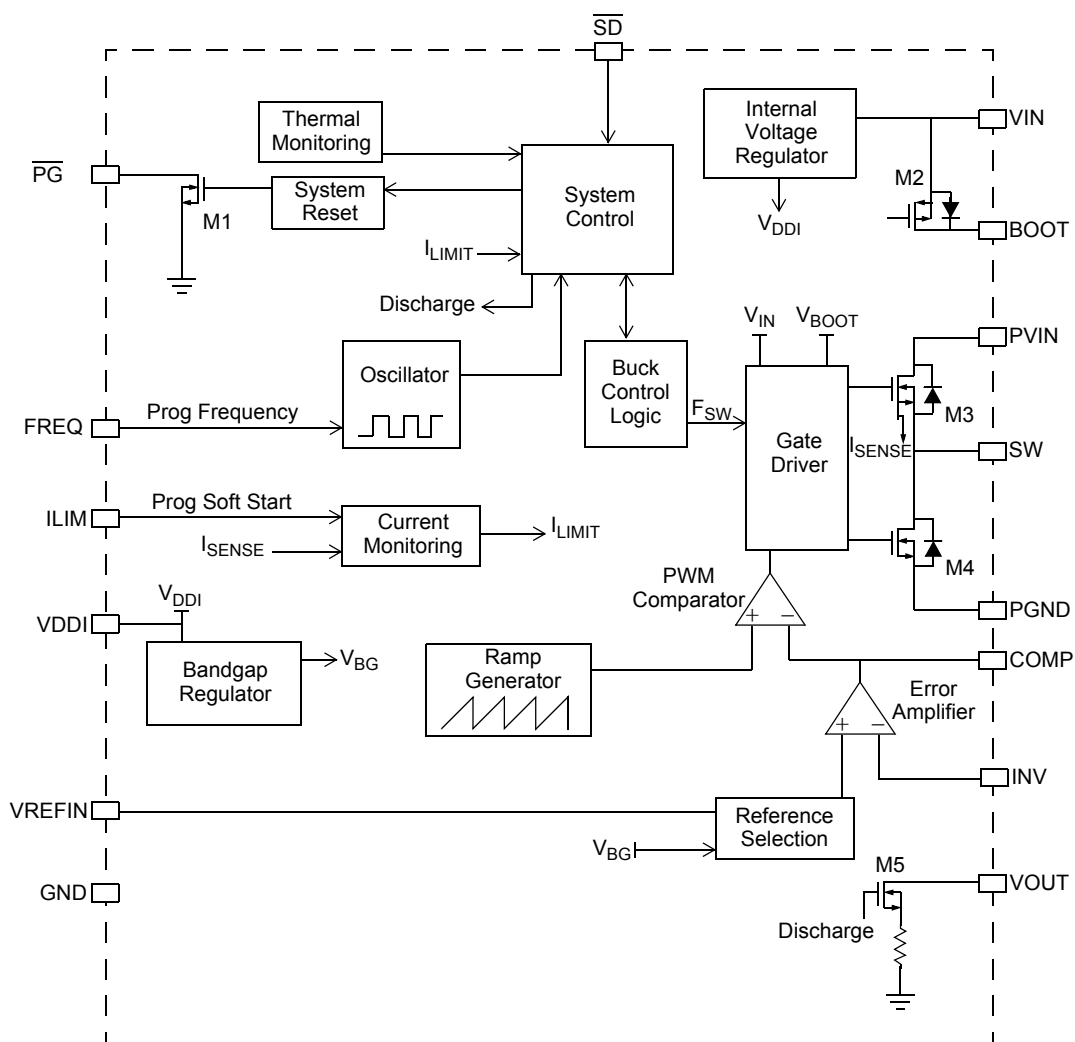


Figure 2. 34713 Simplified Internal Block Diagram

PIN CONNECTIONS

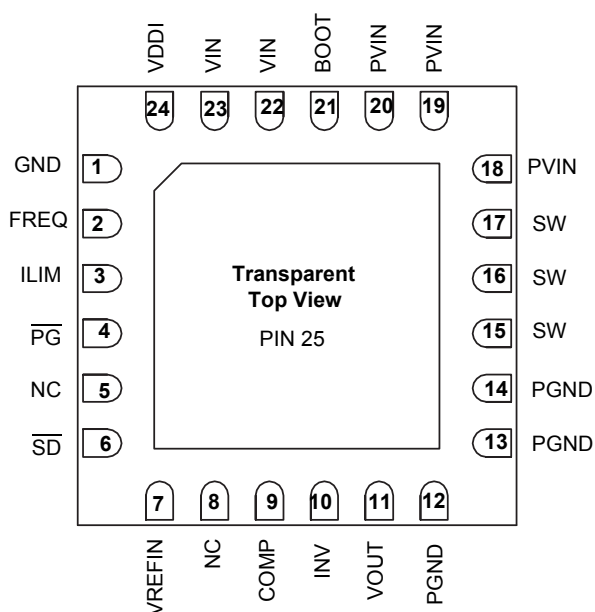


Figure 3. 34713 Pin Connections

Table 1. 34713 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 10](#).

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	GND	Ground	Signal Ground	Analog signal ground of IC
2	FREQ	Passive	Frequency Adjustment	Buck converter switching frequency adjustment pin
3	ILIM	Input	Soft Start	Soft Start adjustment
4	PG	Output	Power Good	Active-low (open drain) power-good status reporting pin
5, 8	NC	None	No Connect	No internal connections to these pins. Recommend attaching a 0.1 μ F capacitor from pin 8 to GND.
6	SD	Input	Shutdown	Shutdown mode input control pin
7	VREFIN	Input	Voltage Tracking Reference Input	Voltage Tracking Reference voltage input
9	COMP	Passive	Compensation	Buck converter external compensation network pin
10	INV	Input	Error Amplifier Inverting Input	Buck converter error amplifier inverting input pin
11	VOUT	Output	Output Voltage Discharge FET	Discharge FET drain connection (connect to buck converter output capacitors)
12,13,14	PGND	Ground	Power Ground	Ground return for buck converter and discharge FET
15,16,17	SW	Output	Switching Node	Buck converter power switching node
18,19,20	PVIN	Supply	Power-Circuit Supply Input	Buck converter main supply voltage input
21	BOOT	Passive	Bootstrap	Bootstrap switching node (connect to bootstrap capacitor)
22,23	VIN	Supply	Logic-Circuit Supply Input	Logic circuits supply voltage input
24	VDDI	Passive	Internal Voltage Regulator	Internal Vdd Regulator (connect filter capacitor to this pin)

34713

Table 1. 34713 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on [page 10](#).

Pin Number	Pin Name	Pin Function	Formal Name	Definition
25	GND	Ground	Thermal Pad	Thermal pad for heat transfer. Connect the thermal pad to the analog ground and the ground plane for heat sinking.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Input Supply Voltage (VIN) Pin	V _{IN}	-0.3 to 7.0	V
High Side MOSFET Drain Voltage (PVIN) Pin	PV _{IN}	-0.3 to 7.0	V
Switching Node (SW) Pin	V _{SW}	-0.3 to 7.0	V
BOOT Pin (Referenced to SW Pin)	V _{BOOT} - V _{SW}	-0.3 to 7.0	V
PG, VOUT,and SD Pins	-	-0.3 to 7.0	V
VDDI, FREQ, ILIM, INV, COMP, and VREFIN Pins	-	-0.3 to 3.0	V
Continuous Output Current ⁽¹⁾	I _{OUT}	+5.0	A
ESD Voltage ⁽²⁾			
Human Body Model	V _{ESD1}	±2000	V
Machine Model (MM)	V _{ESD2}	±200	
Charge Device Model	V _{ESD3}	±750	
THERMAL RATINGS			
Operating Ambient Temperature ⁽³⁾	T _A	-40 to 85	°C
Storage Temperature	T _{STG}	-65 to +150	°C
Peak Package Reflow Temperature During Reflow ^{(4), (5)}	T _{PPRT}	Note 5	°C
Maximum Junction Temperature	T _{J(MAX)}	+150	°C
Power Dissipation (T _A = 85°C) ⁽⁶⁾	P _D	2.9	W

Notes

- Continuous output current capability so long as T_J is $\leq T_{J(MAX)}$.
- ESD testing is performed in accordance with the Human Body Model (HBM) ($C_{ZAP} = 100$ pF, $R_{ZAP} = 1500$ Ω), the Machine Model (MM) ($C_{ZAP} = 200$ pF, $R_{ZAP} = 0$ Ω), and the Charge Device Model (CDM), Robotic ($C_{ZAP} = 4.0$ pF).
- The limiting factor is junction temperature, taking into account power dissipation, thermal resistance, and heatsinking.
- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
- Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx)], and review parametrics.
- Maximum power dissipation at indicated ambient temperature

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
THERMAL RESISTANCE⁽⁷⁾			
Thermal Resistance, Junction to Ambient, Single-layer Board (1s) ⁽⁸⁾	$R_{\theta JA}$	139	°C/W
Thermal Resistance, Junction to Ambient, Four-layer Board (2s2p) ⁽⁹⁾	$R_{\theta JMA}$	43	°C/W
Thermal Resistance, Junction to Board ⁽¹⁰⁾	$R_{\theta JB}$	22	°C/W

Notes

7. The PVIN, SW, and PGND pins comprise the main heat conduction paths.
8. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
9. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal. There are no thermal vias connecting the package to the two planes in the board.
10. Thermal resistance between the device and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions $3.0\text{ V} \leq V_{\text{IN}} \leq 6.0\text{ V}$, $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 85^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{\text{A}} = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
IC INPUT SUPPLY VOLTAGE (VIN)					
Input Supply Voltage Operating Range	V_{IN}	3.0	-	6.0	V
Input DC Supply Current ⁽¹¹⁾ Normal Mode: $\overline{\text{SD}} = 1$, Unloaded Outputs	I_{IN}	-	-	25	mA
Input DC Supply Current ⁽¹¹⁾ Shutdown Mode, $\overline{\text{SD}} = 0$	I_{INOFF}	-	-	100	μA
INTERNAL SUPPLY VOLTAGE OUTPUT (VDDI)					
Internal Supply Voltage Range	V_{DDI}	2.35	2.5	2.65	V
BUCK CONVERTER (PVIN, SW, PGND, BOOT, INV, COMP, ILIM)					
High Side MOSFET Drain Voltage Range	P_{VIN}	2.5	-	6.0	V
Output Voltage Adjustment Range ^{(12),(13)}	V_{OUT}	0.7	-	3.6	V
Output Voltage Accuracy ^{(12),(14)}	-	-1.0	-	1.0	%
Line Regulation ⁽¹²⁾ Normal Operation, $V_{\text{IN}} = 3.0$ to 6.0 V , $I_{\text{OUT}} = +5.0\text{ A}$	REG_{LN}	-1.0	-	1.0	%
Load Regulation ⁽¹²⁾ Normal Operation, $I_{\text{OUT}} = 0.0$ to 5.0 A	REG_{LD}	-1.0	-	1.0	%
Error Amplifier Common Mode Voltage Range ^{(12),(13)}	V_{REF}	0.0	-	1.35	V
Output Under-voltage Threshold	V_{UVR}	-8.0	-	-1.5	%
Output Over-voltage Threshold	V_{OVR}	1.5	-	8.0	%
Continuous Output Current	I_{OUT}	-	-	5.0	A
Over-current Limit	I_{LIM}	-	6.5	-	A
Soft start Adjusting reference Voltage Range	V_{ILIM}	1.25	-	V_{DDI}	V
Short-circuit Current Limit	I_{SHORT}	-	8.5	-	A
High Side N-CH Power MOSFET (M3) $R_{\text{DS(ON)}}$ ⁽¹²⁾ $I_{\text{OUT}} = 1.0\text{ A}$, $V_{\text{BOOT}} - V_{\text{SW}} = 3.3\text{ V}$	$R_{\text{DS(ON)HS}}$	10	-	50	$\text{m}\Omega$
Low Side N-CH Power MOSFET (M4) $R_{\text{DS(ON)}}$ ⁽¹²⁾ $I_{\text{OUT}} = 1.0\text{ A}$, $V_{\text{IN}} = 3.3\text{ V}$	$R_{\text{DS(ON)LS}}$	10	-	50	$\text{m}\Omega$

Notes

11. Section "MODES OF OPERATION", page 13 has a detailed description of the different operating modes of the 34713
12. Design information only, this parameter is not production tested.
13. The $\pm 1\%$ accuracy is only guaranteed for V_{EFOUT} greater then or equal 0.7 V at room temperature.
14. Overall output accuracy is directly affected by the accuracy of the external feedback network, 1% feedback resistors are recommended

Table 3. Static Electrical Characteristics

Characteristics noted under conditions $3.0\text{ V} \leq V_{\text{IN}} \leq 6.0\text{ V}$, $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 85^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{\text{A}} = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
M2 $R_{\text{DS(ON)}}$ $V_{\text{IN}} = 3.3\text{ V}$, M2 is on	$R_{\text{DS(ON)M2}}$	1.5	-	4.0	Ω
SW Leakage Current (Standby and Shutdown modes)	I_{SW}	-10	-	10	μA
PVIN Pin Leakage Current Shutdown Mode	I_{PVIN}	-10	-	10	μA
INV Pin Leakage Current	I_{INV}	-1.0	-	1.0	μA
Error Amplifier DC Gain ⁽¹⁵⁾	A_{EA}	-	150	-	dB
Error Amplifier Unit Gain Bandwidth ⁽¹⁵⁾	$U_{\text{GBW}_{\text{EA}}}$	-	3.0	-	MHz
Error Amplifier Slew Rate ⁽¹⁵⁾	$S_{\text{R}_{\text{EA}}}$	-	7.0	-	$\text{V}/\mu\text{s}$
Error Amplifier Input Offset ⁽¹⁵⁾	$\text{OFFSET}_{\text{EA}}$	-3.0	0	3.0	mV
Thermal Shutdown Threshold ⁽¹⁵⁾	T_{SDFET}	-	170	-	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis ⁽¹⁵⁾	T_{SDHYFET}	-	25	-	$^{\circ}\text{C}$

OSCILLATOR (FREQ)

Oscillator Frequency Adjusting Reference Voltage Range	V_{FREQ}	0.0	-	V_{DDI}	V
--	-------------------	-----	---	------------------	---

TRACKING (VREFIN, VOUT)

VREFIN External Reference Voltage Range ⁽¹⁵⁾	V_{REFIN}	0.0	-	1.35	V
VOUT Total Discharge Resistance ⁽¹⁵⁾	$R_{\text{TDR(M5)}}$	-	50	-	Ω

CONTROL AND SUPERVISORY ($\overline{\text{SD}}$, $\overline{\text{PG}}$)

$\overline{\text{SD}}$ High Level Input Voltage	V_{SDHI}	2.0	-	-	V
$\overline{\text{SD}}$ Low Level Input Voltage	V_{SDLO}	-	-	0.4	V
$\overline{\text{SD}}$ Pin Internal Pull-up Resistor ⁽¹⁵⁾	R_{SDUP}	1.0	-	2.0	$\text{M}\Omega$
$\overline{\text{PG}}$ Low Level Output Voltage $I_{\text{PG}} = 3.0\text{ mA}$	V_{PGLO}	-	-	0.4	V
$\overline{\text{PG}}$ Pin Leakage Current M1 is off, Pulled up to VIN	I_{PGLKG}	-1.0	-	1.0	μA

Notes

15. Design information only, this parameter is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions $3.0\text{ V} \leq V_{\text{IN}} \leq 6.0\text{ V}$, $-40^{\circ}\text{C} \leq T_{\text{A}} \leq 85^{\circ}\text{C}$, $\text{GND} = 0\text{ V}$, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_{\text{A}} = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
BUCK CONVERTER (PVIN, SW, PGND, BOOT)					
Switching Node (SW) Rise Time ⁽¹⁶⁾ ($P_{\text{VIN}} = 3.3\text{ V}$, $I_{\text{OUT}} = 5.0\text{ A}$)	t_{RISE}	-	14	-	ns
Switching Node (SW) Fall Time ⁽¹⁶⁾ ($P_{\text{VIN}} = 3.3\text{ V}$, $I_{\text{OUT}} = 5.0\text{ A}$)	t_{FALL}	-	20	-	ns
Minimum OFF Time	t_{OFFMIN}	-	150	-	ns
Minimum ON Time	t_{ONMIN}	-	0 ⁽¹⁷⁾	-	ns
Soft Start Duration (Normal Mode) ILIM= 1.25 - 1.49 V 1.50 - 1.81 V 1.82 - 2.13 V 2.14 - 2.50 V	t_{SS}	- - - -	3.2 1.6 0.8 0.4	- - - -	ms
Over-current Limit Timer	t_{LIM}	-	10	-	ms
Over-current Limit Retry Time-out Period	t_{TIMEOUT}	80	-	120	ms
Output Under-voltage/Over-voltage Filter Delay Timer	t_{FILTER}	5.0	-	25	μs
OSCILLATOR (FREQ)					
Oscillator Default Switching Frequency Oscillator Frequency tolerance is $\pm 10\%$ (FREQ = GND)	f_{SW}	-	1.0	-	MHz
Oscillator Switching Frequency Range	f_{SW}	200	-	1000	KHz
CONTROL AND SUPERVISORY ($\overline{\text{SD}}$, $\overline{\text{PG}}$)					
$\overline{\text{PG}}$ Reset Delay	t_{PGRESET}	8.0	-	12	ms
Thermal Shutdown Retry Timeout Period ⁽¹⁶⁾	t_{TIMEOUT}	80	-	120	ms

Notes

16. Design information only, this parameter is not production tested.
17. The regulator has the ability to enter into pulse skip mode when the inductor current ripple reaches the threshold for the LS zero detect, which has a typical value of 500 mA.

FUNCTIONAL DESCRIPTION

INTRODUCTION

Advanced microprocessor-based systems require compact, efficient, and accurate point-of-load (PoL) power supplies. These PoL supply high current and fast transient response capability while maintaining regulation accuracy. Voltage monitoring (power sequencing) and increased operating frequency are also key features for PoL power supplies.

PoL power supplies are non-isolated DC to DC converters that are physically located near their load (on the same printed circuit board) and take their input supply from an intermediate bus. Their close proximity to the load allows for higher efficiency, localized protection, and minimum distribution losses. Their compact design and low component-count also reduces overall system cost.

The 34713 is a PoL single-output power supply that embodies an integrated solution that's both highly cost-effective and reliable. It utilizes a voltage-mode synchronous buck switching converter topology with integrated low $R_{DS(ON)}$ (50 m Ω) N-channel power MOSFETs for high-

efficiency operation. It provides an output voltage with an accuracy of less than $\pm 2.0\%$, capable of supplying up to 5.0 A of continuous current. Its power sequencing/tracking abilities makes it ideal for systems with multiple related supply rails. It has an adjustable switching frequency, thus permitting greater design flexibility and optimization over a wide range of operating conditions, and can operate at up to 1.0 MHz to significantly reduce the external components size and cost. It also features an over-current limit control, and protects against output over-voltage, under-voltage, and over-temperature conditions. It also protects the system from short-circuit events and incorporates a power-good output signal to alert the host MCU should a fault occur.

Operation can be enabled or disabled by controlling the $\overline{SD}$ pin, which offers power sequencing capabilities.

By monolithically integrating the control and supervisory circuitry along with power-FETs, the 34713 offers a complete, compact, cost-effective, and simple solution to satisfy the PoL needs of today's systems.

FUNCTIONAL PIN DESCRIPTION

REFERENCE VOLTAGE INPUT (VREFIN)

The 34713 will track the voltage applied at this pin.

FREQUENCY ADJUSTMENT INPUT (FREQ)

The buck converter switching frequency can be adjusted by connecting this pin to an external resistor divider between VDDI and GND pins. The default switching frequency (FREQ pin connected to ground, GND) is set at 1.0 MHz.

SOFT START ADJUSTMENT INPUT (ILIM)

Soft start timing can be adjusted by applying an external voltage between 1.25 V and V_{DDI} on this pin.

SIGNAL GROUND (GND)

Analog ground of the IC. Internal analog signals are referenced to this pin voltage.

INTERNAL SUPPLY VOLTAGE OUTPUT (VDDI)

This is the output of the internal bias voltage regulator. Connect a 1.0 μ F, 6.0 V low ESR ceramic filter capacitor between this pin and the GND pin. Filtering any spikes on this output is essential to the internal circuitry stable operation.

OUTPUT VOLTAGE DISCHARGE PATH (VOUT)

Output voltage of the Buck Converter is connected to this pin. It only serves as the output discharge path once the $\overline{SD}$ signal is asserted.

ERROR AMPLIFIER INVERTING INPUT (INV)

Buck converter error amplifier inverting input. Connect the output voltage feedback network to this pin.

COMPENSATION INPUT (COMP)

Buck converter external compensation network connects to this pin. Use a type III compensation network.

INPUT SUPPLY VOLTAGE (VIN)

IC power supply input voltage. Input filtering is required for the device to operate properly.

POWER GROUND (PGND)

Buck converter and discharge MOSFET power ground. It is the source of the buck converter low side power MOSFET.

SWITCHING NODE (SW)

Buck converter switching node. This pin is connected to the output inductor.

POWER INPUT VOLTAGE (PVIN)

Buck converter power input voltage. This is the drain of the buck converter high side power MOSFET.

BOOTSTRAP INPUT (BOOT)

Bootstrap capacitor input pin. Connect a capacitor (as discussed on page 18) between this pin and the SW pin to

enhance the gate of the high side Power MOSFET during switching.

SHUTDOWN INPUT ($\overline{SD}$)

If this pin is tied to the GND pin, the device will be in Shutdown mode. If left unconnected or tied to the VIN pin, the device will be in Normal mode. The pin has an internal pull-up of 1.5 M Ω .

POWER GOOD OUTPUT SIGNAL ($\overline{PG}$)

This is an active low open drain output that is used to report the status of the device to a host. This output activates after a successful power up sequence and stays active as long as the device is in normal operation and is not experiencing any faults. This output activates after a 10 ms delay and must be pulled up by an external resistor to a supply voltage (e.g., V_{IN}).

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

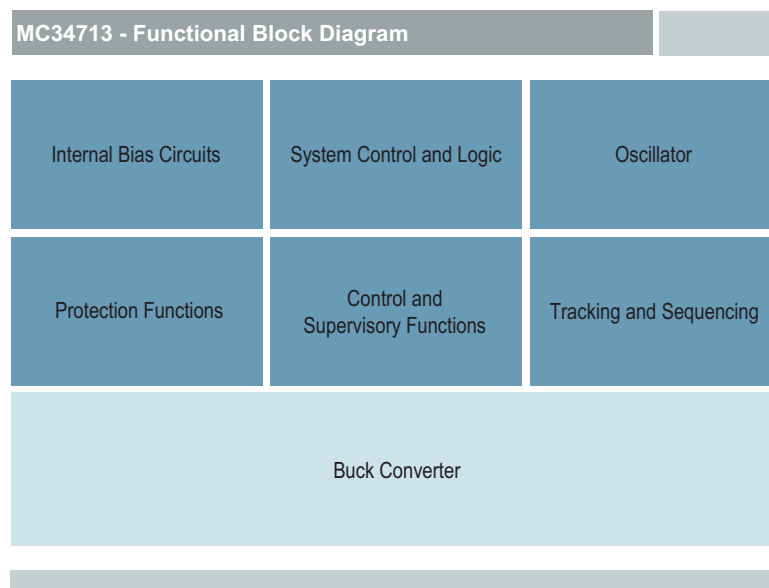


Figure 4. 34713 Block Diagram

INTERNAL BIAS CIRCUITS

This block contains all circuits that provide the necessary supply voltages and bias currents for the internal circuitry. It consists of:

- Internal voltage supply regulator: This regulator supplies the V_{DDI} voltage that is used to drive the digital/analog internal circuits. It is equipped with a Power-On-Reset (POR) circuit that watches for the right regulation levels. External filtering is needed on the VDDI pin. This block will turn off during the shutdown mode.
- Internal bandgap reference voltage: This supplies the reference voltage to some of the internal circuitry.
- Bias circuit: This block generates the bias currents necessary to run all of the blocks in the IC.

SYSTEM CONTROL AND LOGIC

This block is the brain of the IC where the device processes data and reacts to it. Based on the status of the $\overline{SD}$ pin, the system control reacts accordingly and orders the device into the right status. It also takes inputs from all of the monitoring/protection circuits and initiates power up or power

down commands. It communicates with the buck converter to manage the switching operation and protects it against any faults.

OSCILLATOR

This block generates the clock cycles necessary to run the IC digital blocks. It also generates the buck converter switching frequency. The switching frequency has a default value of 1.0 MHz and can be programmed by connecting a resistor divider to the FREQ pin, between VDDI and GND pins (See [Figure 1](#)).

PROTECTION FUNCTIONS

This block contains the following circuits:

- Over-current limit and short-circuit detection: This block monitors the output of the buck converter for over current conditions and short-circuit events and alerts the system control for further command.
- Thermal limit detection: This block monitors the temperature of the device for overheating events. If the temperature rises above the thermal shutdown

threshold, this block will alert the system control for further commands.

- Output over-voltage and under-voltage monitoring: This block monitors the buck converter output voltage to ensure it is within regulation boundaries. If not, this block alerts the system control for further commands.

CONTROL AND SUPERVISORY FUNCTIONS

This block is used to interface with an outside host. It contains the following circuits:

- Shutdown control input: An outside host can put the 34713 device into shutdown mode by sending a logic “0” to the $\overline{\text{SD}}$ pin.
- Power good output signal $\overline{\text{PG}}$: The 34713 can communicate to an external host that a fault has occurred by releasing the drive on the $\overline{\text{PG}}$ pin high, allowing the signal/pin to be pulled high by the external pull-up resistor.

TRACKING AND SEQUENCING

This block allows the output of the 34713 to track the voltage applied at the VREFIN pin in different tracking configurations. This will be discussed in further details later in this document. For power down during a shutdown mode, the 34713 uses internal discharge MOSFET ([Figure 2](#)) to discharge the output. The discharge MOSFET is only active

during shutdown mode. Using this block along with controlling the $\overline{\text{SD}}$ pin can offer the user power sequencing capabilities by controlling when to turn the 34713 output on or off.

BUCK CONVERTER

This block provides the main function of the 34713: DC to DC conversion from an un-regulated input voltage to a regulated output voltage used by the loads for reliable operation. The buck converter is a high performance, fixed frequency (externally adjustable), synchronous buck PWM voltage-mode control. It drives integrated 50 m Ω N-channel power MOSFETs saving board space and enhancing efficiency. The switching regulator output voltage is adjustable with an accuracy of less than $\pm 2\%$ to meet today's requirements. Its output has the ability to track the voltage applied at the VREFIN pin. The regulator's voltage control loop is compensated using a type III compensation network, with external components to allow for optimizing the loop compensation, for a wide range of operating conditions. A typical bootstrap circuit with an internal PMOS switch is used to provide the voltage necessary to properly enhance the high side MOSFET gate.

The 34713 has the ability to supply up to 5.0 A of continuous current, making it suitable for many high current applications.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

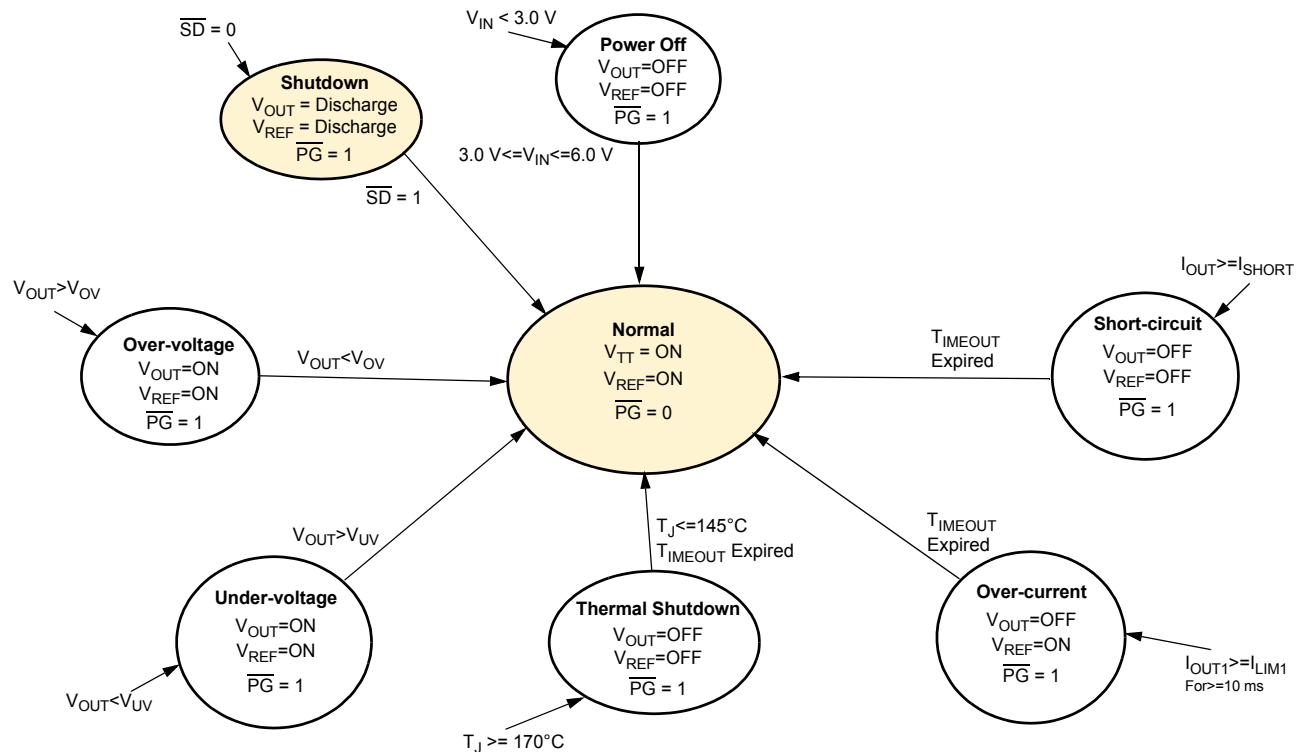


Figure 5. Operation Modes Diagram

MODES OF OPERATION

The 34713 has two primary modes of operation:

Normal Mode

In normal mode, all functions and outputs are fully operational. To be in this mode, the V_{IN} needs to be within its operating range, Shutdown input is high, and no faults are present. This mode consumes the most amount of power.

Shutdown Mode

In this mode, activated by pulling the $\overline{SD}$ pin low, the chip is in a shutdown state and the output is disabled and discharged. In this mode, the 34713 consumes the least amount of power since almost all of the internal blocks are disabled.

START-UP SEQUENCE

When power is first applied, the 34713 checks the status of the $\overline{SD}$ pin. If the device is in a shutdown mode, no block will power up and the output will not attempt to ramp. Once the $\overline{SD}$ pin is released to enable the device, the V_{DDI} internal supply voltage and the bias currents are established and the internal V_{DDI} POR signal is also released. The rest of the

internal blocks will be enabled and the buck converter switching frequency and soft start values are determined by reading the $FREQ$ and $ILIM$ pins respectively. A soft start cycle is then initiated to ramp up the output of the buck converter. The buck converter error amplifier uses the voltage on the $VREFIN$ pin as its reference voltage until $VREFIN$ is equal to 0.7 V, then the error amplifier defaults to the internal 0.7 V reference voltage. This method helps achieve multiple tracking configurations as will be explained later in this document.

Soft start is used to prevent the output voltage from overshooting during startup. At initial startup, the output capacitor is at zero volts; $V_{OUT} = 0$ V. Therefore, the voltage across the inductor will be PV_{IN} during the capacitor charge phase which will create a very sharp di/dt ramp. Allowing the inductor current to rise too high can result in a large difference between the charging current and the actual load current that can result in an undesired voltage spike once the capacitor is fully charged. The soft start is active each time the IC goes out of standby or shutdown mode, power is recycled, or after a fault retry.

After a successful start-up cycle where the device is enabled, no faults have occurred, and the output voltage has reached its regulation point, the 34713 pulls the power good

output signal low after a 10 ms reset delay, to indicate to the host that the device is in normal operation.

PROTECTION AND DIAGNOSTIC FEATURES

The 34713 monitors the application for several fault conditions to protect the load from overstress. The reaction of the IC to these faults ranges from turning off the outputs to just alerting the host that something is wrong. In the following paragraphs, each fault condition is explained:

Output Over-voltage

An over-voltage condition occurs once the output voltage goes higher than the rising over-voltage threshold (V_{OVR}). In this case, the power good output signal is pulled high, alerting the host that a fault is present, but the output will stay active. To avoid erroneous over-voltage conditions, a 20 μ s filter is implemented. The buck converter will use its feedback loop to attempt to correct the fault. Once the output voltage falls below the falling over-voltage threshold (V_{OVF}), the fault is cleared and the power good output signal is pulled low, the device is back in normal operation.

Output Under-voltage

An under-voltage condition occurs once the output voltage falls below the falling under-voltage threshold (V_{UVF}). In this case, the power good output signal is pulled high, alerting the host that a fault is present, but the output will stay active. To avoid erroneous under-voltage conditions, a 20 μ s filter is implemented. The buck converter will use its feedback loop to attempt to correct the fault. Once the output voltage rises above the rising under-voltage threshold (V_{UVR}), the fault is cleared and the power good output signal is pulled low, the device is back in normal operation.

Output Over-current

This block detects over-current in the Power MOSFETs of the buck converter. It is comprised of a sense MOSFET and a comparator. The sense MOSFET acts as a current detecting device by sampling a ratio of the load current. That sample is compared via the comparator with an internal reference to determine if the output is in over-current or not. If the peak current in the output inductor reaches the over current limit (I_{LIM}), the converter will start a cycle-by-cycle

operation to limit the current, and a 10 ms over-current limit timer (t_{LIM}) starts. The converter will stay in this mode of operation until one of the following occurs:

- The current is reduced back to the normal level before t_{LIM} expires, and in this case normal operation is regained.
- t_{LIM} expires without regaining normal operation, at which point the device turns off the output and the power good output signal is pulled high. At the end of a time-out period of 100 ms ($t_{TIMEOUT}$), the device will attempt another soft start cycle.
- The device reaches the thermal shutdown limit (T_{SDFET}) and turns off the output. The power good output signal is pulled high.
- The output current keeps increasing until it reaches the short circuit current limit (I_{SHORT}). See below for more details.

Short-circuit Current Limit

This block uses the same current detection mechanism as the over-current limit detection block. If the load current reaches the I_{SHORT} value, the device reacts by shutting down the output immediately. This is necessary to prevent damage in case of a permanent short-circuit. Then, at the end of a timeout period of 100 ms ($t_{TIMEOUT}$), the device will attempt another soft start cycle.

Thermal Shutdown

Thermal limit detection block monitors the temperature of the device and protects against excessive heating. If the temperature reaches the thermal shutdown threshold (T_{SDFET}), the converter output switches off and the power good output signal indicates a fault by pulling high. The device will stay in this state until the temperature has decreased by the hysteresis value and then After a timeout period ($T_{TIMEOUT}$) of 100 ms, the device will retry automatically and the output will go through a soft start cycle. If successful normal operation is regained, the power good output signal is asserted low to indicate that.

TYPICAL APPLICATIONS

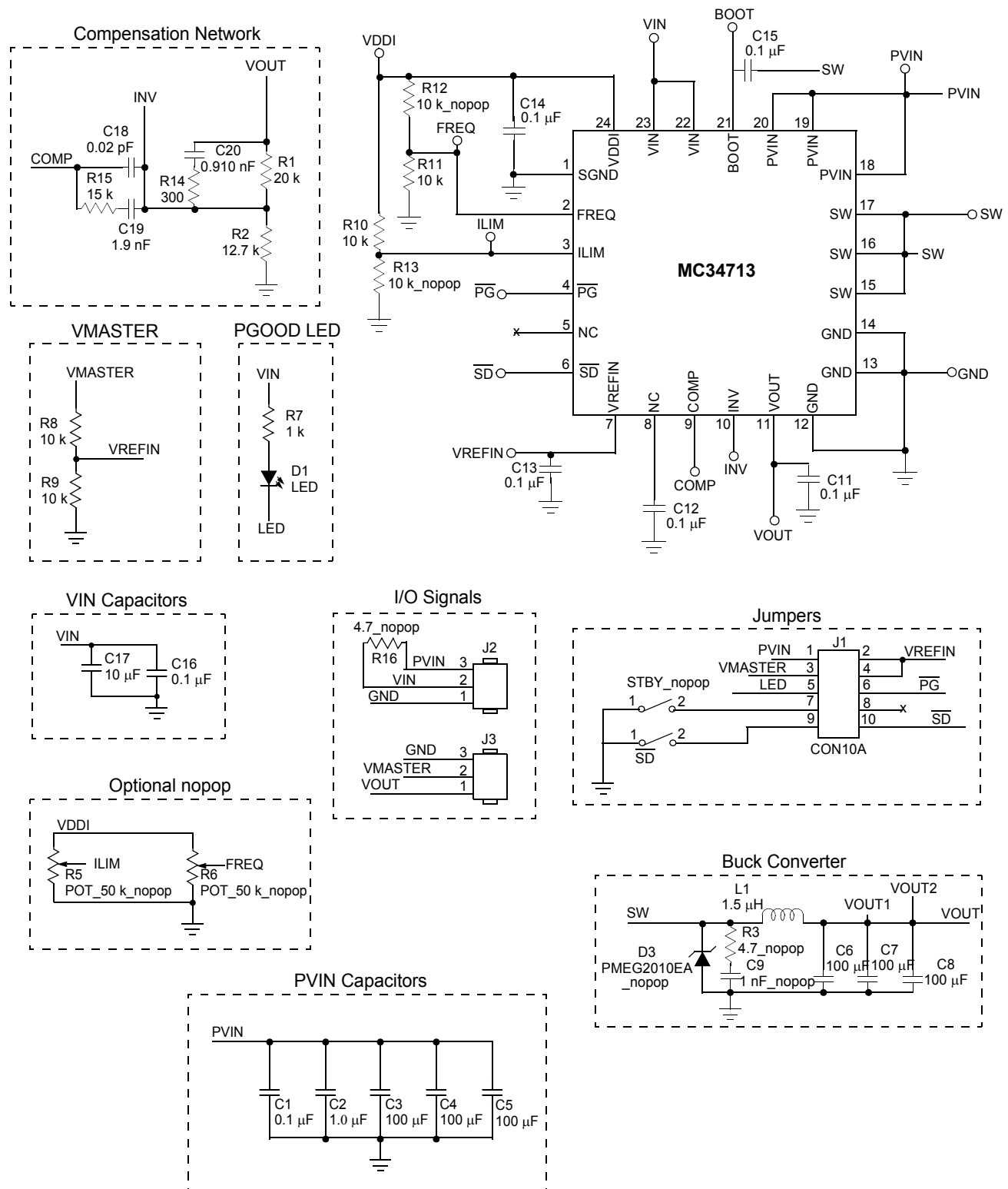


Figure 6. Typical Applications

COMPONENT SELECTION

SWITCHING FREQUENCY SELECTION

The switching frequency defaults to a value of 1.0 MHz when the FREQ pin is grounded, and 200 kHz when the FREQ pin is connected to VDDI. Intermediate switching frequencies can be obtained by connecting an external resistor divider to the FREQ pin. The table below shows the resulting switching frequency versus FREQ pin voltage.

Table 5. Switching Frequency Adjustment

FREQUENCY	VOLTAGE APPLIED TO PIN FREQ
200	2.341 – 2.500
253	2.185 - 2.340
307	2.029 - 2.184
360	1.873 - 2.028
413	1.717 – 1.872
466	1.561 – 1.716
520	1.405 - 1.560
573	1.249 - 1.404
627	1.093 - 1.248
680	0.936 - 1.092
733	0.781 - 0.936
787	0.625 - 0.780
840	0.469 - 0.624
893	0.313 - 0.468
947	0.157 - 0.312
1000	0.000 - 0.156

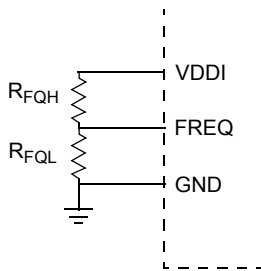


Figure 7. Resistor Divider for Frequency Adjustment

SELECTION OF THE INDUCTOR

Inductor calculation is straight forward, being

$$L = D'_{MAX} * T * \frac{(V_o + I_o * (R_{DS(ON)FET} + R_{INDUCTOR}))}{\Delta I_o}$$

where,

$$D'_{MAX} = 1 - \frac{V_o}{V_{in_max}}$$

Maximum OFF time percentage

T

Switching period.

$R_{DS(ON)FET}$

Drain – to – source resistance of FET

$R_{INDUCTOR}$

Winding resistance of Inductor

$$\Delta I_o = 0.4 * I_o$$

Output current ripple.

OUTPUT FILTER CAPACITOR

For the output capacitor, the following considerations are more important than the actual capacitance value, the physical size, the ESR and the voltage rating:

Transient Response percentage, TR_%

(Use a recommended value of 2 to 4% to assure a good transient response.)

Maximum Transient Voltage, TR_v_dip = $V_o * TR_%$

Maximum current step,

$$\Delta I_o_step = \frac{(V_{in_min} - V_o) * D_max}{F_{sw} * L}$$

Inductor Current rise time,

$$dt_I_rise = \frac{T * I_o}{\Delta I_o_step}$$

where,

D_max = Maximum ON time percentage.

I_o = Rated output current.

V_{in_min} = Minimum input voltage at PV_{IN}

As a result, it is possible to calculate

$$C_o = \frac{I_o * dt_I_rise}{TR_V_dip}$$

In order to find the maximum allowed ESR,

$$ESR_{max} = \frac{\Delta V_o * F_{sw} * L}{V_o(1 - D_{min})}$$

The effects of the ESR is often neglected by the designers and may present a hidden danger to the ultimate supply stability. Poor quality capacitors have widely disparate ESR value, which can make the closed loop response inconsistent.

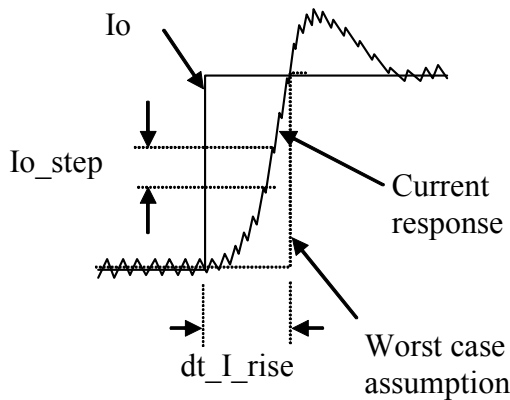


Figure 8. Transient Parameters

TYPE III COMPENSATION NETWORK

Power supplies are desired to offer accurate and tight regulation output voltages. To accomplish this requires a high DC gain. But with high gain comes the possibility of instability. The purpose of adding compensation to the internal error amplifier is to counteract some of the gains and phases contained in the control-to-output transfer function that could jeopardized the stability of the power supply. The Type III compensation network used for 34713 comprises two poles (one integrator and one high frequency pole to cancel the zero generated from the ESR of the output capacitor) and two zeros to cancel the two poles generated from the LC filter as shown in [Figure 9](#).

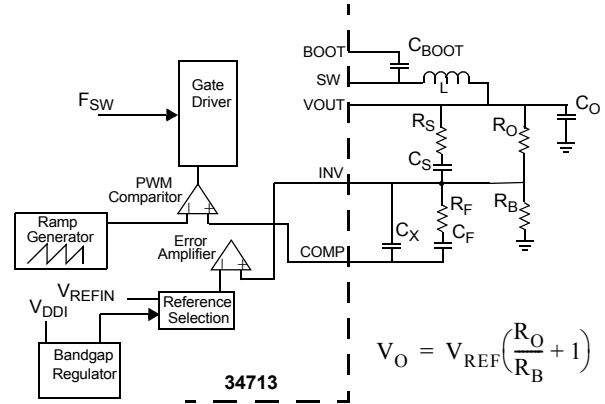


Figure 9. Type III Compensation Network

Consider the crossover frequency, F_{CROSS} , of the open loop gain at one-tenth of the switching frequency, F_{SW} .

Then,

$$F_{CROSS} = \frac{10}{2\pi \cdot R_O C_F} \Rightarrow$$

$$C_F = \frac{10}{2\pi \cdot R_O F_{CROSS}}$$

where R_O is a user selected resistor. Knowing the LC frequency, it can be obtained the values of R_F and C_S :

$$F_{LC} = \frac{1}{2\pi \sqrt{LC_o}} = F_{z1} = F_{z2}$$

$$F_{z1} = \frac{1}{2\pi \cdot R_F C_F}$$

$$F_{z2} = \frac{1}{2\pi \cdot R_O C_S}$$

This gives as a result,

$$R_F = \frac{1}{2\pi \cdot C_F F_{z1}} \quad \&$$

$$C_S = \frac{1}{2\pi \cdot R_O F_{z2}}$$

Calculate R_S by placing the Pole 1 at the ESR zero frequency:

$$F_{ESR} = \frac{1}{2\pi * C_o * ESR} = F_{P1}$$

$$F_{P1} = \frac{1}{2\pi * R_s C_s}$$

$$\Rightarrow R_s = \frac{1}{2\pi * F_{P1} C_s}$$

Equating the Pole 2 to 5 times the Crossover Frequency to achieve a faster response and a proper phase margin,

$$5 * F_{CROSS} = F_{P2} = \frac{1}{2\pi * R_F \frac{C_F C_X}{C_F + C_X}}$$

$$\Rightarrow C_X = \frac{C_F}{2\pi * R_F C_F F_{P2} - 1}$$

BOOTSTRAP CAPACITOR

The bootstrap capacitor is needed to supply the gate voltage for the high side MOSFET. This N-Channel MOSFET needs a voltage difference between its gate and source to be able to turn on. The high side MOSFET source is the SW node, so it is not ground and it is floating and moving in voltage, so we cannot just apply a voltage directly to the gate of the high side that is referenced to ground, we need a voltage referenced to the SW node. That is why the bootstrap capacitor is needed for. This capacitor charges during the high side off time, since the low side will be on during that time, so the SW node and the bottom of the bootstrap capacitor will be connected to ground and the top of the capacitor will be connected to a voltage source, so the capacitor will charge up to that voltage source (say 5.0 V). Now when the low side MOSFET switches off and the high side MOSFET switches on, the SW node rises up to Vin, and the voltage on the boot pin will be Vcap + Vin. So the gate of the high side will have Vcap across it and it will be able to

stay enhanced. A 0.1 μF capacitor is a good value for this bootstrap element.

LAYOUT GUIDELINES

The layout of any switching regulator requires careful consideration. First, there are high di/dt signals present, and the traces carrying these signals need to be kept as short and as wide as possible to minimize the trace inductance, and therefore reduce the voltage spikes they can create. To do this, an understanding of the major current carrying loops is important. See [Figure 10](#). These loops, and their associated components, should be placed in such a way as to minimize the loop size to prevent coupling to other parts of the circuit. Also, the current carrying power traces and their associated return traces should run adjacent to one another, to minimize the amount of noise coupling. If sensitive traces must cross the current carrying traces, they should be made perpendicular to one another to reduce field interaction.

Second, small signal components which connect to sensitive nodes need consideration. The critical small signal components are the ones associated with the feedback circuit. The high impedance input of the error amp is especially sensitive to noise, and the feedback and compensation components should be placed as far from the switch node, and as close to the input of the error amplifier as possible. Other critical small signal components include the bypass capacitors for VIN, VREFIN, and VDDI. Locate the bypass capacitors as close to the pin as possible.

The use of a multi-layer printed circuit board is recommended. Dedicate one layer, usually the layer under the top layer, as a ground plane. Make all critical component ground connections with vias to this layer. Make sure that the power ground, PGND, is connected directly to the ground plane and not routed through the thermal pad or analog ground. Dedicate another layer as a power plane and split this plane into local areas for common voltage nets.

The IC input supply (VIN) should be connected with a dedicated trace to the input supply. This will help prevent noise from the Buck Regulator's power input (PVIN) from injecting switching noise into the IC's analog circuitry.

In order to effectively transfer heat from the top layer to the ground plane and other layers of the printed circuit board, thermal vias need to be used in the thermal pad design. It is recommended that 5 to 9 vias be spaced evenly and have a finished diameter of 0.3 mm.

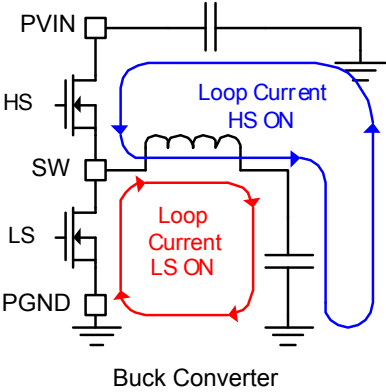


Figure 10. Current Loops

SOFT START SELECTION

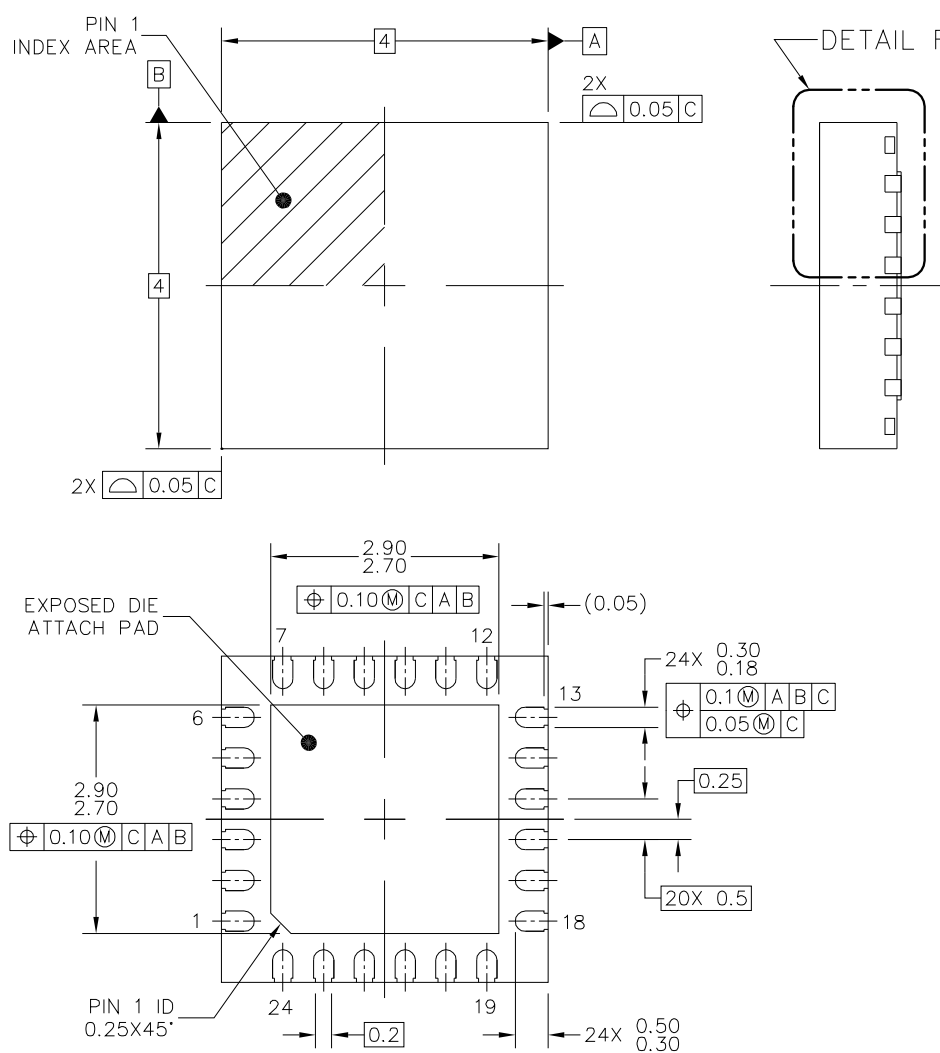
Table 6 shows the voltage that should be applied to the terminal ILIM to get the desired configuration of the soft start timing.

Table 6. ILIM Table

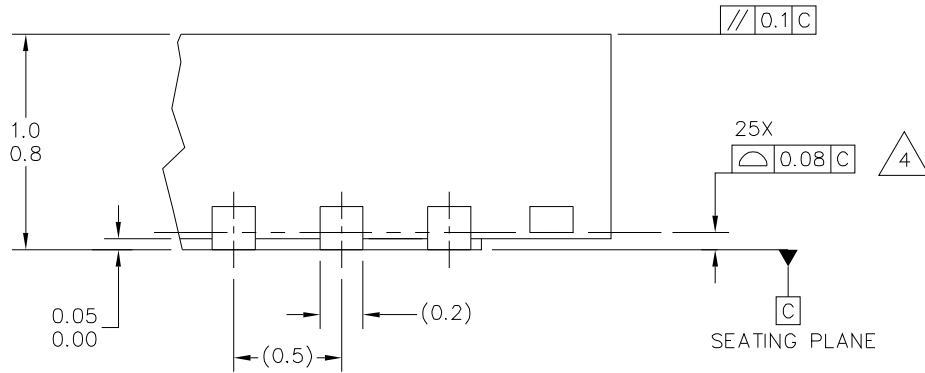
Soft Start (ms)	Voltage Applied to ILIM
3.2	1.25 - 1.49
1.6	1.50 - 1.81
0.8	1.82 - 2.13
0.4	2.14 - 2.50

PACKAGING

PACKAGING DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: QFN, THERMALLY ENHANCED 4 X 4 X 0.9, 0.5 PITCH, 24 TERMINAL	DOCUMENT NO: 98ASA00474D		REV: A
	CASE NUMBER: 2296-02		11 OCT 2012
	STANDARD: NON-JEDEC		



DETAIL F
VIEW ROTATED 90°CW

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: QFN, THERMALLY ENHANCED 4 X 4 X 0.9, 0.5 PITCH, 24 TERMINAL		DOCUMENT NO: 98ASA00474D	REV: A	
		CASE NUMBER: 2296-02	11 OCT 2012	
		STANDARD: NON-JEDEC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS IS A NON-JEDEC REGISTERED PACKAGE.
4.  COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: QFN, THERMALLY ENHANCED 4 X 4 X 0.9, 0.5 PITCH, 24 TERMINAL	DOCUMENT NO: 98ASA00474D		REV: A
	CASE NUMBER: 2296-02		11 OCT 2012
	STANDARD: NON-JEDEC		

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	2/2006	- Pre-release version - Implemented Revision History page
2.0	11/2006	- Initial release - Converted format from Market Assessment to Product Preview - Major updates to the data, form, and style
3.0	2/2007	Major updates to the data, form, and style
4.0	5/2007	- Changed Feature from 2% to 1%, relabeled to include soft start - Changed 34713 Simplified Application Diagram - Made change to 34713 Simplified Internal Block Diagram - Removed Machine Model in Maximum Ratings - Changed Input DC Supply Current⁽¹¹⁾ Normal mode and Input DC Supply Current⁽¹¹⁾ Shutdown mode - Changed Output Voltage Accuracy^{(12),(14)} - Changed Soft start Adjusting reference Voltage Range and Short-circuit Current Limit - Changed High Side N-CH Power MOSFET (M3) RDS(ON)⁽¹²⁾ and Low Side N-CH Power MOSFET (M4) RDS(ON)⁽¹²⁾ - Changed M2 RDS(ON) and PVIN Pin Leakage Current - Changed SD Pin Internal Pull-up Resistor⁽¹⁵⁾ - Changed Soft Start Duration (Normal Mode) - Changed Over-current Limit Retry Time-out Period and Output Under-voltage/Over-voltage Filter Delay Timer - Changed PG Reset Delay and Thermal Shutdown Retry Timeout Period⁽¹⁶⁾ - Changed definition for Soft Start Adjustment input (ILIM) - Changed drawings in Typical Applications - Changed drawing in Type III Compensation Network - Changed table for Soft Start Selection - Removed PC34713EP/R2 from the ordering information and added MC34713EP/R2 - Changed the data sheet status to Advance Information
5.0	1/2008	- Made changes to Switching Node (SW) Pin, BOOT Pin (Referenced to SW Pin), Output Under-voltage Threshold, Output Over-voltage Threshold, High Side N-CH Power MOSFET (M3) RDS(ON)⁽¹²⁾, Low Side N-CH Power MOSFET (M4) RDS(ON)⁽¹²⁾, Charge Device Model - Added Machine Model (MM), SW Leakage Current (Standby and Shutdown modes), Error Amplifier DC Gain⁽¹⁵⁾, Error Amplifier Unit Gain Bandwidth⁽¹⁵⁾, Error Amplifier Slew Rate⁽¹⁵⁾, Error Amplifier Input Offset⁽¹⁵⁾, High Side MOSFET Drain Voltage (PVIN) Pin - Added pin 25 to Figure 3 and the 34713 Pin Definitions - Added the section Layout Guidelines
6.0	11/2014	- Updated case outline ((changed 98ARL10577D to 98ASA00474D) as per PCN 16331 - Updated format and style

**How to Reach Us:**

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. SMARTMOS is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© 2014 Freescale Semiconductor, Inc.

Document Number: MC34713
Rev. 6.0
11/2014

