Ultra-Wideband, Fixed Gain Video BUFFER AMPLIFIER with Disable

FEATURES

- VERY HIGH BANDWIDTH (G = +2): 800MHz
- FLEXIBLE SUPPLY RANGE:
  +5V to +12V Single Supply
  ±2.5V to ±6V Dual Supplies
- INTERNALLY FIXED GAIN: +2 or ±1
- LOW SUPPLY CURRENT: 13mA
- LOW DISABLED CURRENT: 120µA
- HIGH OUTPUT CURRENT: 100mA
- OUTPUT VOLTAGE SWING: ±4.0V
- SOT23-6 AVAILABLE

APPLICATIONS

- BROADBAND VIDEO LINE DRIVERS
- MULTIPLE LINE VIDEO DA
- PORTABLE INSTRUMENTS
- ADC BUFFERS
- ACTIVE FILTERS
- HFA1112 IMPROVED DROP-IN

OPA693 RELATED PRODUCTS

	SINGLES	DUALS	TRIPLES
Voltage Feedback	OPA690	OPA2690	OPA3690
Current Feedback	OPA691	OPA2691	OPA3691
Fixed Gain	OPA692	—	OPA3692

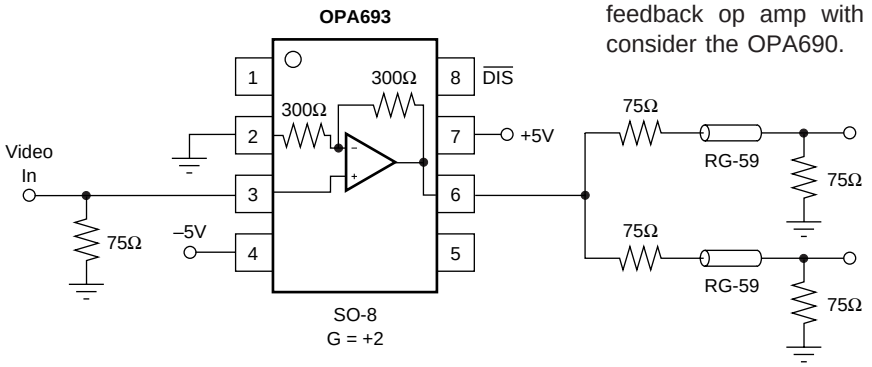
DESCRIPTION

The OPA693 provides an easy to use, broadband fixed gain buffer amplifier. Depending on the external connections, the internal resistor network may be used to provide either a fixed gain of +2 video buffer or a gain of +1 or –1 voltage buffer. Operating on a low 13mA supply current, the OPA693 offers a slew rate (2500V/µs) and bandwidth (> 800MHz) normally associated with a much higher supply current. A new output stage architecture delivers high output current with a minimal headroom and crossover distortion. This gives exceptional single-supply operation. Using a single +5V supply, the OPA693 can deliver a $2.5V_{PP}$ swing with over 80mA drive current and 500MHz bandwidth at a gain of +2. This combination of features makes the OPA693 an ideal RGB line driver or single-supply undersampling Analog-to-Digital Converter (ADC) input driver.

The OPA693's low 13mA supply current is precisely trimmed at 25°C. This trim, along with low drift over temperature, ensures lower maximum supply current than competing products that report only a room temperature nominal supply current. System power may be further reduced by using the optional disable control pin. Leaving this disable pin open, or holding it HIGH, gives normal operation. This optional disable allows the OPA693 to fit into existing video buffer layouts where the disable pin is unconnected to get improved performance with no board changes. If pulled LOW, the OPA693 supply current drops to less than 120µA while the output goes into a high impedance state. This feature may be used for power savings.

The low gain stable current feedback architecture used in the OPA693 is particularly suitable for high full-power bandwidth cable driving requirements. Where the additional flexibility of an op amp is required, consider the OPA695 ultra wideband current feedback op amp. Where a unity gain stable voltage feedback op amp with very high slew rate is required, consider the OPA690.

PRODUCT PREVIEW



800MHz, 2-Output Component Video DA

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply	±6.5VDC
Internal Power Dissipation[2]	See Thermal Information
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: D, DVB	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Packages must be derated based on specified θ_{JA}. Maximum T_J must be observed.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

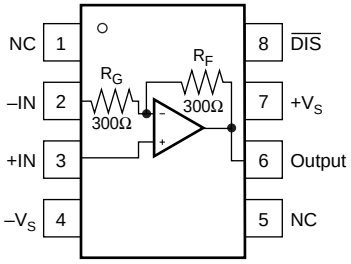
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA693	SO-8	D	–40°C to +85°C	OPA693D	OPA693ID	Rails, 100
"	"	"	"	"	OPA693IDR	Tape and Reel, 2500
OPA693	SOT23-6	DBV	–40°C to +85°C	TBD	OPA693IDBVT	Tape and Reel, 250
"	"	"	"	"	OPA693IDBVR	Tape and Reel, 3000

NOTES: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PRODUCT PREVIEW

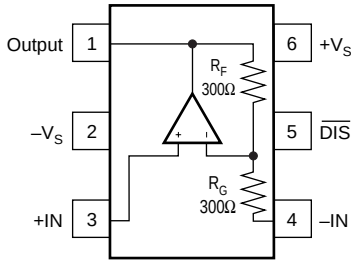
PIN CONFIGURATION

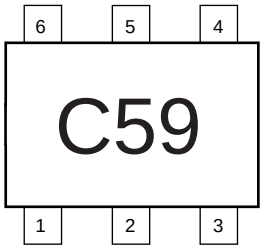
Top View **SO-8**



NC: No Connection

Top View **SOT23-6**





Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **25°C.**

G = +2 (–IN grounded) and $R_L = 100\Omega$ (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA693ID, IDBV						
		TYP	MIN/MAX OVER TEMPERATURE[1]					
		+25°C	+25°C	0°C to 70°C	–40°C to +85°C	UNITS	MIN/ MAX	TEST LEVEL[2]
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth ($V_O < 0.5V_{PP}$)	G = +1	1200				MHz	typ	C
	G = +2	800	600	550	500	MHz	min	B
	G = –1	700	550	500	450	MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, $V_O < 0.5V_{PP}$	400	300	250	200	MHz	min	B
Peaking at a Gain of +1	$V_O < 0.5V_{PP}$	0.5	1	1.5	1.8	dB	max	B
Large-Signal Bandwidth	G = +2, $V_O = 5V_{PP}$	220				MHz	typ	C
Slew Rate	G = +2, 4V Step	2400	2100	1375	1350	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	0.7				ns	typ	C
	G = +2, V_O = 5V Step	2.2				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	5				ns	typ	C
0.1%	G = +2, V_O = 2V Step	3				ns	typ	C
Harmonic Distortion	G = +2, f = 10MHz, $V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 100\Omega$	–75				dBc	max	B
	$R_L \geq 500\Omega$	–85				dBc	max	B
3rd-Harmonic	$R_L = 100\Omega$	–89				dBc	max	B
	$R_L \geq 500\Omega$	–99				dBc	max	B
Input Voltage Noise	f > 1MHz	1.6				nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	17				pA/√Hz	max	B
Inverting Input Current Noise (internal)	f > 1MHz	21				pA/√Hz	max	B
Differential Gain	NTSC, $R_L = 150\Omega$	0.02				%	typ	C
	NTSC, $R_L = 37.5\Omega$	0.05				%	typ	C
Differential Phase	NTSC, $R_L = 150\Omega$	0.01				deg	typ	C
	NTSC, $R_L = 37.5\Omega$	0.05				deg	typ	C
DC PERFORMANCE[3]								
Gain Error	G = +1	±0.2				%	typ	C
	G = +2	±0.3	**±0.6**	±0.7	±0.8	%	max	A
	G = –1, $R_S = 0\Omega$	±0.2	±0.5	±0.6	±0.8	%	max	B
Internal R_F and R_G								
Maximum		300	**341**	345	348	Ω	max	A
Minimum		300	**264**	260	255	Ω	min	A
Average Drift			0.13	0.13	0.13	%/C°	max	B
Input Offset Voltage	V_{CM} = 0V	±0.7	**±2.0**			mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±12	±20	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	+10	**±30**			µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V					nA/°C	max	B
Inverting Input Bias Current (internal)	V_{CM} = 0V	±10	**±40**			µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V					nA°C	max	B
INPUT								
Common-Mode Input Range		±3.5	**±3.4**	±3.3	±3.2	V	min	B
Noninverting Input Impedance		100 || 2				kΩ || pF	typ	C
OUTPUT								
Voltage Output Swing	No Load	±4.0	**±3.8**			V	min	A
	100Ω Load	±3.9	**±3.7**			V	min	A
Current Output, Sourcing		+120	**+90**			mA	min	A
Sinking		–120	**–90**			mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.12				Ω	typ	C

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and +25°C specifications. Junction temperature = ambient temperature +10°C at high temperature limit specifications.
(2) Test Levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(3) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

Boldface limits are tested at **25°C.**

G = +2 (–IN grounded) and R_L = 100Ω (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA693ID, IDBV						TEST LEVEL(2)
		TYP	MIN/MAX OVER TEMPERATURE(1)					
		+25°C	+25°C	0°C to 70°C	–40°C to +85°C	UNITS	MIN/ MAX	
DISABLE/POWER DOWN ($\overline{DIS}$ Pin)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0	–80	**–120**			µA	max	A
Disable Time	V_{IN} = +1V_{DC}	1				µs	typ	C
Enable Time	V_{IN} = +1V_{DC}	25				ns	typ	C
Off Isolation	G = +2, 5MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn On Glitch	G = +2, R_L = 150Ω, V_{IN} = V	±100				mV	typ	C
Turn Off Glitch	G = +2, R_L= 150Ω, V_{IN} = V	±20				mV	typ	C
Enable Voltage	+V_S = +5V	3.3	**3.5**			V	min	A
Disable Voltage	+V_S = +5V	1.8	**1.7**			V	max	A
Control Pin Input Bias Current	$V_{\overline{DIS}}$ = 0	75	**130**			µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6**	±6	±6	V	max	A
Max Quiescent Current	V_S = ±5V	13	**13.3**			mA	max	A
Min Quiescent Current	V_S = ±5V	13	**12.7**			mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input Referred	58	**55**			dB	min	A
TEMPERATURE RANGE								
Specification: D, DBV		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}								
D SO-8		125				°C/W	typ	C
DBV SOT23-6		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient temperature for low temperature limit and +25°C specifications. Junction temperature = ambient temperature +10°C at high temperature limit specifications.
(2) Test Levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(3) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA693ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 693	Samples
OPA693IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C59	Samples
OPA693IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C59	Samples
OPA693IDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C59	Samples
OPA693IDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	C59	Samples
OPA693IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 693	Samples

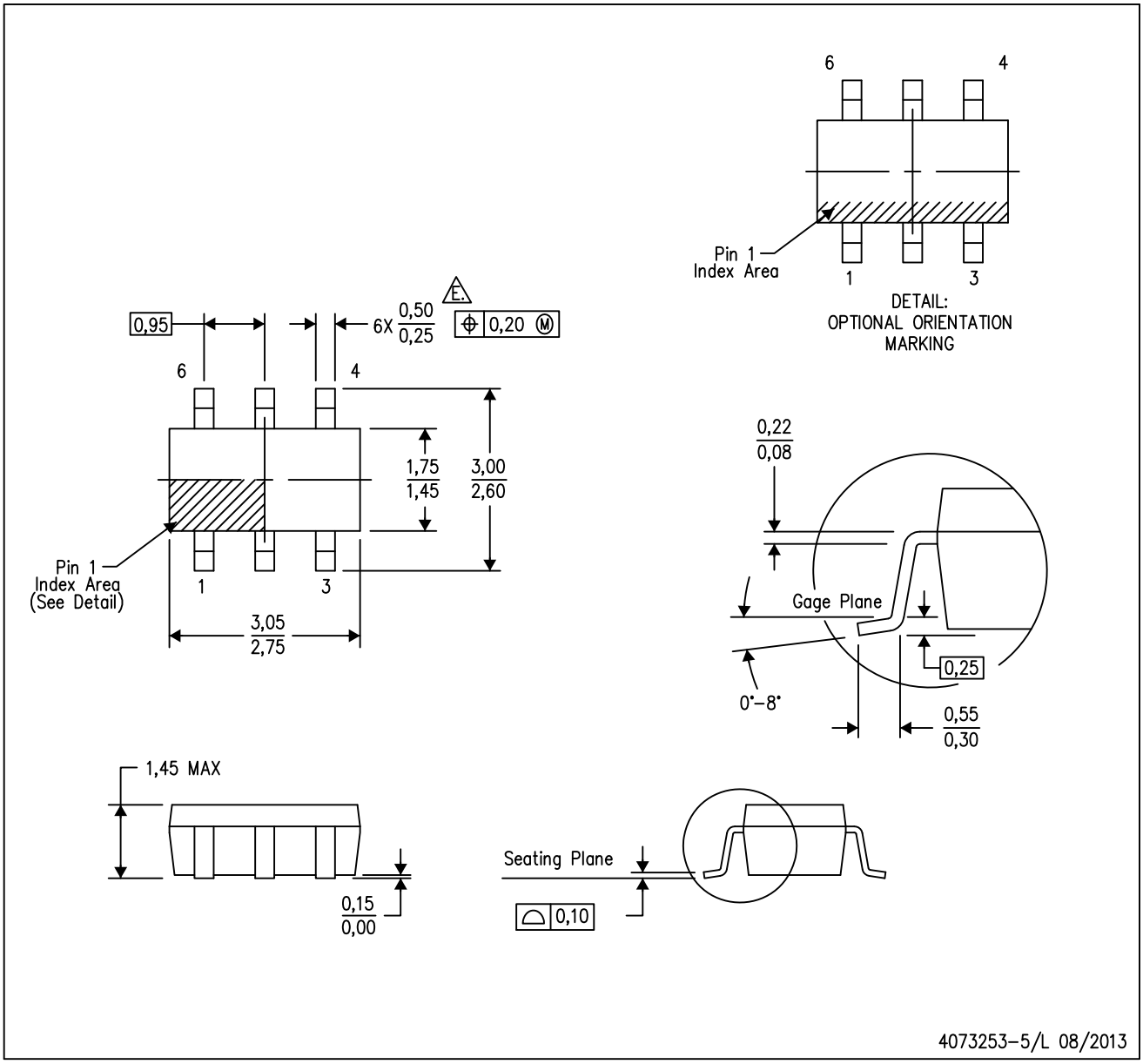
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

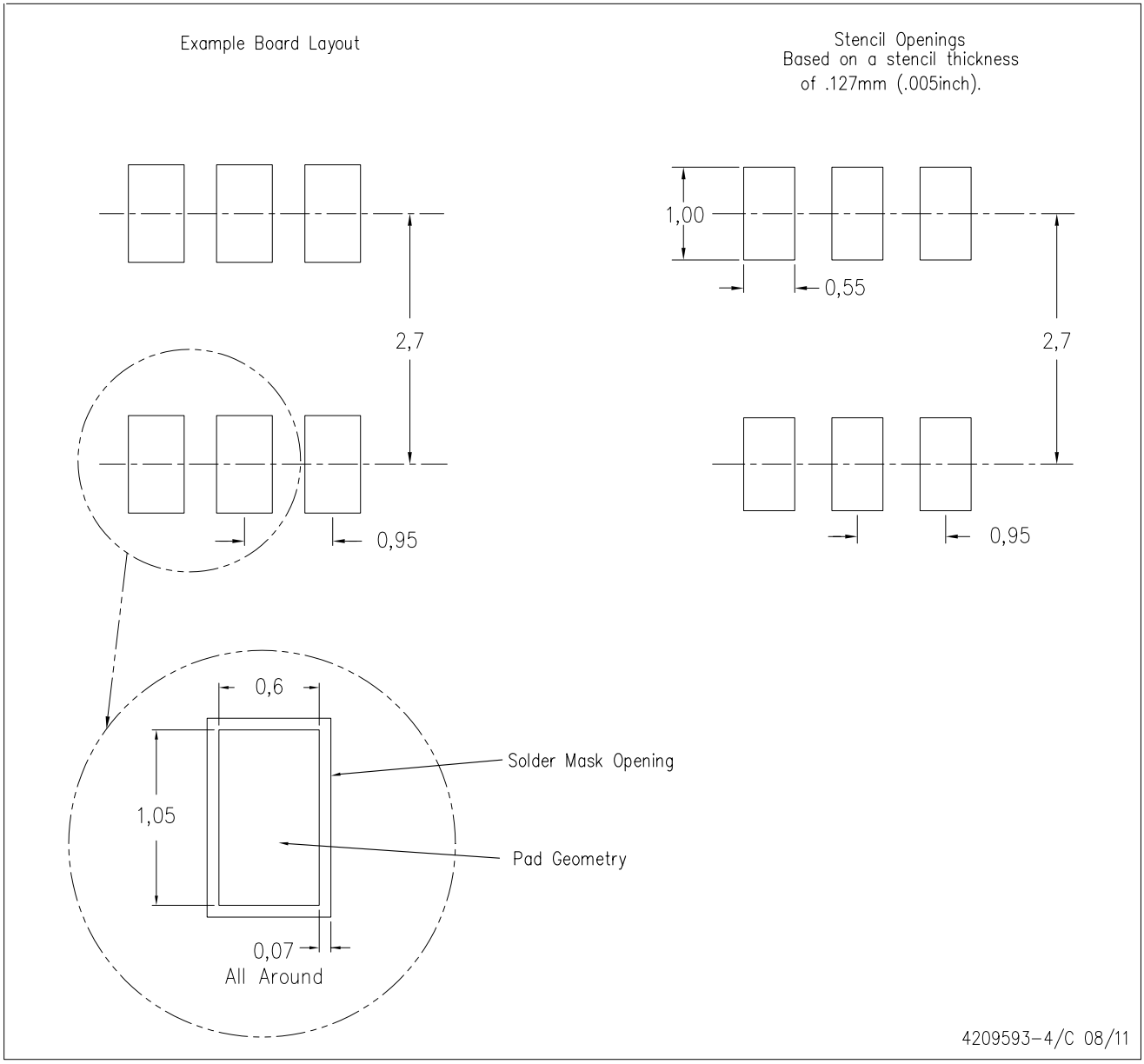
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



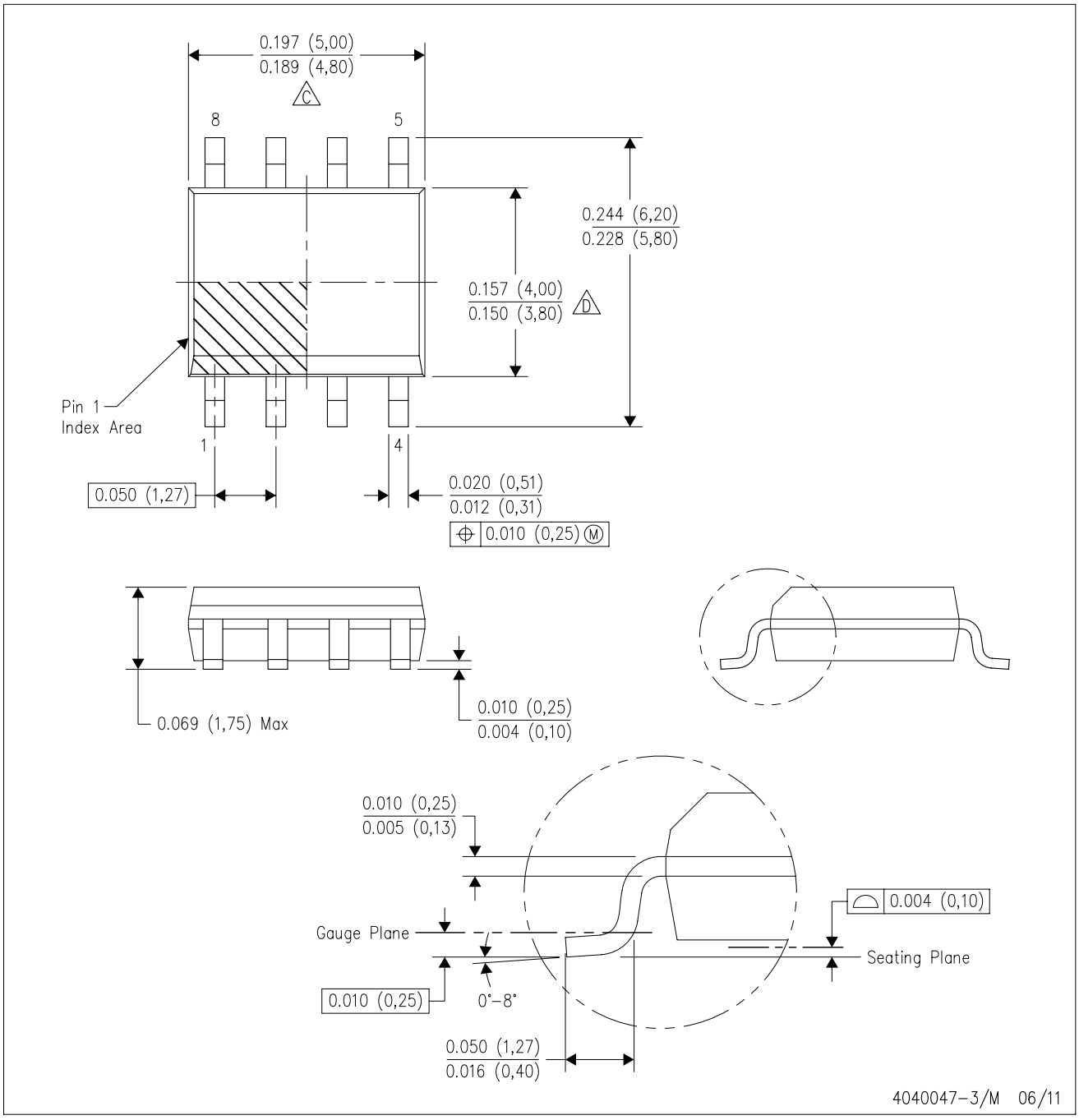
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



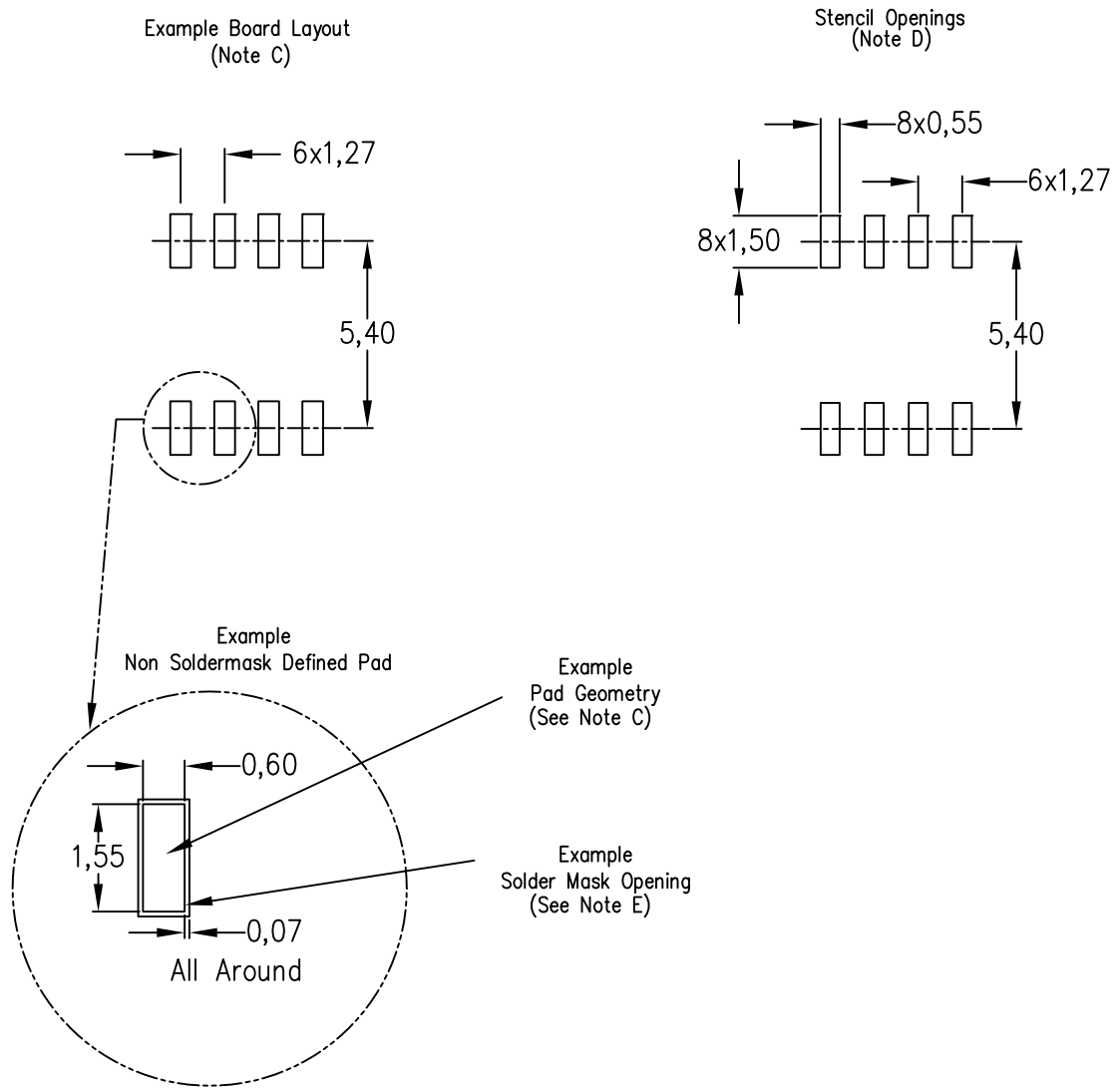
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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