High Voltage 500mA, 200kHz Step-Down Switching Regulator with 100µA Quiescent Current

FEATURES

- **Wide Input Range: 3.3V to 60V**
- **Load Dump (Input Transient) Protection to 80V**
- **500mA Peak Switch Current**
- **Burst Mode® Operation: 100µA Quiescent Current****
- **Low Shutdown Current: I_Q < 1µA**
- **Defeatable Burst Mode Operation**
- 200kHz Switching Frequency
- Saturating Switch Design: 0.8Ω On-Resistance
- Peak Switch Current Maintained Over Full Duty Cycle Range*
- 1.25V Feedback Reference Voltage
- Easily Synchronizable
- Soft-Start Capability
- Small 10-Pin Thermally Enhanced DFN Package

APPLICATIONS

- High Voltage Power Conversion
- 14V and 42V Automotive Systems
- Industrial Power Systems
- Distributed Power Systems
- Battery-Powered Systems
- Powered Ethernet

**See Burst Mode Operation section for conditions.

DESCRIPTION

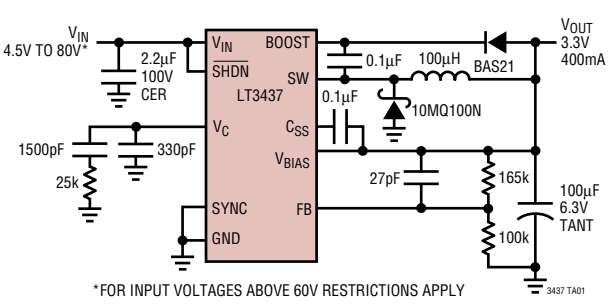
The LT®3437 is a 200kHz monolithic buck switching regulator that accepts input voltages up to 80V. A high efficiency 500mA, 0.8Ω switch is included on the die along with all the necessary oscillator, control and logic circuitry. Current mode topology is used for fast transient response and good loop stability.

Innovative design techniques along with a new high voltage process achieve high efficiency over a wide input range. Efficiency is maintained over a wide output current range by employing Burst Mode operation at low currents, utilizing the output to bias the internal circuitry, and by using a supply boost capacitor to fully saturate the power switch. Burst Mode operation can be defeated by a logic high signal on the SYNC pin which results in lower light load ripple at the expense of light load efficiency. Patented circuitry maintains peak switch current over the full duty cycle range.* Shutdown reduces input supply current to less than 1µA. External synchronization can be implemented by driving the SYNC pin with logic-level inputs. A single capacitor from the C_{SS} pin to the output provides a controlled output voltage ramp (soft-start).

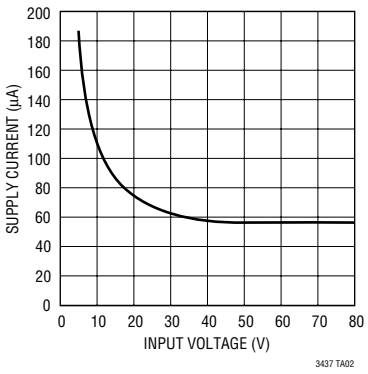
The LT3437 is available in a low profile (0.75mm) 3mm × 3mm 10-pin DFN package or a 16-Pin TSSOP Package, both with exposed pad leadframes for low thermal resistance.

TYPICAL APPLICATION

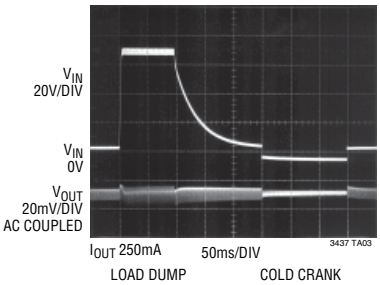
14V to 3.3V Step-Down Converter with 100µA No Load Quiescent Current



Supply Current vs Input Voltage



Input Voltage Transient Response



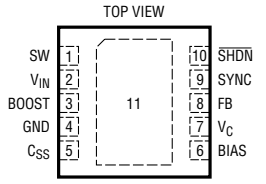
ABSOLUTE MAXIMUM RATINGS

(Note 1)

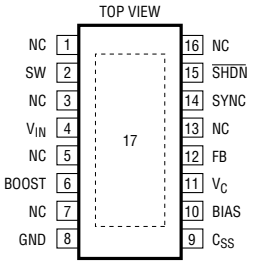
V_{IN}, $\overline{SHDN}$, BIAS, SW Operating 60V
V_{IN}, $\overline{SHDN}$ 100ms Transient, <15% Duty Cycle 80V
BOOST Pin Above SW 35V
BOOST Pin Voltage Operating 75V
BOOST Pin 100ms Transient, <15% Duty Cycle 85V
SYNC, C_{SS}, FB 6V

Operating Junction Temperature Range
LT3437EDD (Note 2) ..... –40°C to 125°C
LT3437IDD (Note 2) ..... –40°C to 125°C
LT3437EFE (Note 2) ..... –40°C to 125°C
LT3437IFE (Note 2) ..... –40°C to 125°C
LT3437HFE (Note 2) ..... –40°C to 140°C
Storage Temperature Range ..... –65°C to 125°C
DD Package ..... –65°C to 125°C
FE Package ..... –65°C to 150°C

PACKAGE/ORDER INFORMATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
θ_{JA} = 45°C/W, $\theta_{JC(PAD)}$ = 10°C/W
EXPOSED PAD IS GND (PIN 11)
MUST BE SOLDERED TO GND (PIN 4)



FE PACKAGE
16-LEAD PLASTIC TSSOP
θ_{JA} = 45°C/W, $\theta_{JC(PAD)}$ = 10°C/W
EXPOSED PAD IS GND (PIN 17)
MUST BE SOLDERED TO GND (PIN 8)

ORDER PART NUMBER	DD PART MARKING	ORDER PART NUMBER	FE PART MARKING
LT3437EDD LT3437IDD	LBDJ LBDK	LT3437EFE LT3437IFE LT3437HFE	3437EFE 3437IFE 3437HFE

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C to 125°C temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, $\overline{SHDN}$ = 12V, BIAS = 5V, FB = 1.25V, C_{SS}/SYNC = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Threshold		●	1.15	1.3	1.45	V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = 12V	●		5	30	µA
	Minimum Input Voltage (Note 3)		●		2.5	3	V
I_{VINS}	Supply Shutdown Current	$\overline{SHDN}$ = 0V, BOOST = 0V, FB/PGFB = 0V, BIAS = 0V			0.1	2	µA
	Supply Sleep Current (Note 4)	BIAS = 0V, FB = 1.35V FB = 1.35V	● ●		150 45	300 75	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C to 125°C temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, $\overline{SHDN}$ = 12V, BIAS = 5V, FB = 1.25V, C_{SS}/SYNC = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{VIN}	Supply Quiescent Current	BIAS = 0V, FB = 1.15V, V_C = 0.8V, SYNC = 2V BIAS = 5V, FB = 1.15V, V_C = 0.8V, SYNC = 2V			1.35 0.475	2 1	mA mA
	Minimum BIAS Voltage (Note 5)				2.7	3.15	V
I_{BIASS}	BIAS Sleep Current (Note 4)		●		110	180	µA
I_{BIAS}	BIAS Quiescent Current	SYNC = 2V			0.75	1	mA
	Minimum Boost Voltage (Note 6)	I_{SW} = 500mA			1.8	2.5	V
	Input Boost Current (Note 7)	I_{SW} = 0.5A I_{SW} = 0.25A			11 8	16 13	mA mA
V_{REF}	Reference Voltage (V_{REF})	3.3V < V_{IN} < 80V	●	1.225	1.25	1.275	V
I_{FB}	FB Input Bias Current				50	200	nA
	EA Voltage Gain (Note 8)				900		V/V
	EA Voltage g_m	dI(V_C)= ±10µA			650		µMho
	EA Source Current	FB = 1.15V		15	35	55	µA
	EA Sink Current	FB = 1.35V		15	30	55	µA
	V_C to SW g_m				1		A/V
	V_C Switching Threshold	V_{SYNC} = 2V			500		mV
	V_C High Clamp			1.5	1.75	2.1	V
I_{PK}	SW Current Limit		●	500	650	900	mA
SW V_{CESAT}	Switch Saturation Voltage (Note 9)	I_{SW} = 250mA I_{SW} = 500mA	● ●		200 400	400 800	mV mV
	Switching Frequency		●	165	200	240	kHz
	Maximum Duty Cycle				95		%
	Minimum SYNC Amplitude				1.5	2	V
	SYNC Frequency Range			240		700	kHz
	SYNC Input Impedance				50		kΩ
I_{CSS}	C_{SS} Current Threshold (Note 10)	FB = 0V		4	10	16	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C to 140°C temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, $\overline{SHDN}$ = 12V, BIAS = 5V, FB = 1.25V, C_{SS}/SYNC = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Threshold		●	1.1	1.3	1.5	V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Current	$\overline{SHDN}$ = 12V	●		5	30	µA
	Minimum Input Voltage (Note 3)		●		2.5	3.5	V
I_{VINS}	Supply Shutdown Current	$\overline{SHDN}$ = 0V, BOOST = 0V, FB/PGFB = 0V, BIAS = 0V			0.1	2	µA
	Supply Sleep Current (Note 4)	BIAS = 0V, FB = 1.35V FB = 1.35V	● ●		150 45	300 75	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C to 140°C temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, $\overline{SHDN}$ = 12V, BIAS = 5V, FB = 1.25V, C_{SS}/SYNC = 0V unless otherwise noted.

I_{VIN}	Supply Quiescent Current	BIAS = 0V, FB = 1.15V, V_C = 0.8V, SYNC = 2V BIAS = 5V, FB = 1.15V, V_C = 0.8V, SYNC = 2V			1.35 0.475	2 1	mA mA
	Minimum BIAS Voltage (Note 5)				2.7	3.15	V
I_{BIASS}	BIAS Sleep Current (Note 4)		●		110	180	µA
I_{BIAS}	BIAS Quiescent Current	SYNC = 2V			0.75	1	mA
	Minimum Boost Voltage (Note 6)	I_{SW} = 500mA			1.8	2.5	V
	Input Boost Current (Note 7)	I_{SW} = 0.5A I_{SW} = 0.25A			11 8	16 13	mA mA
V_{REF}	Reference Voltage (V_{REF})	3.3V < V_{VIN} < 60V V_{VIN} = 80V	● ●	1.212 1.190	1.25 1.25	1.288 1.288	V V
I_{FB}	FB Input Bias Current				50	200	nA
	EA Voltage Gain (Note 8)				900		V/V
	EA Voltage g_m	dI(V_C)= ±10µA			650		µMho
	EA Source Current	FB = 1.15V		15	35	55	µA
	EA Sink Current	FB = 1.35V		15	30	55	µA
	V_C to SW g_m				1		A/V
	V_C Switching Threshold	V_{SYNC} = 2V			500		mV
	V_C High Clamp			1.5	1.75	2.1	V
I_{PK}	SW Current Limit		●	400	650	900	mA
SW V_{CESAT}	Switch Saturation Voltage (Note 9)	I_{SW} = 250mA I_{SW} = 500mA	● ●		200 400	400 800	mV mV
	Switching Frequency		●	140	200	240	kHz
	Maximum Duty Cycle				95		%
	Minimum SYNC Amplitude				1.5	2	V
	SYNC Frequency Range			240		500	kHz
	SYNC Input Impedance				50		kΩ
I_{CSS}	C_{SS} Current Threshold (Note 10)	FB = 0V		4	10	16	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3437EDD/LT3437EFE are guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3437IDD/LT3437IFE are guaranteed and tested over the full –40°C to 125°C operating junction temperature range. The LT3437HFE is also tested to the LT3437 Electrical Characteristics table at 140°C operating junction temperature. High junction temperatures degrade operating lifetimes.

Note 3: Minimum input voltage is defined as the voltage where switching starts. Actual minimum input voltage to maintain a regulated output will depend upon output voltage and load current. See Applications Information.

Note 4: Supply input current is the quiescent current drawn by the input pin. Its typical value depends on the voltage on the BIAS pin and operating state of the LT3437. With the BIAS pin at 0V, all of the quiescent current required to operate the LT3437 will be provided by the V_{IN} pin. With the BIAS voltage above its minimum input voltage, a portion of the total quiescent current will be supplied by the BIAS pin. Supply sleep current is defined as the quiescent current during the "sleep" portion of Burst Mode operation. See Applications Information for determining application supply currents.

Note 5: Minimum BIAS voltage is the voltage on the BIAS pin when I_{BIAS} is sourced into the pin.

Note 6: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the internal power switch.

Note 7: Boost current is the current flowing into the BOOST pin with the pin held 3.3V above input voltage. It flows only during switch on time.

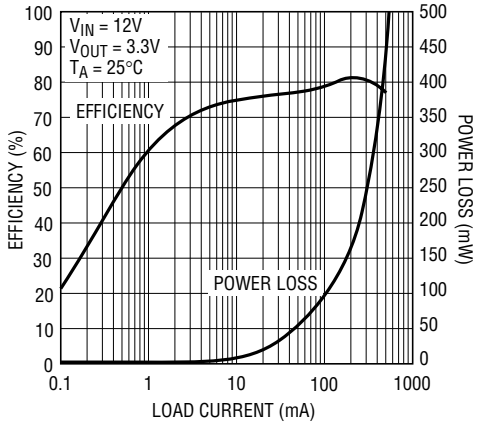
Note 8: Gain is measured with a V_C swing from 1.15V to 750mV.

Note 9: Switch saturation voltage guaranteed by correlation to wafer level measurements for DD package parts.

Note 10: The C_{SS} threshold is defined as the value of current sourced into the C_{SS} pin which results in an increase in sink current from the V_C pin. See the Soft-Start section in Applications Information.

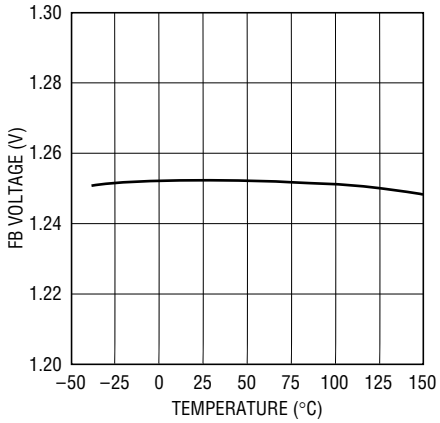
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency and Power Loss vs Load Current



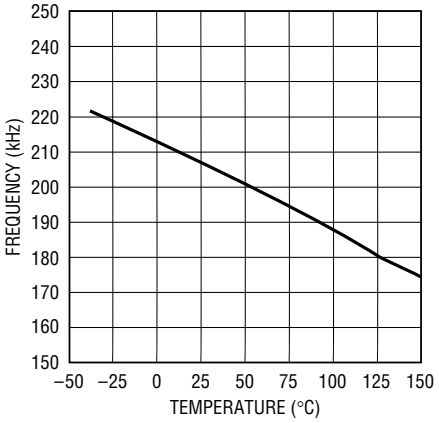
3437 G01

FB Voltage vs Temperature



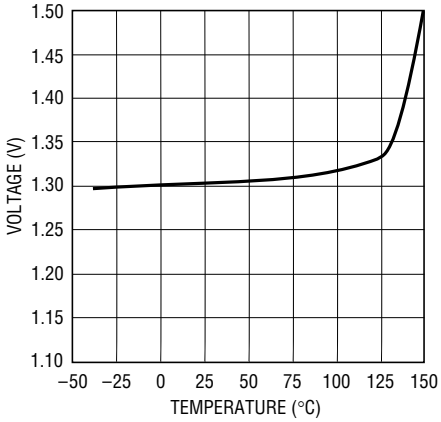
3437 G02

Oscillator Frequency vs Temperature



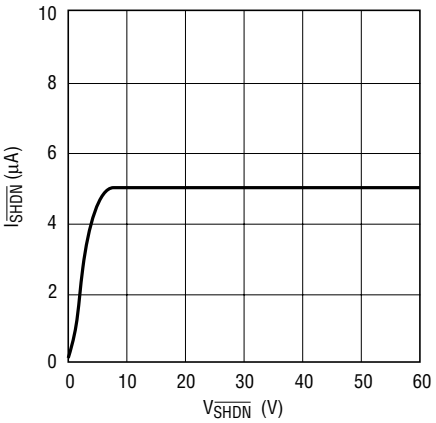
3437 G03

$\overline{SHDN}$ Threshold



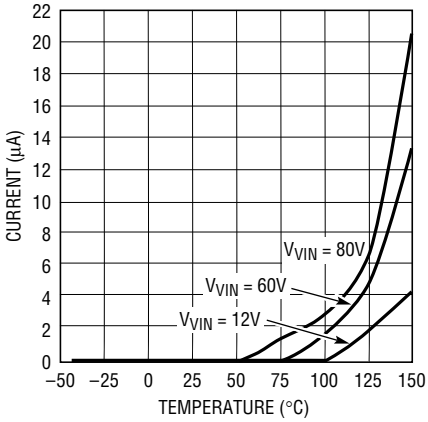
3437 G04

$\overline{SHDN}$ Pin Current



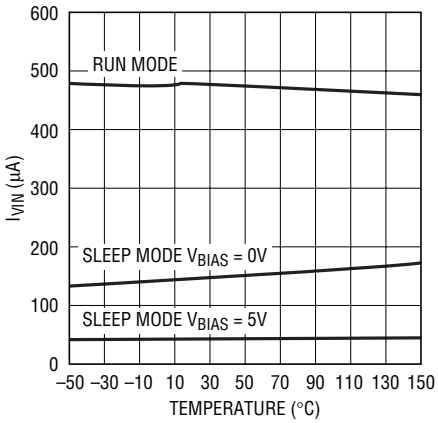
3437 G05

Shutdown Supply Current vs Temperature



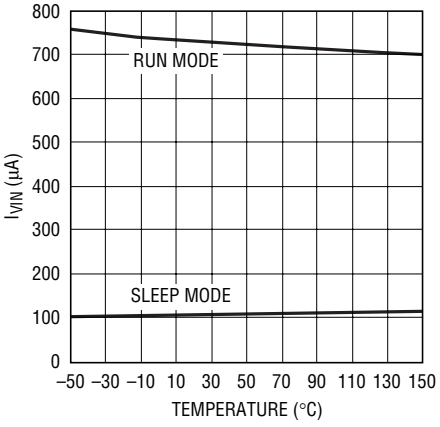
3437 G06

Input Current vs Temperature



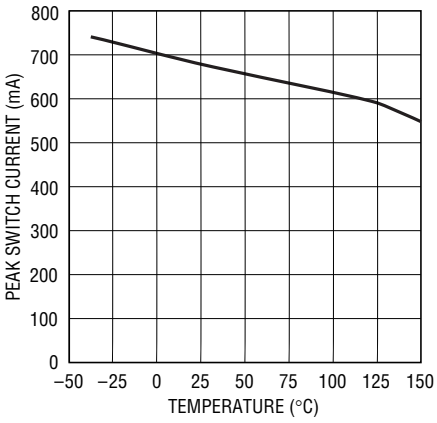
3437 G07

Bias Current vs Temperature



3437 G08

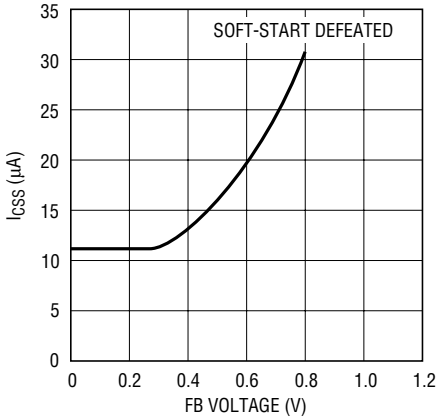
Switch Peak Current Limit vs Temperature



3437 G09

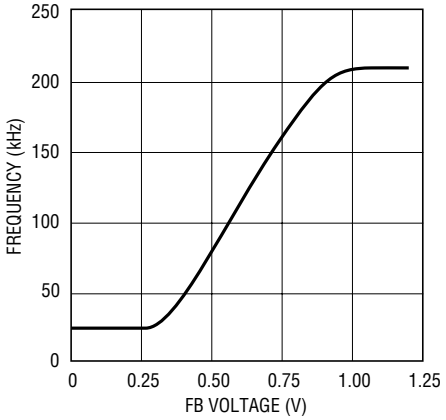
TYPICAL PERFORMANCE CHARACTERISTICS

Soft-Start Current Threshold vs FB Voltage



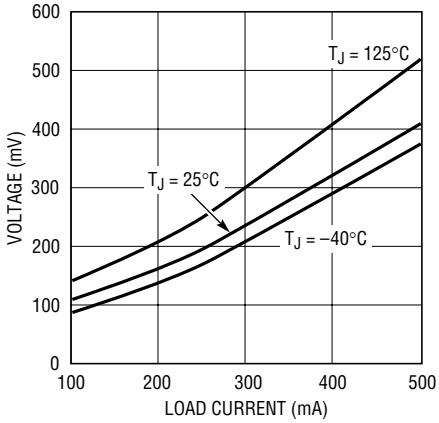
3437 G10

Oscillator Frequency vs FB Voltage



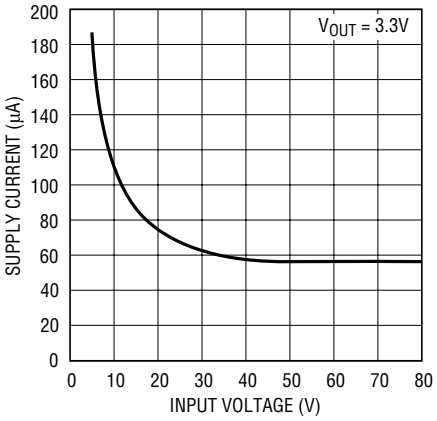
3437 G11

Switch On Voltage (V_{CESAT})



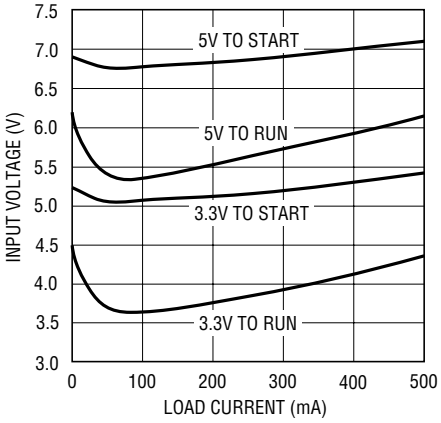
3437 G12

Supply Current vs Input Voltage



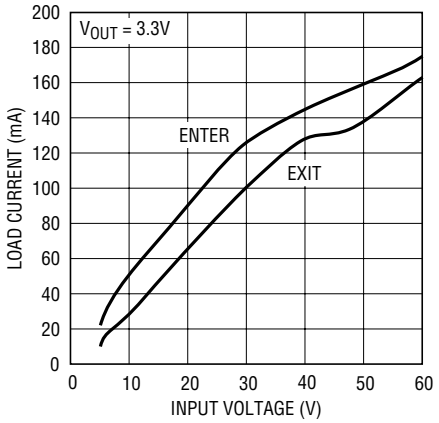
3437 F13

Minimum Input Voltage



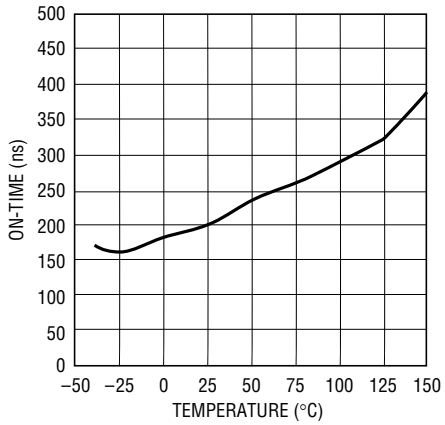
3437 G14

Burst Mode Threshold vs Input Voltage



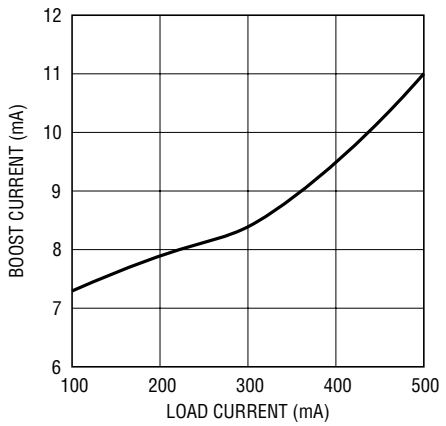
3437 G15

Minimum On-Time



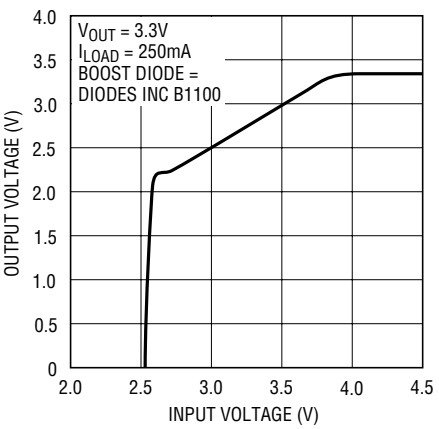
3437 G16

Boost Current vs Load Current



3437 G17

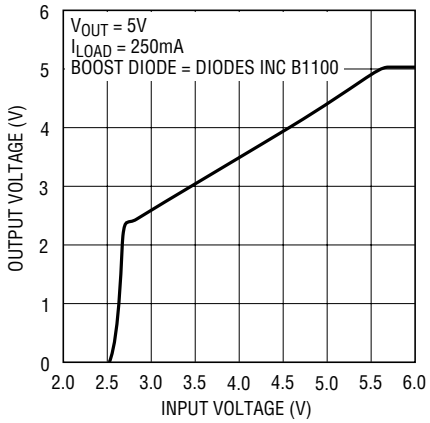
Dropout Operation



3437 G18

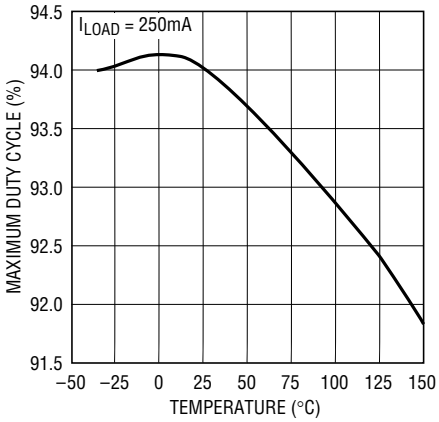
TYPICAL PERFORMANCE CHARACTERISTICS

Dropout Operation



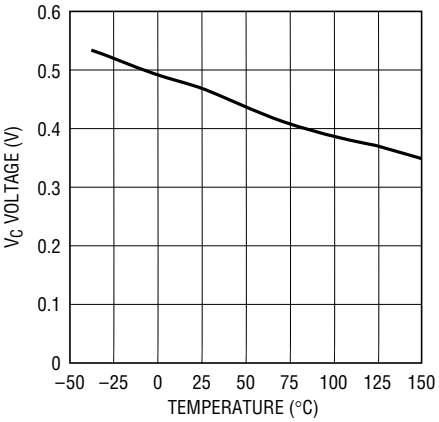
3437 G19

Maximum Duty Cycle vs Temperature



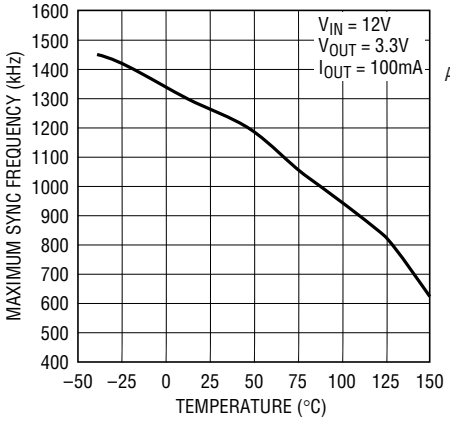
3437 G20

V_C Switching Threshold vs Temperature



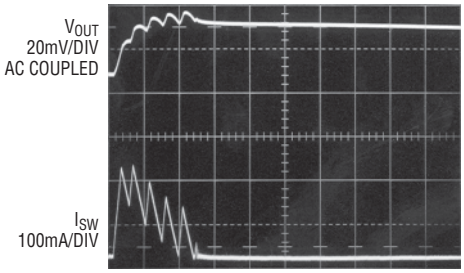
3437 G21

Maximum Sync Frequency vs Temperature



3437 G22

Burst Mode Operation

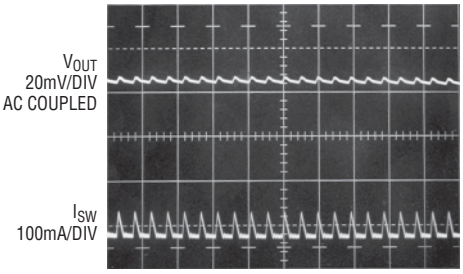


V_{IN} = 12V
V_{OUT} = 3.3V
I_Q = 100µA

10µs/DIV

3437 G23

Burst Mode Defeated

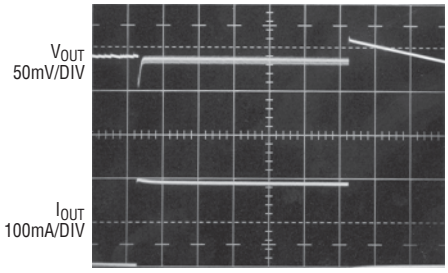


V_{IN} = 12V
V_{OUT} = 3.3V
I_Q = 1.7mA
V_{SYNC} = 3.3V

10µs/DIV

3437 G24

Step Response

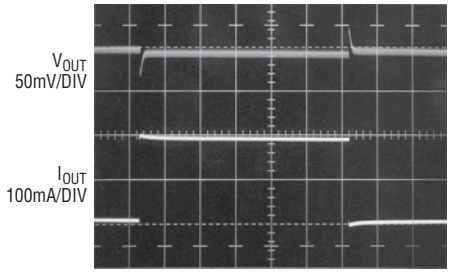


1ms/DIV

LOAD STEP 0mA TO 200mA

3437 G25

Step Response



1ms/DIV

LOAD STEP 100mA TO 300mA

3437 G26

PIN FUNCTIONS (DD/FE)

SW (Pin 1/Pin 2): The SW pin is the emitter of the on-chip power NPN switch. This pin is driven up to the input pin voltage during switch on time. Inductor current drives the SW pin negative during switch off time. Negative voltage is clamped with an external schottky catch diode to prevent excessive negative voltages.

NC (Pins 1, 3, 5, 7, 13, 16)(FE Package ONLY): No Connection. The NC pins are electrically isolated from the LT3437. The NC pins may be connected to PCB traces to aid PCB layout.

V_{IN} (Pin 2/Pin 4): This is the collector of the on-chip power NPN switch. V_{IN} powers the internal control circuitry when a voltage on the BIAS pin is not present. High di/dt edges occur on this pin during switch turn on and off. Keep the path short from the V_{IN} pin through the input bypass capacitor, through the catch diode back to SW. All trace inductance on this path will create a voltage spike at switch off, adding to the V_{CE} voltage across the internal NPN.

BOOST (Pin 3/Pin 6): The BOOST pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch. Without this added voltage, the typical switch voltage loss would be about 1.5V. The additional BOOST voltage allows the switch to saturate and its voltage loss approximates that of a 0.8Ω FET structure.

GND (Pins 4, 11/Pins 8, 17): The GND pin connection acts as the reference for the regulated output, so load regulation will suffer if the "ground" end of the load is not at the same voltage as the GND pin of the IC. This condition will occur when load current or other currents flow through metal paths between the GND pin and the load ground. Keep the path between the GND pin and the load ground short and use a ground plane when possible. The GND pin also acts as a heat sink and should be soldered (along with the exposed leadframe) to the copper ground plane to reduce thermal resistance (see Applications Information).

C_{SS} (Pin 5/Pin 9): A capacitor from the C_{SS} pin to the regulated output voltage determines the output voltage ramp rate during start-up. When the current through the C_{SS} capacitor exceeds the C_{SS} threshold (I_{CSS}), the voltage ramp of the output is limited. The C_{SS} threshold is proportional to the FB voltage (see Typical Performance Characteristics) and is defeated for FB voltage greater than 0.9V (typical). See Soft-Start section in Applications Information for details.

PIN FUNCTIONS (DD/FE)

BIAS (Pin 6/Pin 10): The BIAS pin is used to improve efficiency when operating at higher input voltages and light load current. Connecting this pin to the regulated output voltage forces most of the internal circuitry to draw its operating current from the output voltage rather than the input supply. This architecture increases efficiency especially when the input voltage is much higher than the output. Minimum output voltage setting for this mode of operation is typically 2.7V.

V_C (Pin 7/Pin 11): The V_C pin is the output of the error amplifier and the input of the peak switch current comparator. It is normally used for frequency compensation, but can also serve as a current clamp or control loop override. V_C sits at about 0.45V for light loads and 1.5V at maximum load. During the sleep portion of Burst Mode operation, the V_C pin is held at a voltage slightly below the burst threshold for better transient response. Driving the V_C pin to ground will disable switching and place the IC into sleep mode.

FB (Pin 8/Pin 12): The feedback pin is used to determine the output voltage using an external voltage divider from the output that generates 1.25V at the FB pin. When the FB pin drops below 0.9V, switching frequency is reduced, the SYNC function is disabled and output ramp rate control is enabled via the C_{SS} pin. See the Feedback section in Applications Information for details.

SYNC (Pin 9/Pin 14): The SYNC pin is used to synchronize the internal oscillator to an external signal. It is directly logic compatible and can be driven with any signal between 25% and 75% duty cycle. The synchronizing range is equal to maximum initial operating frequency up to 700kHz. When the voltage on the FB pin is below 0.9V the SYNC function is disabled. When a synchronization signal or logic-level high is present at the SYNC pin, Burst Mode operation is disabled. See the synchronizing section in Applications Information for details.

$\overline{\text{SHDN}}$ (Pin 10/Pin 15): The $\overline{\text{SHDN}}$ pin is used to turn off the regulator and to reduce input current to less than 1µA. The $\overline{\text{SHDN}}$ pin requires a voltage above 1.3V with a typical source current of 5µA to take the IC out of the shutdown state.

Exposed Pad (Pin 11/Pin 17): Ground. Must be soldered to the PCB.

BLOCK DIAGRAM

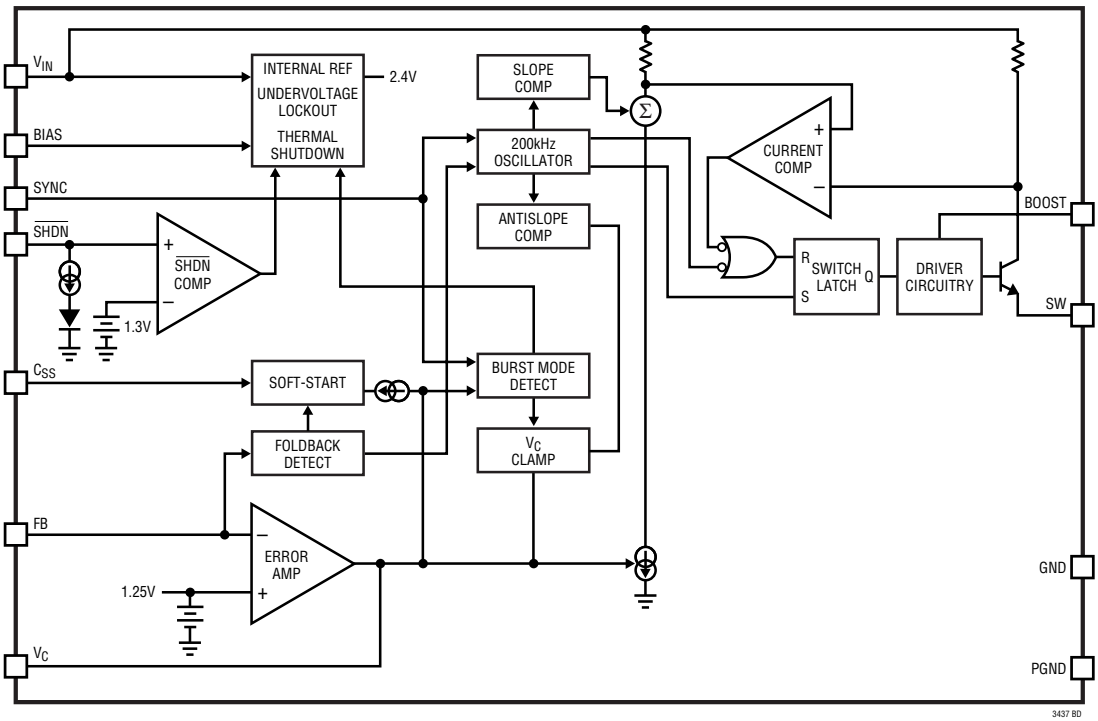


Figure 1. LT3437 Block Diagram

The LT3437 is a constant frequency, current mode buck converter. This means that there is an internal clock and two feedback loops that control the duty cycle of the power switch. In addition to the normal error amplifier, there is a current sense amplifier that monitors switch current on a cycle-by-cycle basis. A switch cycle starts with an oscillator pulse which sets the RS latch to turn the switch on. When switch current reaches a level set by the current comparator, the latch is reset and the switch turns off. Output voltage control is obtained by using the output of the error amplifier to set the switch current trip point. This technique means that the error amplifier commands current to be delivered to the output rather than voltage. A voltage fed system will have low phase shift up to the resonant frequency of the inductor and output capacitor, then an abrupt 180° shift will occur. The current fed system will have 90° phase shift at a much lower frequency, but will not have the additional 90° shift until well beyond the LC resonant frequency. This makes it much easier to frequency compensate the feedback loop and gives much quicker transient response and line rejection.

Most of the circuitry of the LT3437 operates from an internal 2.4V bias line. The bias regulator normally draws power from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 2.7V, bias power will be drawn from the external source (typically the regulated output voltage). This improves efficiency.

High switch efficiency is attained by using the BOOST pin to provide a voltage to the switch driver which is higher than the input voltage, allowing the switch to be saturated. This boosted voltage is generated with an external capacitor and diode.

To further optimize efficiency, the LT3437 automatically switches to Burst Mode operation in light load situations. In Burst Mode operation, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 45μA and bias input current to 110μA.

If lower output ripple is desired over light load efficiency, Burst Mode operation can be defeated by setting the SYNC pin voltage greater than 2V. A logic-level low on the $\overline{SHDN}$ pin disables the IC and reduces input supply current to less than 1μA. External synchronization can be implemented by driving the SYNC pin with logic-level inputs.

APPLICATIONS INFORMATION

FEEDBACK PIN FUNCTIONS

The feedback (FB) pin on the LT3437 is used to set output voltage and provide several overload protection features. The first part of this section deals with selecting resistors to set output voltage, and the remaining part talks about frequency foldback and soft-start features. Please read both parts before committing to a final design.

Referring to Figure 2, the output voltage is determined by a voltage divider from V_{OUT} to ground which generates 1.25V at the FB pin. Since the output divider is a load on the output, care must be taken when choosing the resistor divider values. For light load applications the resistor values should be as large as possible to achieve peak efficiency in Burst Mode operation. Extremely large values for resistor R1 will cause an output voltage error due to the 50nA FB pin input current. The suggested value for the output divider resistor (see Figure 2) from FB to ground (R2) is 100k or less. A formula for R1 is shown below. A table of standard 1% values is shown in Table 1 for common output voltages.

$$R1 = R2 \bullet \frac{V_{OUT} - 1.25}{1.25 + R2 \bullet 50nA}$$

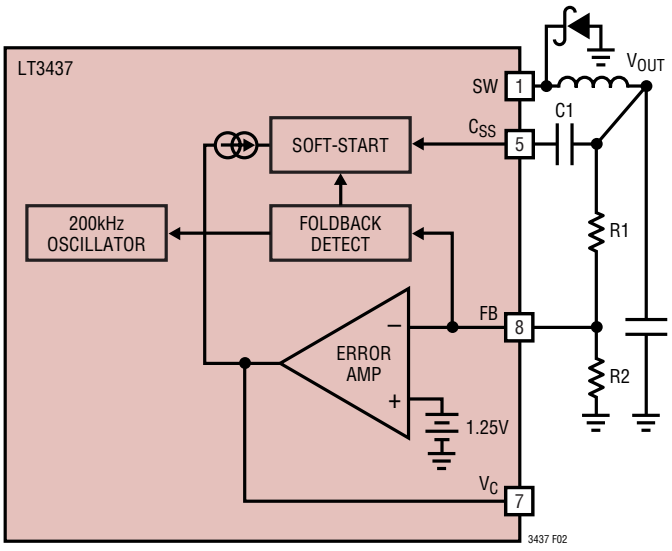


Figure 2. Feedback Network

Table 1

OUTPUT VOLTAGE (V)	R2 (kΩ, 1%)	R1 NEAREST (1%) (kΩ)	OUTPUT ERROR (%)
2.5	100	100	0
3	100	140	0
3.3	100	165	0.38
5	100	300	0
6	100	383	0.63
8	100	536	–0.63
10	100	698	–0.25
12	100	866	0.63

More Than Just Voltage Feedback

The FB pin is used for more than just output voltage sensing. It also reduces switching frequency and controls the soft-start voltage ramp rate when output voltage is below the regulated level (see the Frequency Foldback and Soft-Start Current graphs in Typical Performance Characteristics).

Frequency foldback is done to control power dissipation in both the IC and in the external diode and inductor during short-circuit conditions. A shorted output requires the switching regulator to operate at very low duty cycles. As a result, the average current through the diode and inductor is equal to the short-circuit current limit of the switch (typically 500mA for the LT3437). Minimum switch on time limitations would prevent the switcher from attaining a sufficiently low duty cycle if switching frequency were maintained at 200kHz, so frequency is reduced by about 10:1 when the FB pin voltage drops below 0.4V (see Frequency Foldback graph). As the feedback voltage rises, the switching frequency increases to 200kHz with 0.95V on the FB pin. During frequency foldback, external synchronization is disabled to prevent interference with foldback operation. Frequency foldback does not affect operation during normal load conditions.

In addition to lowering switching frequency, the soft-start ramp rate is also affected by the feedback voltage. Large capacitive loads or high input voltages can cause a

APPLICATIONS INFORMATION

high input current surge during start-up. The soft-start function reduces input current surge by regulating switch current via the V_C pin to maintain a constant voltage ramp rate (dV/dt) at the output. A capacitor (C1 in Figure 2) from the C_{SS} pin to the output determines the maximum output dV/dt. When the feedback voltage is below 0.4V, the V_C pin will rise, resulting in an increase in switch current and output voltage. If the dV/dt of the output causes the current through the C_{SS} capacitor to exceed I_{CSS}, the V_C voltage is reduced resulting in a constant dV/dt at the output. As the feedback voltage increases, I_{CSS} increases, resulting in an increased dV/dt until the soft-start function is defeated with 0.9V present at the FB pin. The soft-start function does not affect operation during normal load conditions. However, if a momentary short (brown out condition) is present at the output which causes the FB voltage to drop below 0.9V, the soft-start circuitry will become active.

INPUT CAPACITOR

Step-down regulators draw current from the input supply in pulses. The rise and fall times of these pulses are very fast. The input capacitor is required to reduce the voltage ripple this causes at the input of LT3437 and force the switching current into a tight local loop, thereby minimizing EMI. The RMS ripple current can be calculated from:

$$I_{RIPPLE(RMS)} = \frac{I_{OUT}}{V_{IN}} \sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}$$

Ceramic capacitors are ideal for input bypassing. At 200kHz switching frequency input capacitor values in the range of 2.2µF to 10µF are suitable for most applications. If operation is required close to the minimum input required by the LT3437, a larger value may be required. This is to prevent excessive ripple causing dips below the minimum operating voltage resulting in erratic operation.

Input voltage transients caused by input voltage steps, or by hot plugging the LT3437 to a pre-powered source such as a wall adapter, can exceed maximum V_{IN} ratings. The sudden application of input voltage will cause a large surge of current in the input leads that will store energy in the parasitic inductance of the leads. This energy will cause the input voltage to swing above the DC level of input power source and it may exceed the maximum voltage rating of the input capacitor and LT3437. All input voltage transient sequences should be observed at the V_{IN} pin of the LT3437 to ensure that absolute maximum voltage ratings are not violated.

The easiest way to suppress input voltage transients is to add a small aluminum electrolytic capacitor in parallel with the low ESR input capacitor. The selected capacitor needs to have the right amount of ESR to critically damp the resonant circuit formed by the input lead inductance and the input capacitor. The typical values of ESR will fall in the range of 0.5Ω to 2Ω and capacitance will fall in the range of 5µF to 50µF.

If tantalum capacitors are used, values in the 22µF to 470µF range are generally needed to minimize ESR and meet ripple current and surge ratings. Care should be taken to ensure the ripple and surge ratings are not exceeded. The AVX TPS and Kemet T495 series are surge rated. AVX recommends derating capacitor operating voltage by 2:1 for high surge applications.

OUTPUT CAPACITOR

The output capacitor is normally chosen by its effective series resistance (ESR) because this is what determines output ripple voltage. To get low ESR takes volume, so physically smaller capacitors have higher ESR. The ESR range for typical LT3437 applications is 0.05Ω to 0.2Ω. A typical output capacitor is an AVX type TPS, 100µF at 10V, with a guaranteed ESR less than 0.1Ω. This is a “D” size surface mount solid tantalum capacitor. TPS capacitors are specially constructed and tested for low ESR, so they give the lowest ESR for a given volume. The value in microfarads is not particularly critical, and values from 22µF to greater than 500µF work well, but you cannot cheat Mother Nature on ESR. If you find a tiny 22µF solid tantalum capacitor, it will have high ESR and output ripple

APPLICATIONS INFORMATION

voltage could be unacceptable. Table 2 shows some typical solid tantalum surface mount capacitors.

Table 2. Surface Mount Solid Tantalum Capacitor ESR and Ripple Current

E CASE SIZE	ESR MAX (Ω)	RIPPLE CURRENT (A)
AVX TPS	0.1 to 0.3	0.7 to 1.1
D CASE SIZE		
AVX TPS	0.1 to 0.3	0.7 to 1.1
C CASE SIZE		
AVX TPS	0.2	0.5

Many engineers have heard that solid tantalum capacitors are prone to failure if they undergo high surge currents. This is historically true, and type TPS capacitors are specially tested for surge capability, but surge ruggedness is not a critical issue with the output capacitor. Solid tantalum capacitors fail during very high turn-on surges which do not occur at the output of regulators. High discharge surges, such as when the regulator output is dead shorted, do not harm the capacitors.

Unlike the input capacitor RMS, ripple current in the output capacitor is normally low enough that ripple current rating is not an issue. The current waveform is triangular with a typical value of $30mA_{RMS}$. The formula to calculate this is:

Output capacitor ripple current (RMS)

$$I_{RIPPLE(RMS)} = \frac{0.29(V_{OUT})(V_{IN} - V_{OUT})}{(L)(f)(V_{IN})} = \frac{I_{P-P}}{\sqrt{12}}$$

CERAMIC CAPACITORS

Higher value, lower cost ceramic capacitors are now becoming available. They are generally chosen for their good high frequency operation, small size and very low ESR (effective series resistance). Low ESR reduces output ripple voltage but also removes a useful zero in the loop frequency response, common to tantalum capacitors. To compensate for this, a resistor R_C can be placed in series with the V_C compensation capacitor C_C (Figure 10). Care must be taken, however, since this resistor sets the high frequency gain of the error amplifier, including the gain at the switching frequency. If the gain of the error amplifier is high enough at the switching frequency, output ripple voltage (although smaller for a ceramic output capacitor) may still affect the proper operation of the regulator. A filter capacitor C_F in parallel with the R_C/C_C network, along with a small feedforward capacitor C_{FB}, is suggested to control possible ripple at the V_C pin. The LT3437 can be stabilized using a 100µF ceramic output capacitor and V_C component values of C_C = 1500pF, R_C = 25k, C_F = 330pF and C_{FB} =27pF.

OUTPUT RIPPLE VOLTAGE

Figure 3 shows a typical output ripple voltage waveform for the LT3437. Ripple voltage is determined by the impedance of the output capacitor and ripple current through the inductor. Peak-to-peak ripple current through the inductor into the output capacitor is:

$$I_{P-P} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{(V_{IN})(L)(f)}$$

For high frequency switchers the ripple current slew rate is also relevant and can be calculated from:

$$\frac{di}{dt} = \frac{V_{IN}}{L}$$

Peak-to-peak output ripple voltage is the sum of a triwave created by peak-to-peak ripple current times ESR and a square wave created by parasitic inductance (ESL) and ripple current slew rate. Capacitive reactance is assumed to be small compared to ESR or ESL.

$$V_{RIPPLE} = (I_{P-P})(ESR) + (ESL)\frac{di}{dt}$$

Example: with V_{IN} = 12V, V_{OUT} = 3.3V, L = 100µH, ESR = 0.075Ω, ESL = 10nH:

$$I_{P-P} = \frac{(3.3)(12 - 3.3)}{(12)(100e-6)(200e3)} = 0.120A$$

$$\frac{di}{dt} = \frac{12}{100e-6} = 0.12e6$$

V_{RIPPLE} = (0.120A)(0.075) + (10e – 9)(0.12e6)
= 0.009 + 0.0012 = $10.2mV_{P-P}$

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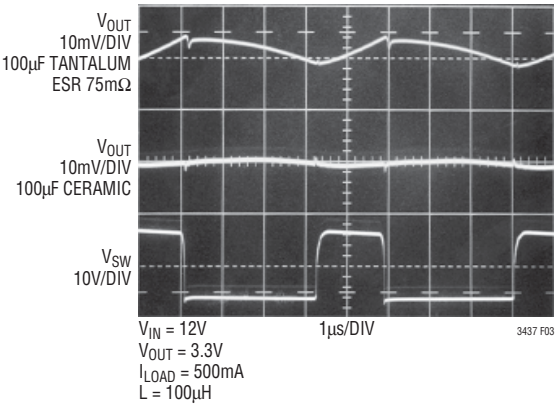

Figure 3. LT3437 Ripple Voltage Waveform

MAXIMUM OUTPUT LOAD CURRENT

Maximum load current for a buck converter is limited by the maximum switch current rating (I_{PK}). The current rating for the LT3437 is 500mA. Unlike most current mode converters, the LT3437 maximum switch current limit does not fall off at high duty cycles. Most current mode converters suffer a drop off of peak switch current for duty cycles above 50%. This is due to the effects of slope compensation required to prevent subharmonic oscillations in current mode converters. (For detailed analysis, see Application Note 19.)

The LT3437 is able to maintain peak switch current limit over the full duty cycle range by using patented circuitry to cancel the effects of slope compensation on peak switch current without affecting the frequency compensation it provides.

Maximum load current would be equal to maximum switch current for an infinitely large inductor, but with finite inductor size, maximum load current is reduced by one-half peak-to-peak inductor current. The following formula assumes continuous mode operation, implying that the term on the right ($I_{P-P}/2$) is less than I_{OUT}.

$$I_{OUT(MAX)} = I_{PK} - \frac{(V_{OUT})(V_{IN} - V_{OUT})}{2(L)(f)(V_{IN})} = I_{PK} - \frac{I_{P-P}}{2}$$

Discontinuous operation occurs when:

$$I_{OUT(DIS)} \leq \frac{V_{OUT}(V_{IN} - V_{OUT})}{2(L)(f)(V_{IN})}$$

For V_{OUT} = 5V, V_{IN} = 8V and L = 68µH:

$$I_{OUT(MAX)} = 0.5 - \frac{(5)(8-5)}{2(68e-6)(200e3)(8)}$$
$$= 0.5 - 0.069 = 0.431A$$

Note that there is less load current available at the higher input voltage because inductor ripple current increases. At V_{IN} = 15V, duty cycle is 33% and for the same set of conditions:

$$I_{OUT(MAX)} = 0.5 - \frac{(5)(15-5)}{2(68e-6)(200e3)(15)}$$
$$= 0.5 - 0.121 = 0.379A$$

To calculate actual peak switch current in continuous mode with a given set of conditions, use:

$$I_{SW(PK)} = I_{OUT} + \frac{V_{OUT}(V_{IN} - V_{OUT})}{2(L)(f)(V_{IN})}$$

If a small inductor is chosen which results in discontinuous mode operation over the entire load range, the maximum load current is equal to:

$$I_{OUT(MAX)} = \frac{I_{PK}^2 2(f)(L)(V_{IN})}{2(V_{OUT})(V_{IN} - V_{OUT})}$$

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CHOOSING THE INDUCTOR

For most applications the output inductor will fall in the range of 68µH to 220µH. Lower values are chosen to reduce physical size of the inductor. Higher values allow more output current because they reduce peak current seen by the LT3437 switch, which has a 0.5A limit. Higher values also reduce output ripple voltage and reduce core loss.

When choosing an inductor you might have to consider maximum load current, core and copper losses, allowable component height, output voltage ripple, EMI, fault current in the inductor, saturation and of course cost. The following procedure is suggested as a way of handling these somewhat complicated and conflicting requirements.

1. Choose a value in microhenries such that the maximum load current plus half of the inductor ripple current is less than the minimum peak switch current (I_{PK}). Choosing a small inductor with lighter loads may result in discontinuous mode of operation, but the LT3437 is designed to work well in either mode.

   Assume that the average inductor current is equal to load current and decide whether or not the inductor must withstand continuous fault conditions. If maximum load current is 0.25A, for instance, a 0.25A inductor may not survive a continuous minimum peak switch current overload condition.

   For applications with a duty cycle above 50%, the inductor value should be chosen to obtain an inductor ripple current of less than 40% of the peak switch current.

2. Calculate peak inductor current at full load current to ensure that the inductor will not saturate. Peak current can be significantly higher than output current, especially with smaller inductors and lighter loads, so do not omit this step. Powdered iron cores are forgiving because they saturate softly, whereas ferrite cores saturate abruptly. Other core materials fall somewhere in between. The following formula assumes continuous mode of operation, but it errs only slightly on the high side for discontinuous mode, so it can be used for all conditions.

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{2\left(f\right)\left(L\right)\left(V_{IN}\right)}$$

   V_{IN} = maximum input voltage

   f = switching frequency, 200kHz

3. Decide if the design can tolerate an “open” core geometry like a rod or barrel, which has high magnetic field radiation, or whether it needs a closed core like a toroid, to prevent EMI problems. This is a tough decision because the rods or barrels are temptingly cheap and small, and there are no helpful guidelines to calculate when the magnetic field radiation will be a problem.

4. After making an initial choice, consider the secondary things like output voltage ripple, second sourcing, etc. Use the experts in Linear Technology’s applications department if you feel uncertain about the final choice. They have experience with a wide range of inductor types and can tell you about the latest developments in low profile, surface mounting, etc.

Table 3. Inductor Selection Criteria

VENDOR/ PART NO.	VALUE (µH)	$I_{DC(MAX)}$ (mA)	DCR (Ohms)	HEIGHT (mm)
UP1B-101	100	530	1.11	5.0
UP1B-151	150	460	1.61	5.0
UP2B-221	220	380	1.96	5.0
D01605T-473MX	47	450	1.1	1.8
D01605T-104MX	100	300	2.3	1.8
D03308P-154	150	600	0.94	3.0
D03308P-224	220	500	1.6	3.0
CDRH4D28-470	47	480	0.387	3.0
CDRH4D28-101	100	290	1.02	3.0
CDRH5D28-101	100	420	0.520	3.0

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Short-Circuit Considerations

The LT3437 is a current mode controller. It uses the V_C node voltage as an input to a current comparator which turns off the output switch on a cycle-by-cycle basis as this peak current is reached. The internal clamp on the V_C node, nominally 1.5V, then acts as an output switch peak current limit. This action becomes the switch current limit specification. The maximum available output power is then determined by the switch current limit.

A potential controllability problem could occur under short-circuit conditions. If the power supply output is short circuited, the feedback amplifier responds to the low output voltage by raising the control voltage, V_C, to its peak current limit value. Ideally, the output switch would be turned on, and then turned off as its current exceeded the value indicated by V_C. However, there is finite response time involved in both the current comparator and turn-off of the output switch. This results in a minimum on time $t_{ON(MIN)}$. When combined with the large ratio of V_{IN} to $(V_F + I \bullet R)$, the diode forward voltage plus inductor I • R voltage drop, the potential exists for a loss of control. Expressed mathematically the requirement to maintain control is:

$$f \bullet t_{ON} \leq \frac{V_F + I \bullet R}{V_{IN}}$$

where:

f = switching frequency

t_{ON} = switch on time

V_F = diode forward voltage

V_{IN} = Input voltage

I • R = inductor I • R voltage drop

If this condition is not observed, the current will not be limited at I_{PK} but will cycle-by-cycle ratchet up to some higher value. Using the nominal LT3437 clock frequency of 200kHz, a V_{IN} of 40V and a $(V_F + I \bullet R)$ of say 0.7V, the maximum t_{ON} to maintain control would be approximately 90ns, an unacceptably short time.

The solution to this dilemma is to slow down the oscillator to allow the current in the inductor to drop to a sufficiently low value such that the current does not continue to ratchet higher. When the FB pin voltage is abnormally low, thereby indicating some sort of short-circuit condition, the oscillator frequency will be reduced. Oscillator frequency is reduced by a factor of 10 when the FB pin voltage is below 0.4V and increases linearly to its typical value of 200kHz at a FB voltage of 0.95V (see Typical Performance Characteristics). These oscillator frequency reductions during short-circuit conditions allow the LT3437 to maintain current control

SOFT-START

For applications where $[V_{IN}/(V_{OUT} + V_F)] > 10$ or large input surge currents cannot be tolerated, the LT3437 soft-start feature should be used to control the output capacitor charge rate during start-up, or during recovery from an output short circuit, thereby adding additional control over peak inductor current. The soft-start function limits the switch current via the V_C pin to maintain a constant voltage ramp rate (dV/dt) at the output capacitor. A capacitor (C1 in Figure 2) from the C_{SS} pin to the regulated output voltage determines the output voltage ramp rate. When the current through the C_{SS} capacitor exceeds the C_{SS} threshold (I_{CSS}), the voltage ramp of the output capacitor is limited by reducing the V_C pin voltage. The C_{SS} threshold is proportional to the FB voltage (see Typical Performance Characteristics) and is defeated for FB voltages greater than 0.9V (typical). The output dV/dt can be approximated by:

$$\frac{dV}{dt} = \frac{I_{CSS}}{C_{SS}}$$

but actual values will vary due to start-up load conditions, compensation values and output capacitor selection.

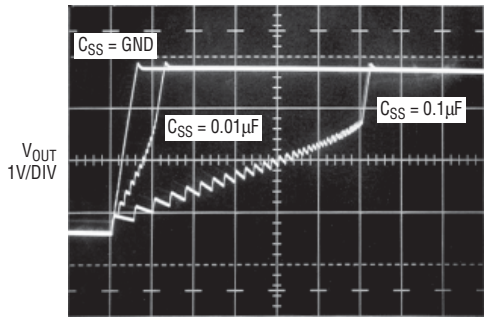

Figure 4. V_{OUT} dV/dt

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Burst Mode OPERATION

To enhance efficiency at light loads, the LT3437 automatically switches to Burst Mode operation which keeps the output capacitor charged to the proper voltage while minimizing the input quiescent current. During Burst Mode operation, the LT3437 delivers short bursts of current to the output capacitor followed by sleep periods where the output power is delivered to the load by the output capacitor. In addition, V_{IN} and BIAS quiescent currents are reduced to typically 45µA and 110µA, respectively, during the sleep time. As the load current decreases towards a no load condition, the percentage of time that the LT3437 operates in sleep mode increases and the average input current is greatly reduced, resulting in higher efficiency.

The minimum average input current depends on the V_{IN} to V_{OUT} ratio, V_C frequency compensation, feedback divider network and Schottky diode leakage. It can be approximated by the following equation:

$$I_{IN(AVG)} \cong I_{VINS} + I_{\overline{SHDN}} + \left(\frac{V_{OUT}}{V_{IN}}\right)\frac{\left(I_{BIASS} + I_{FB} + I_S\right)}{\left(\eta\right)}$$

where

I_{VINS} = input pin current in sleep mode

V_{OUT} = output voltage

V_{IN} = input voltage

I_{BIASS} = BIAS pin current in sleep mode

I_{FB} = feedback network current

I_S = catch diode reverse leakage at V_{OUT}

η = low current efficiency (non Burst Mode operation)

Example: For V_{OUT} = 3.3V, V_{IN} = 12V

$$I_{IN(AVG)} \cong 45\mu A + 5\mu A + \left(\frac{3.3}{12}\right)\frac{\left(110\mu A + 12.5\mu A + 0.5\mu A\right)}{\left(0.8\right)}$$

$$= 45\mu A + 5\mu A + 42\mu A = 92\mu A$$

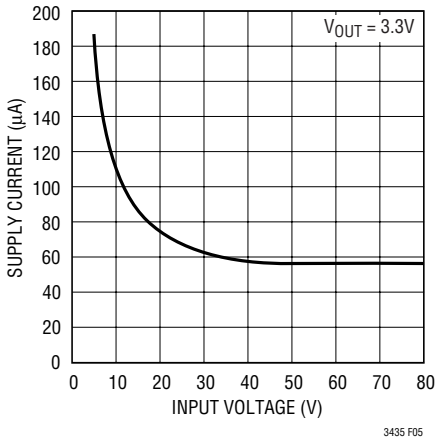

Figure 5. I_Q vs V_{IN}

During the sleep portion of the Burst Mode cycle, the V_C pin voltage is held just below the level needed for normal operation to improve transient response. See the Typical Performance Characteristics section for burst and transient response waveforms.

If Burst Mode operation is undesirable, it can be defeated by placing 2V or greater on the SYNC pin. When Burst Mode operation is defeated, output ripple at light loads will be reduced at the expense of light load efficiency.

CATCH DIODE

The catch diode carries load current during the SW off time. The average diode current is therefore dependent on the switch duty cycle. At high input to output voltage ratios, the diode conducts most of the time. As the ratio approaches unity, the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is short circuited. Under this condition, the diode must safely handle I_{PEAK} at maximum duty cycle.

To maximize high and low load current efficiency, a fast switching diode with low forward drop and low reverse leakage should be used. Low reverse leakage is critical to maximize low current efficiency since its value over temperature can potentially exceed the magnitude of the LT3437 supply current. Low forward drop is critical for high current efficiency since the loss is proportional to forward drop.

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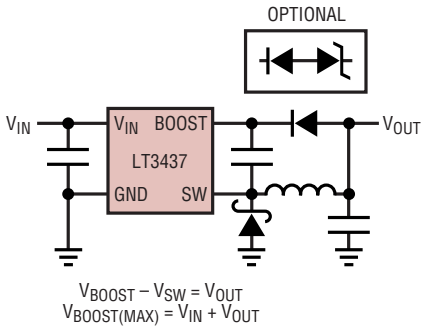
These requirements result in the use of a Schottky type diode. DC switching losses are minimized due to its low forward voltage drop, and AC behavior is benign due to its lack of a significant reverse recovery time. Schottky diodes are generally available with reverse voltage ratings of 60V, and even 100V, and are price competitive with other types.

The use of so-called "ultrafast" recovery diodes is generally not recommended. When operating in continuous mode, the reverse recovery time exhibited by "ultrafast" diodes will result in a slingshot type effect. The power internal switch will ramp up V_{IN} current into the diode in an attempt to get it to recover. When the diode has finally turned off, some tens of nanoseconds later, the V_{SW} node voltage ramps up at an extremely high dV/dt, perhaps 5V to even 10V/ns! With real world lead inductances, the V_{SW} node can easily overshoot the V_{IN} rail. This can result in poor RFI behavior, and if the overshoot is severe enough, damage the IC itself.

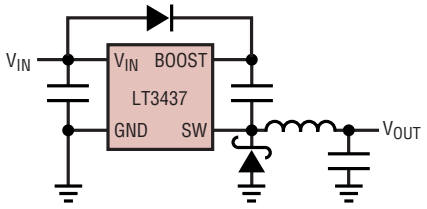
BOOST PIN

For most applications, the boost components are a 0.1µF capacitor and a BAS21 diode. The anode is typically connected to the regulated output voltage, to generate a voltage approximately V_{OUT} above V_{IN} to drive the output stage (Figure 6a). However, the output stage discharges the boost capacitor during the on time of the switch. The output driver requires at least 2.5V of headroom throughout this period to keep the switch fully saturated. If the output voltage is less than 3.3V, it is recommended that an alternate boost supply is used. The boost diode can be connected to the input (Figure 6b), but care must be taken to prevent the boost voltage (V_{BOOST} = V_{IN} • 2) from exceeding the BOOST pin absolute maximum rating. The additional voltage across the switch driver also increases power loss and reduces efficiency. If available, an independent supply can be used to generate the required BOOST voltage (Figure 6c). Tying BOOST to V_{IN} or an independent supply may reduce efficiency, but it will reduce the minimum V_{IN} required to start-up with light loads. If the generated BOOST voltage dissipates too much power at maximum load, the BOOST voltage the LT3437 sees can be reduced by placing a Zener diode in series with the BOOST diode (Figure 6a option).



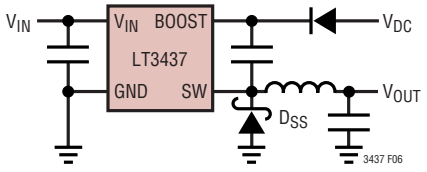
$V_{BOOST} - V_{SW} = V_{OUT}$
$V_{BOOST(MAX)} = V_{IN} + V_{OUT}$

(6a)



$V_{BOOST} - V_{SW} = V_{IN}$
$V_{BOOST(MAX)} = 2V_{IN}$

(6b)



$V_{BOOST} - V_{SW} = V_{DC}$
$V_{BOOST(MAX)} = V_{DC} + V_{IN}$

(6c)

Figure 6. BOOST Pin Configurations

A 0.1µF boost capacitor is recommended for most applications. Almost any type of film or ceramic capacitor is suitable, but the ESR should be <1Ω to ensure it can be fully recharged during the off time of the switch. The capacitor value is derived from worst-case conditions of 4700ns on time, 11mA boost current and 0.7V discharge ripple. The boost capacitor value could be reduced under less demanding conditions, but this will not improve circuit operation or efficiency. Under low input voltage and low load conditions, a higher value capacitor will reduce discharge ripple and improve start-up operation.

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SHUTDOWN FUNCTION AND UNDERVOLTAGE LOCKOUT

The $\overline{SHDN}$ pin on the LT3437 controls the operation of the IC. When the voltage on the $\overline{SHDN}$ pin is below the 1.3V shutdown threshold, the LT3437 is placed in a "zero" supply current state. Driving the $\overline{SHDN}$ pin above the shutdown threshold enables normal operation. The $\overline{SHDN}$ pin has an internal sink current with a typical value of 5µA.

In addition to the shutdown feature, the LT3437 has an undervoltage lockout function. When the input voltage is below 2.5V, switching will be disabled. The undervoltage lockout threshold doesn't have any hysteresis and is mainly used to insure that all internal voltages are at the correct level before switching is enabled. If an undervoltage lockout function with hysteresis is needed to limit input current at low V_{IN} to V_{OUT} ratios, refer to Figure 7 and the following:

$$V_{UVLO} = R1\left(\frac{V_{SHDN}}{R3} + \frac{V_{SHDN}}{R2} + I_{SHDN}\right) + V_{SHDN}$$

$$V_{HYST} = \frac{V_{OUT}(R1)}{R3}$$

R1 should be chosen to minimize quiescent current during normal operation by the following equation:

$$R1 = \frac{V_{IN} - 2V}{(1.5)\left(I_{\overline{SHDN}(TYP)}\right)}$$

Example:

$$R1 = \frac{12 - 2}{1.5(5\mu A)} = 1.3M\Omega$$

$$R3 = \frac{5(1.3M\Omega)}{1} = 6.5M\Omega \text{ (Nearest 1\% } 6.49M\Omega)$$

$$R2 = \frac{1.3}{\frac{7 - 1.3}{1.3M\Omega} - 1\mu A - \frac{1.3}{6.49M\Omega}}$$

$$= 408k \text{ (Nearest 1\% } 412k)$$

See the Typical Performance Characteristics section for graphs of $\overline{SHDN}$ and V_{IN} currents verses input voltage.

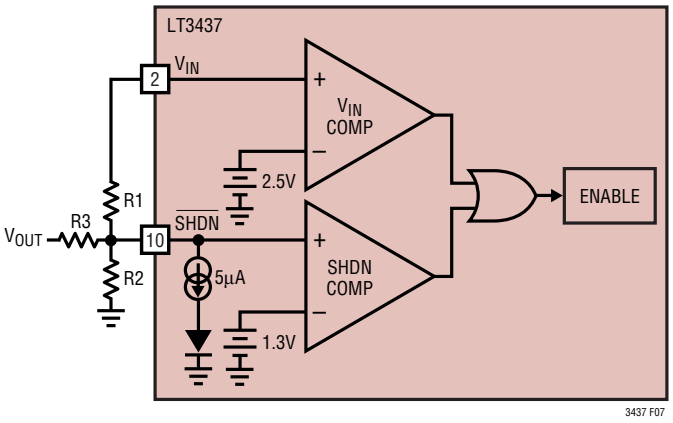

Figure 7. Undervoltage Lockout

SYNCHRONIZING

Oscillator synchronization to an external input is achieved by connecting a TTL logic-compatible square wave with a duty cycle between 25% and 75% to the LT3437 SYNC pin. The synchronizing range is equal to initial operating frequency up to 700kHz. This means that minimum practical sync frequency is equal to the worst-case high self-oscillating frequency (240kHz), not the typical operating frequency of 200kHz. Caution should be used when synchronizing above 300kHz, because at higher sync frequencies the amplitude of the internal slope compensation used to prevent subharmonic switching is reduced. This type of subharmonic switching only occurs at input voltages less than twice output voltage. Higher inductor values will tend to eliminate this problem. See Frequency Compensation section for a discussion of an entirely different cause of subharmonic switching before assuming that the cause is insufficient slope compensation. Application Note 19 has more details on the theory of slope compensation.

If the FB pin voltage is below 0.9V (power-up or output short-circuit conditions), the sync function is disabled. This allows the frequency foldback to operate to avoid hazardous conditions for the SW pin.

If a synchronization signal or logic-level above 2V is present at the SYNC pin, Burst Mode operation is disabled. Burst Mode operation can be enabled or disabled on the fly. If no synchronization or Burst Mode defeat is required, this pin should be connected to ground.

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LAYOUT CONSIDERATIONS

As with all high frequency switchers, when considering layout, care must be taken in order to achieve optimal electrical, thermal and noise performance. For maximum efficiency, switch rise and fall times are typically in the nanosecond range. To prevent noise both radiated and conducted, the high speed switching current path, shown in Figure 8, must be kept as short as possible. This is implemented in the suggested layouts of Figure 9. Shortening this path will also reduce the parasitic trace inductance of approximately 25nH/inch. At switch off, this parasitic inductance produces a flyback spike across the LT3437 switch. When operating at higher currents and input voltages, with poor layout, this spike can generate voltages across the LT3437 that may exceed its absolute maximum rating. A ground plane should always be used under the switcher circuitry to prevent interplane coupling and overall noise.

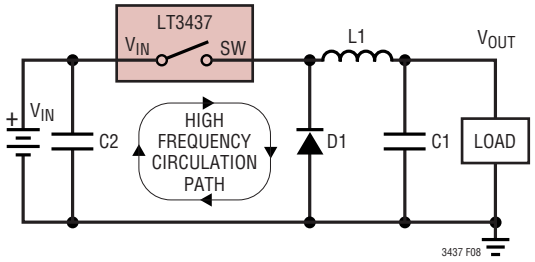
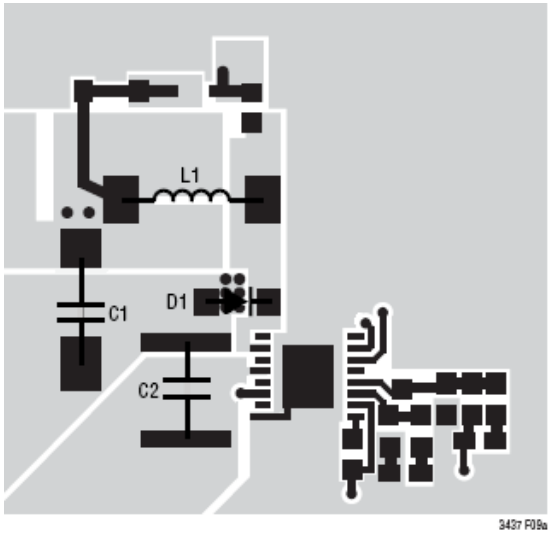


Figure 8. High Speed Switching Path

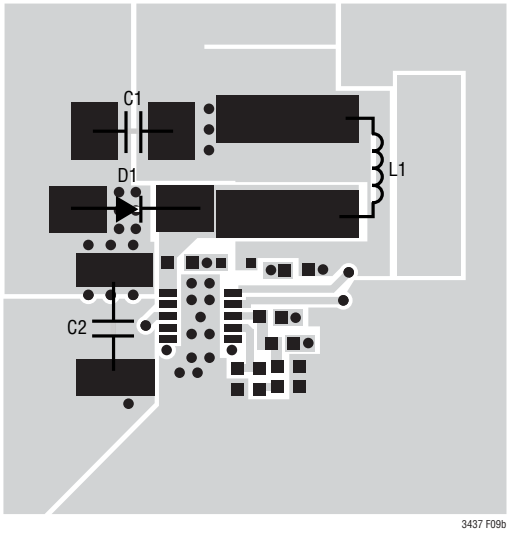
The V_C and FB components should be kept as far away as possible from the switch and boost nodes. The LT3437 pinout has been designed to aid in this. The ground for these components should be separated from the switch current path. Failure to do so will result in poor stability or subharmonic oscillation.

Board layout also has a significant effect on thermal resistance. Pin 4/Pin 8 and the exposed die pad, Pin 11/Pin 17, are connected by a continuous copper plate that runs under the LT3437 die. This is the best thermal path for heat out of the package. Reducing the thermal resistance from Pin 4 and the exposed pad onto the board will reduce die temperature and increase the power capability of the LT3437. This is achieved by providing as much copper area as possible around the exposed pad. Adding multiple solder filled feedthroughs, under and around this pad, to an internal ground plane will also help. Similar treatment to the catch diode and coil terminations will reduce any additional heating effects.

APPLICATIONS INFORMATION



FE Package Topside Metal



DD Package Topside Metal

Figure 9. Suggested Layouts

APPLICATIONS INFORMATION

THERMAL CALCULATIONS

Power dissipation in the LT3437 chip comes from four sources: switch DC loss, switch AC loss, boost circuit current, and input quiescent current. The following formulas show how to calculate each of these losses. These formulas assume continuous mode operation, and should not be used for calculating efficiency at light load currents.

Switch loss:

$$P_{SW} = \frac{R_{SW}\left(I_{OUT}\right)^2\left(V_{OUT}\right)}{V_{IN}} + t_{EFF}\left(1/2\right)\left(I_{OUT}\right)\left(V_{IN}\right)\left(f\right)$$

Boost current loss:

$$P_{BOOST} = \frac{\left(V_{OUT}\right)^2\left(I_{OUT}/30\right)}{V_{IN}}$$

Quiescent current loss:

$P_Q = V_{IN}$ (500µA) + V_{OUT} (800µA)

R_{SW} = switch resistance (≈1 when hot)

t_{EFF} = effective switch current/voltage overlap time

($t_r + t_f + t_{IR} + t_{IF}$)

$t_r = (V_{IN}/0.6)$ns

$t_f = (V_{IN}/2)$ns

$t_{IR} = t_{IF} = (I_{OUT}/0.05)$ns

f = switch frequency

Example: with V_{IN} = 40V, V_{OUT} = 5V and I_{OUT} = 250mA:

$$P_{SW} = \frac{(1)(0.25)^2(5)}{40} + (92)(1/2)(0.25)(40)(200e3)$$

$$0.008 + 0.092 = 0.1W$$

$$P_{BOOST} = \frac{(5)^2(0.25/30)}{40} = 0.005W$$

$$P_Q = 40(0.0005) + 5(0.0008) = 0.024W$$

Total power dissipation is:

P_{TOT} = 0.1 + 0.065 + 0.024 = 0.13W

Thermal resistance for the LT3437 package is influenced by the presence of internal or backside planes. With a full plane under the package, thermal resistance will be about 45°C for the FE and DD packages. No plane will increase resistance to about 150°C/W. To calculate die temperature, use the proper thermal resistance number for the desired package and add in worst-case ambient temperature:

$T_J = T_A + Q_{JA}$ (P_{TOT})

With the DD package (Q_{JA} = 45°C/W) at an ambient temperature of 70°C:

$T_J = 70 + 45(0.1) = 74.5°C$

HIGH TEMPERATURE OPERATION

Extreme care must be taken when designing LT3437 applications to operate at high ambient temperatures. The LT3437 is designed to work at elevated temperatures but erratic operation can occur due to external components. Each passive component should be checked for absolute value and voltage ratings to ensure loop stability at temperature. Boost and Catch diode leakages, as well as increased series resistance, will adversely affect efficiency and low quiescent current operation. Junction temperature increase in the diodes due to self heating (leakage) and power dissipation should be measured to ensure their maximum temperature specifications are not violated.

Input Voltage vs Operating Frequency Considerations

The absolute maximum input supply voltage for the LT3437 is specified at 80V. This is based solely on internal semiconductor junction breakdown effects. Due to internal power dissipation, the actual maximum V_{IN} achievable in a particular application may be less than this.

A detailed theoretical basis for estimating internal power loss is given in the section Thermal Considerations. Note that AC switching loss is proportional to both operating frequency and output current. The majority of AC switching loss is also proportional to the square of input voltage.

For example, while the combination of V_{IN} = 40V, V_{OUT} = 5V at 700mA and f_{OSC} = 200kHz may be easily achievable, simultaneously raising V_{IN} to 80V and f_{OSC} to 700kHz is not possible. Nevertheless, input voltage transients up to 80V can usually be accommodated, assuming the resulting

APPLICATIONS INFORMATION

increase in internal dissipation is of insufficient time duration to raise die temperature significantly.

A second consideration is controllability. A potential limitation occurs with a high step-down ratio of V_{IN} to V_{OUT}, as this requires a correspondingly narrow minimum switch on time. An approximate expression for this (assuming continuous mode operation) is given as follows:

$$t_{ON(MIN)} = (V_{OUT} + V_F)/V_{IN}(f_{OSC})$$

where:

V_{IN} = input voltage

V_{OUT} = output voltage

V_F = Schottky diode forward drop

f_{OSC} = switching frequency

A potential controllability problem arises if the LT3437 is called upon to produce an on time shorter than it is able to produce. Feedback loop action will lower, then reduce, the V_C control voltage to the point where some sort of cycle-skipping or Burst Mode behavior is exhibited.

In summary:

1. Be aware that the simultaneous requirements of high V_{IN}, high I_{OUT} and high f_{OSC} may not be achievable in practice due to internal dissipation. The Thermal Considerations section offers a basis to estimate internal power. In questionable cases, a prototype supply should be built and exercised to verify acceptable operation.
2. The simultaneous requirements of high V_{IN}, low V_{OUT} and high f_{OSC} can result in an unacceptably short minimum switch on time. Cycle skipping and/or Burst Mode behavior will result causing an increase in output voltage ripple while maintaining the correct output voltage.

FREQUENCY COMPENSATION

Before starting on the theoretical analysis of frequency response, the following should be remembered—the worse the board layout, the more difficult the circuit will be to stabilize. This is true of almost all high frequency analog circuits. Read the Layout Considerations section first. Common layout errors that appear as stability problems are distant placement of input decoupling capacitor and/or catch diode, and connecting the V_C compensation to a ground track carrying significant switch current. In addition, the theoretical analysis considers only first order non-ideal component behavior. For these reasons, it is important that a final stability check is made with production layout and components.

The LT3437 uses current mode control. This alleviates many of the phase shift problems associated with the inductor. The basic regulator loop is shown in Figure 10. The LT3437 can be considered as two g_m blocks, the error amplifier and the power stage.

Figure 11 shows the overall loop response. At the V_C pin, the frequency compensation components used are: R_C = 25k, C_C = 1500pF and C_F = 330pF. The output capacitor used is a 100µF, 10V tantalum capacitor with typical ESR of 100mΩ.

The ESR of the tantalum output capacitor provides a useful zero in the loop frequency response for maintaining stability. This ESR, however, contributes significantly to the ripple voltage at the output (see Output Ripple Voltage in the Applications Information section). It is possible to reduce capacitor size and output ripple voltage by replacing the tantalum output capacitor with a ceramic output capacitor because of its very low ESR. The zero provided by the tantalum output capacitor must now be reinserted back into the loop. Alternatively, there may be cases where, even with the tantalum output capacitor, an additional zero is required in the loop to increase phase margin for improved transient response.

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A zero can be added into the loop by placing a resistor (R_C) at the V_C pin in series with the compensation capacitor, C_C, or by placing a capacitor (C_{FB}) between the output and the FB pin.

When using R_C, the maximum value has two limitations. First, the combination of output capacitor ESR and R_C may stop the loop rolling off altogether. Second, if the loop gain is not rolled off sufficiently at the switching frequency, output ripple will perturb the V_C pin enough to cause unstable duty cycle switching, similar to subharmonic oscillations. If needed, an additional capacitor (C_F) can be added across the R_C/C_C network from the V_C pin to ground to further suppress V_C ripple voltage.

With a tantalum output capacitor, the LT3437 already includes a resistor (R_C) and filter capacitor (C_F) at the V_C pin (see Figures 10 and 11) to compensate the loop over the entire V_{IN} range (to allow for stable pulse skipping for high V_{IN}-to-V_{OUT} ratios ≥ 10). A ceramic output capacitor can still be used with a simple adjustment to the resistor R_C for stable operation (see Ceramic Capacitors section for stabilizing LT3430). If additional phase margin is required, a capacitor (C_{FB}) can be inserted between the output and FB pin, but care must be taken for high output voltage applications. Sudden shorts to the output can create unacceptably large negative transients on the FB pin.

For V_{IN}-to-V_{OUT} ratios < 10, higher loop bandwidths are possible by readjusting the frequency compensation components at the V_C pin.

When checking loop stability, the circuit should be operated over the application's full voltage, current and temperature range. Proper loop compensation may be obtained by empirical methods, as described in Application Notes 19 and 76.

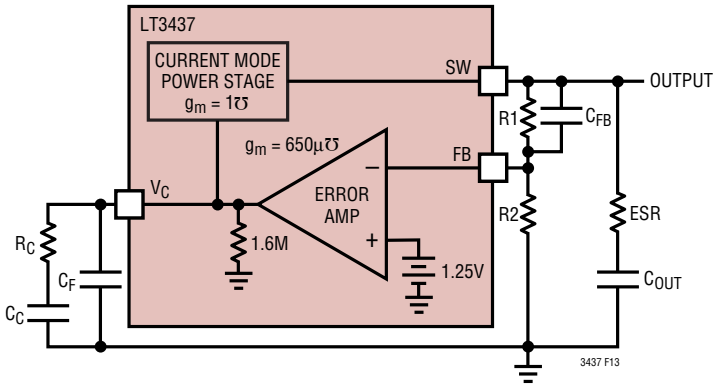


Figure 10. Model for Loop Response

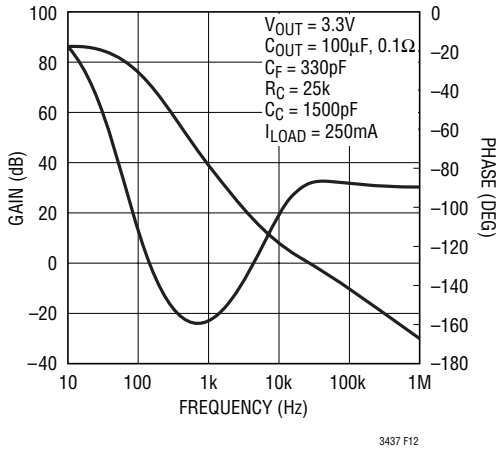
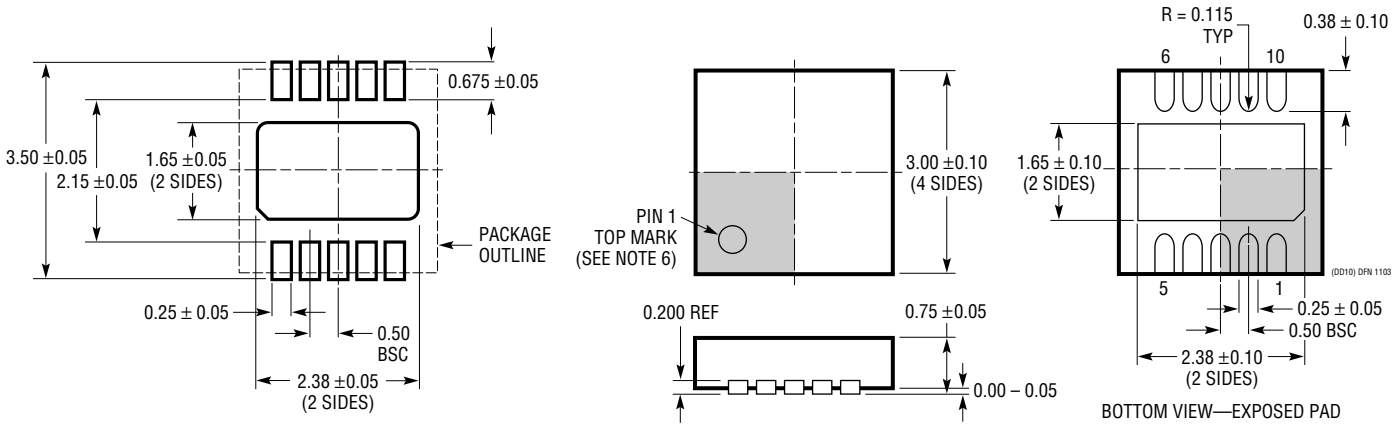


Figure 11. Overall Loop Response

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



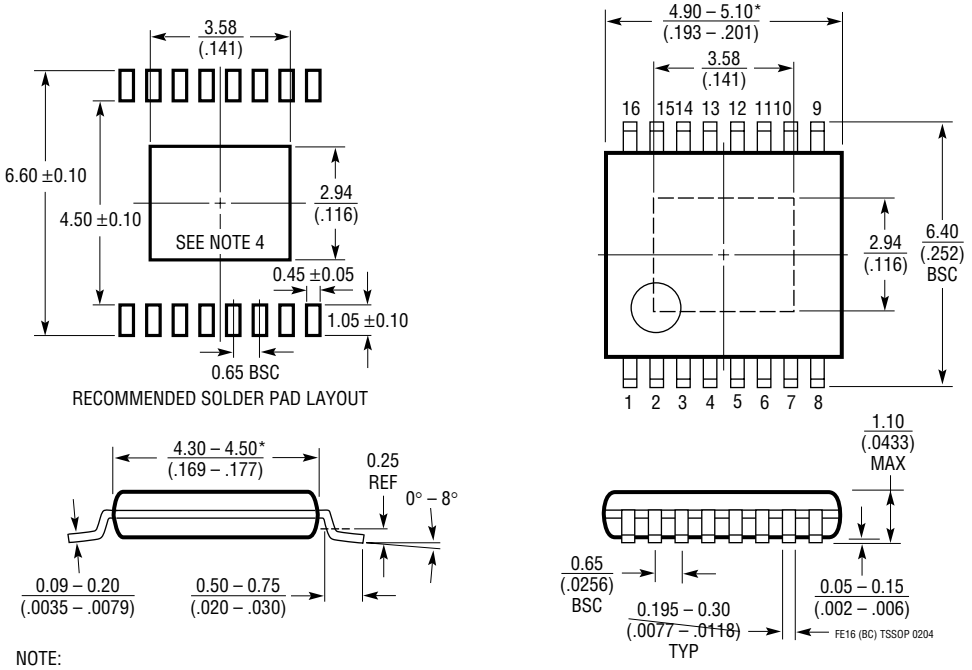
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

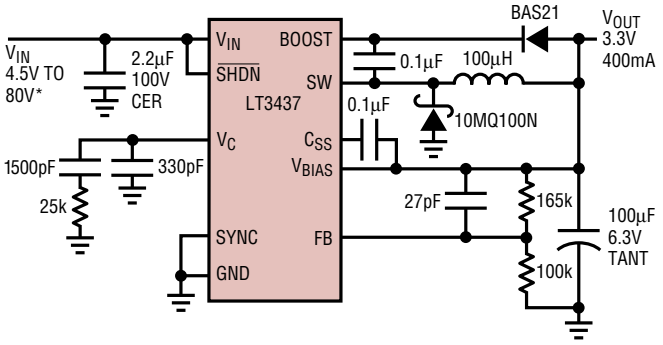
FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BC



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

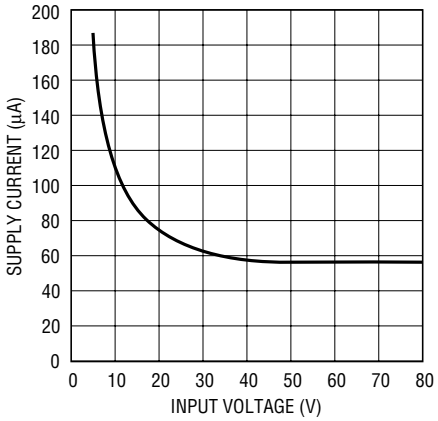
14V to 3.3V Step-Down Converter with 100μA No Load Quiescent Current



*FOR INPUT VOLTAGES ABOVE 60V, SOME RESTRICTIONS MAY APPLY

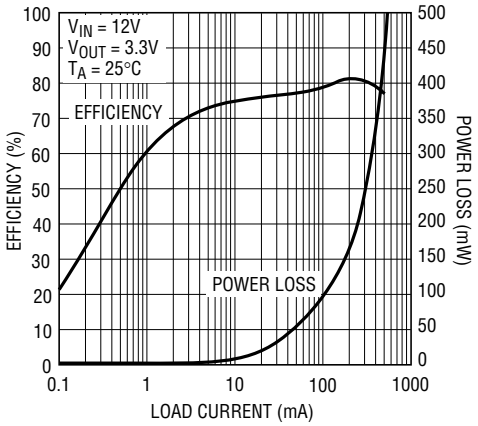
3437 TA04

Supply Current vs Input Voltage



3435 TA05

Efficiency and Power Loss vs Load Current



3437 G01

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1765	25V, 3A (I_{OUT}), 1.25MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 1mA, I_{SD} < 15µA, SO-8, TSSOP16E
LT1766	60V, 1.2A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} < 25µA, TSSOP16/E
LT1767	25V, 1.5A (I_{OUT}), 1.25MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 1mA, I_{SD} < 6µA, MS8/E
LT1776	40V, 550mA (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 7.4V to 40V, $V_{OUT(MIN)}$ = 1.24V, I_Q = 3.2mA, I_{SD} < 30µA, N8, S8
LT1936	36V, 1.4A, 500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 36V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 1.8mA, I_{SD} 4mA MS8/E
LT1940	Dual 1.2A (I_{OUT}), 1.1MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 3.8mA, TSSOP-16E
LT1956	60V, 1.2A (I_{OUT}), 500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} < 25µA, TSSOP16/E
LT1976	60V, 1.5A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.3V to 60V, I_Q = 100µA, I_{SD} < 1µA, TSSOP-16E
LT1977	60V, 1.5A (I_{OUT}), 500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.3V to 60V, I_Q = 100µA, I_{SD} < 1µA, TSSOP-16E
LT3010	80V, 50mA, Low Noise Linear Regulator	V_{IN}: 1.5V to 80V, $V_{OUT(MIN)}$ = 1.28V, I_Q = 30µA, I_{SD} < 1µA, MS8E
LT3430	60V, 2.5A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} < 30µA, TSSOP-16E
LT3431	60V, 2.5A (I_{OUT}), 500kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, $V_{OUT(MIN)}$ = 1.20V, I_Q = 2.5mA, I_{SD} < 30µA, TSSOP-16E
LT3433	60V, 400mA (I_{OUT}), 200kHz/500kHz, Buck-Boost DC/DC Converter	V_{IN}: 5V to 60V, V_{OUT}: 3.3V to 20V, I_Q = 100µA, TSSOP-16E
LT3434/LT3435	60V, 3A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.3V to 60V, I_Q = 100µA, I_{SD} < 1µA, TSSOP-16E
LT3470	40V, 300mA, MicroPower Buck Regulator with Integrated Boost and Catch Diodes	V_{IN}: 4V to 40V, $V_{OUT(MIN)}$ = 1.25V, I_Q = 26µA, ThinSOT
LTC3727/LTC3727-1	36V, 500kHz, High Efficiency Step-Down DC/DC Controllers	V_{IN}: 4V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 670µA, I_{SD} < 20µA, QFN-32, SSOP-28

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