512MB – 2x32Mx64 DDR SDRAM SO-DIMM UNBUFFERED

FEATURES

- Fast Data Transfer Rate: PC2700 and PC3200
- Double-data-rate architecture
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2.5, 3 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Auto and self refresh, (8K/64ms refresh)
- Serial presence detect with EEPROM
- Power supply:

  $V_{CC} = V_{CCQ}$: +2.5V ± 0.2V (166MHz)
  $V_{CC} = V_{CCQ}$: +2.6V ± 0.1V (200MHz)
- Dual Rank
- Standard 200 pin SO-DIMM package
  - Package height options

    D4: 31.75mm (1.25")

NOTE: Consult factory for availability of:
- RoHS compliant products
- Vendor source control options
- Industrial Temperature option

DESCRIPTION

The WV3EG232M64STSU is a 2x32Mx64 Double Data Rate SDRAM memory module based on 512Mb DDR SDRAM component. The module consists of eight 32Mx16 DDR SDRAMs in 66 pin TSOP packages mounted on a 200 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change without notice.

OPERATING FREQUENCIES

	DDR333@CL=2.5	DDR400@CL=3
Clock Speed	166MHz	200MHz
CL-t_{RCD}-t_{RP}	2.5-3-3	3-3-3

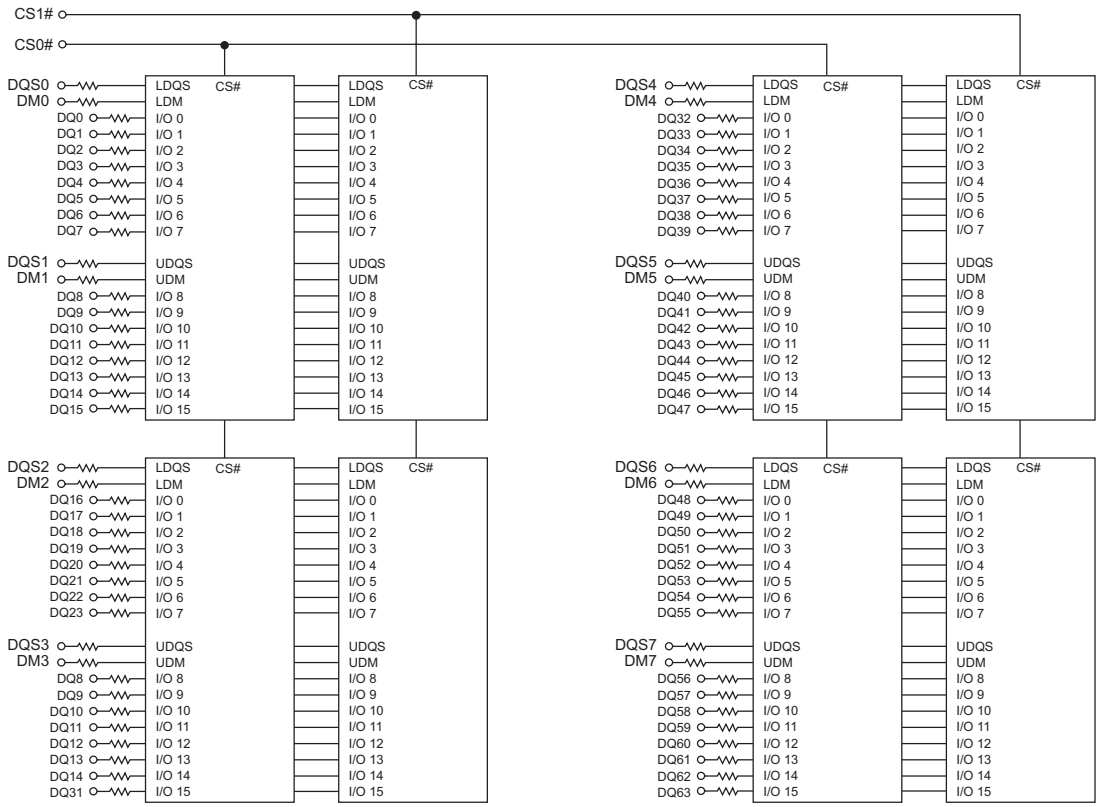
PIN CONFIGURATION

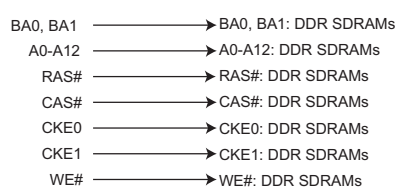
PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V_{REF}	51	V_{SS}	101	A9	151	DQ42
2	V_{REF}	52	V_{SS}	102	A8	152	DQ46
3	V_{SS}	53	DQ19	103	V_{SS}	153	DQ43
4	V_{SS}	54	DQ23	104	V_{SS}	154	DQ47
5	DQ0	55	DQ24	105	A7	155	V_{CC}
6	DQ4	56	DQ28	106	A6	156	V_{CC}
7	DQ1	57	V_{CC}	107	A5	157	V_{CC}
8	DQ5	58	V_{CC}	108	A4	158	CK1#
9	V_{CC}	59	DQ25	109	A3	159	V_{SS}
10	V_{CC}	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	V_{SS}
12	DM0	62	DM3	112	A0	162	V_{SS}
13	DQ2	63	V_{SS}	113	V_{CC}	163	DQ48
14	DQ6	64	V_{SS}	114	V_{CC}	164	DQ52
15	V_{SS}	65	DQ26	115	A10/AP	165	DQ49
16	V_{SS}	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	V_{CC}
18	DQ7	68	DQ31	118	RAS#	168	V_{CC}
19	DQ8	69	V_{CC}	119	WE#	169	DQS6
20	DQ12	70	V_{CC}	120	CAS#	170	DM6
21	V_{CC}	71	NC	121	CS0#	171	DQ50
22	V_{CC}	72	NC	122	CS1#	172	DQ54
23	DQ9	73	NC	123	NC	173	V_{SS}
24	DQ13	74	NC	124	NC	174	V_{SS}
25	DQS1	75	V_{SS}	125	V_{SS}	175	DQ51
26	DM1	76	V_{SS}	126	V_{SS}	176	DQ55
27	V_{SS}	77	NC	127	DQ32	177	DQ56
28	V_{SS}	78	NC	128	DQ36	178	DQ60
29	DQ10	79	NC	129	DQ33	179	V_{CC}
30	DQ14	80	NC	130	DQ37	180	V_{CC}
31	DQ11	81	V_{CC}	131	V_{CC}	181	DQ57
32	DQ15	82	V_{CC}	132	V_{CC}	182	DQ61
33	V_{CC}	83	NC	133	DQS4	183	DQS7
34	V_{CC}	84	NC	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	V_{SS}
36	V_{CC}	86	NC	136	DQ38	186	V_{SS}
37	CK0#	87	V_{SS}	137	V_{SS}	187	DQ58
38	V_{SS}	88	V_{SS}	138	V_{SS}	188	DQ62
39	V_{SS}	89	NC	139	DQ35	189	DQ59
40	V_{SS}	90	V_{SS}	140	DQ39	190	DQ63
41	DQ16	91	NC	141	DQ40	191	V_{CC}
42	DQ20	92	V_{CC}	142	DQ44	192	V_{CC}
43	DQ17	93	V_{CC}	143	V_{CC}	193	SDA
44	DQ21	94	V_{CC}	144	V_{CC}	194	SA0
45	V_{CC}	95	CKE1	145	DQ41	195	SCL
46	V_{CC}	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	V_{CC}SPD
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	V_{SS}	199	NC
50	DQ22	100	A11	150	V_{SS}	200	NC

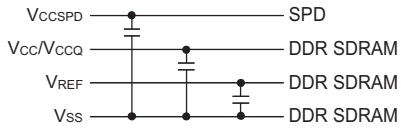
PIN NAMES

A0-A12	Address input (Multiplexed)
BA0-BA1	Bank SelectAddress
DQ0-DQ63	Data Input/Output
DQS0-DQS7	Data Strobe Input/Output
CK0, CK1	Clock Inputs
CK0#, CK1#	Clock inputs complement
CKE0, CKE1	Clock Enable Inputs
CS0#, CS1#	Chip select Inputs
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DM0-DM7	Data-In Mask
V_{CC}	Power Supply
V_{CCQ}	Power Supply for I/Os
V_{SS}	Ground
V_{REF}	Reference Power Supply
V_{CCSPD}	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
NC	No Connect

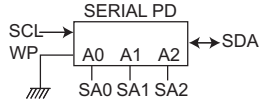
FUNCTIONAL BLOCK DIAGRAM



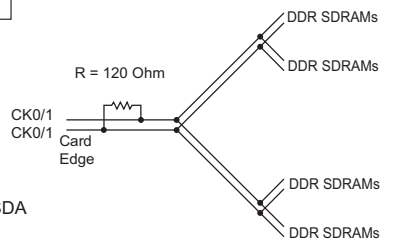




Clock Wiring	
Clock Input	SDRAMs
CK0/CK0# CK1/CK1#	4 SDRAMs 4 SDRAMs



*Clock Net Wiring



NOTE: All resistor values are 22 ohmes unless otherwise specified.

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{CC} and V_{CCQ} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-0.5 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Operating temperature	T_A	0 ~ 70	°C
Power Dissipation	P_D	8	W
Short circuit output current	I_{OS}	50	mA

NOTES:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC CHARACTERISTICS FOR 335 SPEED GRADE

Parameter		Symbol	Min	Max	Unit	Note
Supply voltage DDR266/DDR333 (nominal V_{CC} of 2.5V)		V_{CC}	2.3	2.7	V	
I/O Supply voltage DDR266/DDR333 (nominal V_{CC} of 2.5V)		V_{CCQ}	2.3	2.7	V	
I/O Reference voltage		V_{REF}	0.49*V_{CCQ}	0.51*V_{CCQ}	V	1
I/O Termination voltage		V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage		V_{IH}(DC)	V_{REF}+0.15	V_{CCQ}+0.30	V	
Input logic low voltage		V_{IL}(DC)	-0.3	V_{REF}-0.15	V	
Input voltage level, CK and CK#		V_{IN}(DC)	-0.3	V_{CCQ}+0.30	V	
Input differential voltage, CK and CK#		V_{ID}(DC)	0.3	V_{CCQ}+0.60	V	3
Input crossing point voltage, CK and CK#		V_{IX}(DC)	0.3	V_{CCQ}+0.60	V	
Input leakage current	Addr, CAS#, RAS#, WE#	I_I	-16	16	µA	
	CS#, CKE		-8	8	µA	
	CK, CK#		-8	8	µA	
	DM		-4	4	µA	
Output leakage current		I_{OZ}	-10	10	µA	
Output high current (normal strengh); V_{OUT} = V +0.84V		I_{OH}	-16.8	—	mA	
Output high current (normal strengh); V_{OUT} = V_{TT} -0.84V		I_{OL}	16.8	—	mA	
Output high current (half strengh); V_{OUT} = V_{TT} +0.45V		I_{OH}	-9	—	mA	
Output high current (half strengh); V_{OUT} = V_{TT} -0.45V		I_{OL}	9	—	mA	

NOTES:

1. V_{REF} is expected to be equal to 0.5*V_{CCQ} of the transmitting device, and to track variations in the DC level of the same. Peak to peak noise on V_{REF} may not exceed ±2% of the DC value
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors,is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.

DC CHARACTERISTICS FOR 403 SPEED GRADE

Parameter		Symbol	Min	Max	Unit	Note
Supply voltage DDR266/DDR333 (nominal V_{CC} of 2.5V)		V_{CC}	2.5	2.7	V	
I/O Supply voltage DDR266/DDR333 (nominal V_{CC} of 2.5V)		V_{CCQ}	2.5	2.7	V	
I/O Reference voltage		V_{REF}	0.49*V_{CCQ}	0.51*V_{CCQ}	V	1
I/O Termination voltage		V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage		V_{IH}(DC)	V_{REF}+0.15	V_{CCQ}+0.30	V	
Input logic low voltage		V_{IL}(DC)	-0.3	V_{REF}-0.15	V	
Input voltage level, CK and CK#		V_{IN}(DC)	-0.3	V_{CCQ}+0.30	V	
Input differential voltage, CK and CK#		V_{ID}(DC)	0.3	V_{CCQ}+0.60	V	3
Input crossing point voltage, CK and CK#		V_{IX}(DC)	0.3	V_{CCQ}+0.60	V	
Input leakage current	Addr, CAS#, RAS#, WE#	I_I	-16	16	µA	
	CS#, CKE		-8	8	µA	
	CK, CK#		-8	8	µA	
	DM		-4	4	µA	
Output leakage current		I_{OZ}	-10	10	µA	
Output high current (normal strengh); V_{OUT} = V +0.84V		I_{OH}	-16.8	—	mA	
Output high current (normal strengh); V_{OUT} = V_{TT} -0.84V		I_{OL}	16.8	—	mA	
Output high current (half strengh); V_{OUT} = V_{TT} +0.45V		I_{OH}	-9	—	mA	
Output high current (half strengh); V_{OUT} = V_{TT} -0.45V		I_{OL}	9	—	mA	

NOTES:
1. V_{REF} is expected to be equal to 0.5*V_{CCQ} of the transmitting device, and to track variations in the DC level of the same. Peak to peak noise on V_{REF} may not exceed ±2% of the DC value
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors,is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.

CAPACITANCE

T_A = 25°C, f = 100MHz

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A12, BA0-BA1, RAS#, CAS#, WE#)	C_{IN1}	20	28	pF
Input Capacitance (CKE0, CKE1)	C_{IN2}	12	16	pF
Input Capacitance (CS0#, CS1#)	C_{IN3}	12	16	pF
Input Capacitance (CK0, CK0#, CK1, CK1#)	C_{IN4}	12	16	pF
Input Capacitance (DM0-DM7), (DQS0-DQS7)	C_{IN5}	12	14	pF
Input Capacitance (DQ0-DQ63)	C_{OUT1}	12	14	pF

SAMSUNG & NANYA components.

AC OPERATING TEST CONDITIONS

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage	$V_{IH(AC)}$	V_{REF} +0.31		V	1
Input Low (Logic 0) Voltage	$V_{IL(AC)}$		V_{REF} -0.31	V	1
Input Differential Voltage, CK and CK# inputs	$V_{ID(AC)}$	0.7	V_{CCQ}+0.6	V	
Input Crossing Point Voltage, CK and CK# inputs	$V_{IX(AC)}$	0.5*V_{CCQ}-0.2	0.5*V_{CCQ}+0.2	V	

NOTES:
1. V_{IH} overshoot: V_{IH} = V_{CCQ} +1.5V for a pulse width < 3ns and the pulse can not be greater than 1/3 of the cycle rate.
   V_{IL} undershoot: V_{IL} = -1.5V for a pulse width < 3ns and the pulse can not be greater than 1/3 of the cycle rate.

I_{DD} SPECIFICATIONS AND TEST CONDITIONS

Parameter	Symbol	Conditions	DDR333 @ CL = 2.5 Max	DDR400 @ CL = 3 Max	Unit
Operating current:	I_{DD0}*	One device bank active; Active-Precharge; t_{RC} = $t_{RC(MIN)}$; t_{CK} = $t_{CK(MIN)}$; DQ,DM and DQS inputs change once per clock cycle; Address and control inputs change once every two clock cycles	840	500	mA
Operating current	I_{DD1}*	One device bank; Active-Read-Precharge; BL=4; t_{RC} = $t_{RC(MIN)}$; t_{CK} = $t_{CK(MIN)}$; I_{OUT} = 0mA; Address and control inputs change once per clock cycle	1,120	660	mA
Percharge power-down standby current	I_{DD2P}**	All device banks are idle; Power-down mode; t_{CK} = $t_{CK(MIN)}$; CKE=LOW	40	40	mA
Idle standby current	I_{DD2F}**	CS# = HIGH; All device banks are idle; t_{CK} = $t_{CK(MIN)}$; CKE=HIGH; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS and DM	240	240	mA
Active power-down standby current	I_{DD3P}**	One device bank active; Power-down mode; t_{CK} = $t_{CK(MIN)}$; CKE=LOW	240	360	mA
Active standby current	I_{DD3N}**	CS# = HIGH; CKE=HIGH; One device bank active; t_{RC} = $t_{RAS(MAX)}$; t_{CK} = $t_{CK(MIN)}$; DQ, DM and DQS inputs change twice per clock cycle; Address and other control inputs changing once per clock cycle	360	480	mA
Operating current	I_{DD4R}*	Burst = 2; Reads; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; t_{CK} = $t_{CK(MIN)}$; I_{OUT} = 0mA	1,360	780	mA
Operating current	I_{DD4W}*	Burst = 2; Writes; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; t_{CK} = $t_{CK(MIN)}$; DQ, DM and DQS inputs change twice per clock cycle	1,480	880	mA
Auto refresh current	I_{DD5}**	t_{RC} =$t_{RFC(MIN)}$	1,640	1,760	mA
Self refresh current	I_{DD6}**	CKE < 0.2V	40	40	mA
Orerating current	I_{DD7}*	Four device bank interleaving Reads Burst=4 with auto precharge E_{RC} = $t_{RC(MIN)}$; t_{CK} = $t_{CK(MIN)}$; Address and control inputs change only during Active READ, or WRITE commands	3,040	1,620	mA

NOTE:

I_{DD} specification is based on SAMSUNG components. Other DRAM Manufacturers specification may be different.

* Value calculated as one module rank in this operation condition and other module rank in I_{DD2P} (CKE low) mode.

** Value calculated as all module ranks in this operation condition.

I_{DD} SPECIFICATIONS AND TEST CONDITIONS

Parameter	Symbol	Conditions	DDR333 @ CL = 2.5 Max	Unit
Operating current - One bank Active-Precharge	I_{DD0}*	Operating Current: One device bank active; Active-Precharge; $t_{RC} = t_{RC(min)}$; $t_{CK} = t_{CK(min)}$ DQ, DM, and DQS inputs change once per clock cycle; Address and control inputs changing once every two clock cycle	768	mA
Operating current - One bank operation	I_{DD1}*	Operating Current: One device bank; Active-Read-Precharge; BL = 4; $t_{RC} = t_{RC(min)}$; $t_{CK} = t_{CK(min)}$; I_{OUT} = 0mA; Address and control inputs change once per clock cycle	792	mA
Percharge power-down standby current	I_{DD2P}**	Precharge Power Down Standby Current: All device banks are idle; Power Down mode; $t_{CK} = t_{CK(min)}$; CKE = LOW	40	mA
Precharge Floating standby current	I_{DD2F}**	Idle Standby Current: CS#=HIGH; All device banks are idle; $t_{CK} = t_{CK(min)}$ CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN} = V_{REF}$ for DQ, DQS, and DM	200	mA
Active power - down standby current	I_{DD3P}**	Active Power Down Standby Current: One device bank active; Power Down mode; $t_{CK} = t_{CK(min)}$; CKE = LOW	88	mA
Active standby current	I_{DD3N}**	Active Standby Current: CS# = HIGH; CKE = HIGH; One device bank active $t_{RC} = t_{RAS(max)}$; $t_{CK} = t_{CK(min)}$; DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	360	mA
Operating current - burst read	I_{DD4R}*	Operating Current: Burst = 2; Reads; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; $t_{CK} = t_{CK(min)}$; I_{OUT} = 0mA	832	mA
Operating current - burst write	I_{DD4W}*	Operating Current: Burst = 2; Writes; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; $t_{CK} = t_{CK(min)}$; DQ, DM, and DQS inputs change twice per clock cycle	936	mA
Auto refresh current	I_{DD5}**	Auto-Refresh Current: $t_{RC} = t_{RFC(min)}$	1,544	mA
Self refresh current; CKE =< 0.2V	I_{DD6}**	Self-Refresh Current: CKE < 0.2V	40	mA
Operating current - Four bank operation	I_{DD7}*	Operating Current: Four device bank interleaving Reads Burst = 4 with auto precharge; $t_{RC} = t_{RC(min)}$; $t_{CK} = t_{CK(min)}$; Address and control inputs only during Active READ or WRITE commands.	2,456	mA

NOTE:

I_{DD} specification is based on NANYA components. Other DRAM Manufacturers specification may be different.

* Value calculated as one module rank in this operation condition and other module rank in I_{DD2P} (CKE low) mode.

** Value calculated as all module ranks in this operation condition.

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Parameter		Symbol	403		335		Unit
			Min	Max	Min	Max	
Row Cycle Time		t_{RC}	55		60		t_{CK}
Refresh row cycle time		t_{RFC}	70		72		ns
Row active		t_{RAS}	40	70K	42	120K	ns
RAS# to CAS# delay		t_{RCD}	15		18		t_{CK}
Row precharge time		t_{RP}	15		18		ns
Row active to row active delay		t_{RRD}	10		12		ns
Write recovery time		t_{WR}	15		15		ns
Last data into Read command		t_{WTR}	2		1		ns
Clock cycle time	CL=2.5	t_{CK}	-	-	6	12	ns
	CL=3		5	10	-	-	ns
Clock high level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}
Clock low level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}
DQS-out access time from CK/CK#		t_{DQSCK}	-0.55	0.55	-0.6	+0.6	ns
Output data access time from CK/CK#		t_{AC}	-0.65	0.65	-0.7	+0.7	ns
Data strobe edge to output data edge		t_{DQSQ}	-	0.4	-	0.45	ns
Read Preamble		t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}
Read Postamble		t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}
CK to valid DQS-in		t_{DQSS}	0.72	1.28	0.75	1.25	t_{CK}
DQS-in setup time		t_{WPRES}	0		0		ns
DQS-in hold time		t_{WPRE}	0.25		0.25		t_{CK}
DQS falling edge to CK rising-setup time		t_{DSS}	0.2		0.2		t_{CK}
DQS falling edge to CK rising-hold time		t_{DSH}	0.2		0.2		t_{CK}
DQS-in high level width		t_{DQSH}	0.35		0.35		t_{CK}
DQS-in low level width		t_{DQSL}	0.35		0.35		t_{CK}
Address and control input setup time (fast)		t_{IS}	0.6		0.75		ns

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

Parameter	Symbol	403		335		Unit
		Min	Max	Min	Max	
Address and control input hold time (fast)	t_{IH}	0.6		0.75		ns
Address and control input setup (slow)	t_{IS}	0.7		0.7		ns
Address and control input hold time (slow)	t_{IH}	0.7		0.7		ns
Data-out high impedence time from CK/CK#	t_{HZ}		+0.65		+0.7	ns
Data-out low impedence time from CK/CK#	t_{LZ}	-0.65		-0.7		ns
Mode register set cycle time	t_{MRD}	10		10		ns
DQ & DM setup time to DQS	t_{DS}	0.4		0.4		ns
DQ & DM hold time to DQS	t_{DH}	0.4		0.4		ns
Control & address input pulse width	t_{IPW}	2.2		2.2		ns
DQ & DM input pulse width	t_{DIPW}	1.75		1.75		ns
Exit self refresh to non-Read command	t_{XSNR}	75		75		ns
Exit self refresh to Read command	t_{XSRD}	200		200		t_{CK}
Refresh interval time	t_{REFI}		7.8		7.8	us
Output DQS valid window	t_{QH}	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	—	ns
Clock half period	t_{HP}	t_{CL}min or t_{CH}min	-	t_{CL}min or t_{CH}min	—	ns
Data hold skew factor	t_{QHS}		0.5		0.55	ns
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	ns
Active Read with auto precharge command	t_{RAP}	15		18		ns
Auto precharge write recovery + Precharge time	t_{RAL}	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		t_{CK}

NOTE:
AC Timing Parameters are based on SAMSUNG components. Other DRAM Manufacturers parameters may be different.

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Parameter		Symbol	335		Unit
			Min	Max	
Row cycle time		t_{RC}	60		t_{CK}
Refresh row cycle time		t_{RFC}	72		ns
Row active time		t_{RAS}	42	120K	ns
RAS# to CAS# delay		t_{RCD}	18		t_{CK}
Row precharge time		t_{RP}	18		ns
Row active to Row active delay		t_{RRD}	12		ns
Write recovery time		t_{WR}	15		ns
Last data into Read command		t_{WTR}	1		t_{CK}
Col. address to Col. address delay		t_{CCD}	1		t_{CK}
Clock cycle time	CL=2.5	t_{CK}	6	12	ns
Clock high level width		t_{CH}	0.45	0.55	t_{CK}
Clock low level width		t_{CL}	0.45	0.55	t_{CK}
DQS-out access time from CK/CK#		t_{DQSCK}	-0.6	+0.6	ns
Output data access time from CK/CK#		t_{AC}	-0.7	+0.7	ns
Data strobe edge to output data edge		t_{DQSQ}	-	0.45	ns
Read Preamble		t_{RPRE}	0.9	1.1	t_{CK}
Read Postamble		t_{RPST}	0.4	0.6	t_{CK}
CK to valid DQS-in		t_{DQSS}	0.75	1.25	t_{CK}
DQS-in setup time		t_{WPRES}	0		ns
DQS-in hold time		t_{WPRE}	0.25		t_{CK}
DQS falling edge to CK rising-setup time		t_{DSS}	0.2		t_{CK}
DQS falling edge from CK rising-hold time		t_{DSH}	0.2		t_{CK}
DQS-in high level width		t_{DQSH}	0.35		t_{CK}
DQS-in low level width		t_{DQSL}	0.35		t_{CK}
Address and Control Input setup time (fast)		t_{IS}	0.75		ns
Address and Control Input hold time (fast)		t_{IH}	0.75		ns
Address and Control Input setup time (slow)		t_{IS}	0.7		ns
Address and Control Input hold time (slow)		t_{IH}	0.7		ns
Data-out high impedence time from CK/CK#		t_{HZ}	-0.7	+0.7	ns
Data-out low impedence time from CK/CK#		t_{LZ}	-0.7	+0.7	ns

Note:
AC Timing Parameters are based on NANYA components. Other DRAM Manufacturers parameters may be different.

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

Parameter	Symbol	335		Unit
		Min	Max	
Mode register set cycle time	tMRD	10		ns
DQ & DM setup time to DQS	tDS	0.4		ns
DQ & DM hold time to DQS	tDH	0.4		ns
Control & Address input pulse width	tIPW	2.2		ns
DQ & DM input pulse width	tDIPW	1.75		ns
Exit self refresh o non-Read command	tXSNR	75		ns
Exit self refresh to read command	tXSRD	200		t_{CK}
Refresh interval time	tREFI		7.8	us
Output DQS valid window	tQH	t_{HP} - t_{QHS}	—	ns
Clock half period	tHP	t_{CL}min or t_{CH}min	—	ns
Data hold skew factor	tQHS		0.55	ns
DQS write postamble time	tWPST	0.4	0.6	t_{CK}
Active to Read with Auto precharge command	tRAP	18		
Auto precharge write recovery + Precharge time	tDAL	(t_{WR}/t_{CK}) + (t_{RP}/t_{CK})		t_{CK}

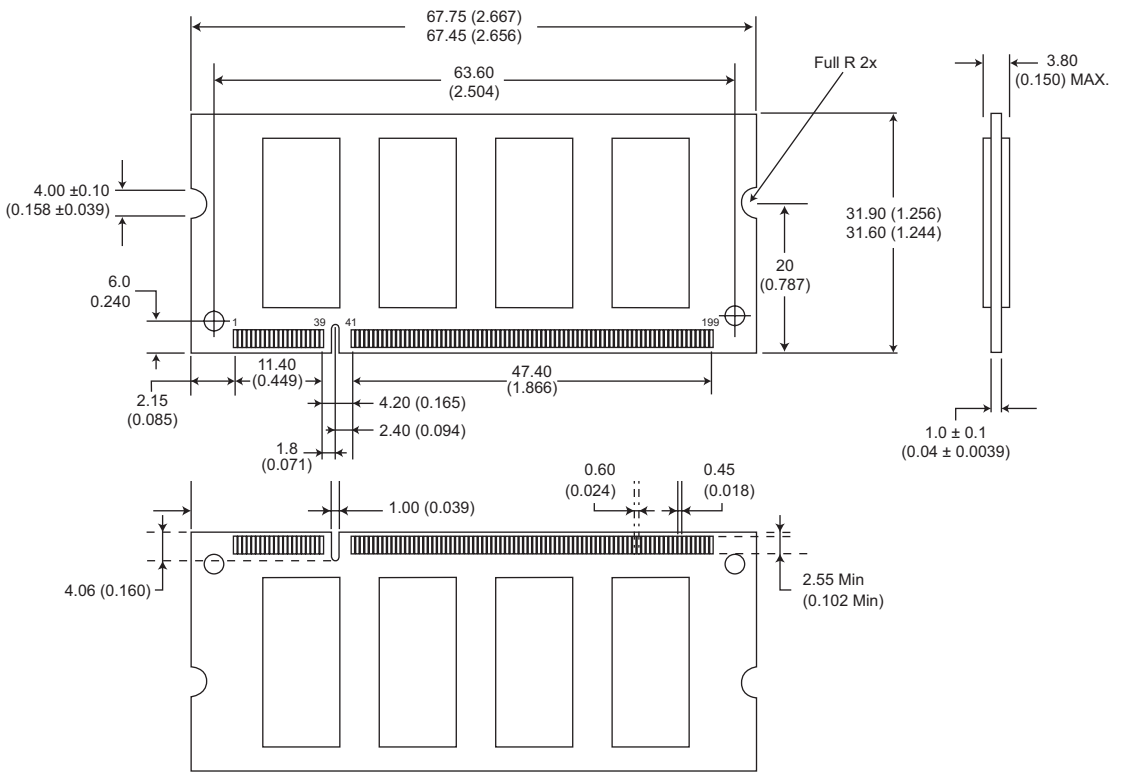
ORDERING INFORMATION FOR D4

Part Number	Speed	Height*	Commercial Operating Range
WV3EG232M64STSU335D4xG	166MHz/333Mbps, CL=2.5	31.75mm (1.25") MAX	0°C to 70°C
WV3EG232M64STSU335D4IxG	166MHz/333Mbps, CL=2.5	31.75mm (1.25") MAX	-40°C to 85°C
WV3EG232M64STSU403D4sG	200MHz/400Mbps, CL=3	31.75mm (1.25") MAX	0°C to 70°C

NOTES:

- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung, N = Nanya and consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option (add "I" for industrial temperature option).

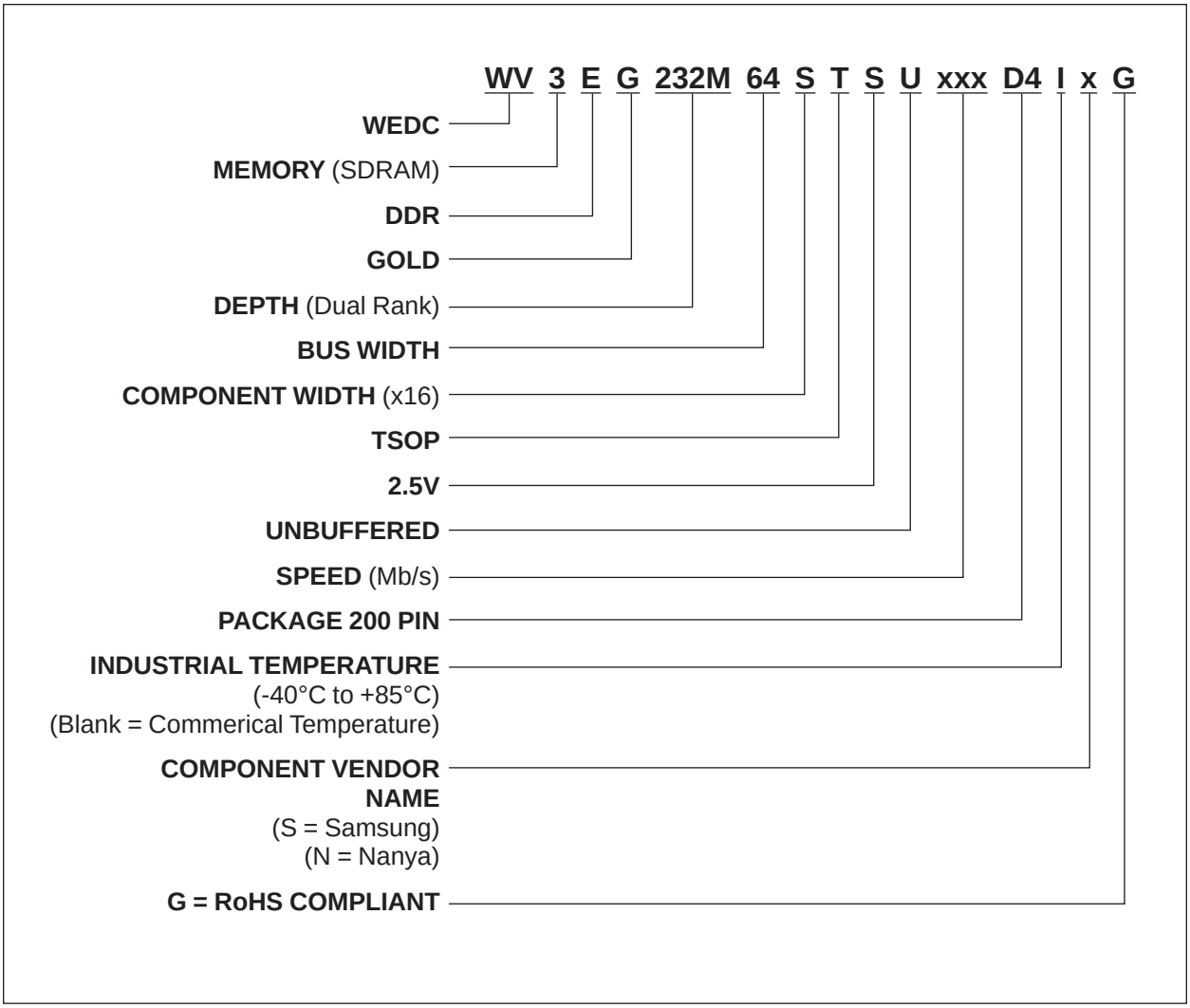
PACKAGE DIMENSIONS FOR D4



Tolerances: ±0.15 (0.006) unless otherwise specified

* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

512MB – 2x32Mx64, DDR SDRAM UNBUFFERED

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	8-05	Preliminary
Rev 1	1.0 Added Samsung's I_{DD}, CAP and AC Specifications	9-05	Preliminary
Rev 2	2.0 Added DDR400(PC3200) Data Rate	8-06	Preliminary