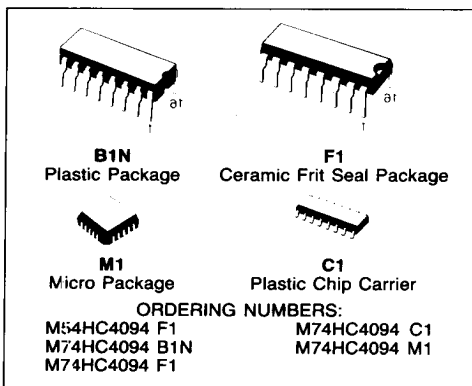


8-BIT SIPO SHIFT LATCH REGISTER (3-STATE)

- **HIGH SPEED**
 $f_{MAX} = 42 \text{ MHz (TYP.) at } V_{CC} = 5V$
- **LOW POWER DISSIPATION**
 $I_{CC} = 4 \mu A \text{ (MAX.) at } T_A = 25^\circ C$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 10 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- **PIN AND FUNCTION COMPATIBLE**
 WITH 4094B



DESCRIPTION

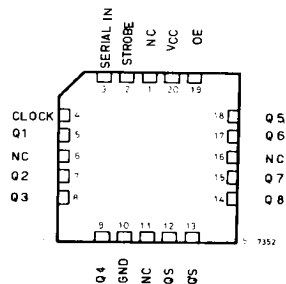
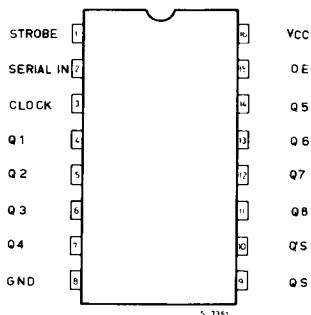
The M54/74HC4094 is a high speed CMOS 8 BIT SIPO SHIFT LATCH REGISTER fabricated with silicon gate C²MOS technology.

It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This device consists of an 8-bit shift register and an 8-bit latch with 3-state output buffer. Data is shifted serially through the shift register on the positive going transition of the clock input signal. The output of the last stage (Qs) can be used to cascade several devices.

Data on the Qs output is transferred to a second output (Qs') on the following negative transition of the clock input signal. The data of each stage of the shift register is provided with a latch, which latches data on the negative going transition of the STROBE input signal. When the STROBE input is held high, data propagates through the latch to a 3-state output buffer.

This buffer is enabled when OUTPUT ENABLE input is taken high. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

TRUTH TABLE

CK	OE	ST	SI	PARA. OUT.		SERI. OUT	
				Q1	Qn	Qs	Qs'
	H	H	L	L	Qn-1	Q7	NC
	H	H	H	H	Qn-1	Q7	NC
	H	L	X	NC	NC	Q7	NC
	L	X	X	Z	Z	Q7	NC
	H	X	X	NC	NC	NC	Qs
	L	X	X	Z	Z	NC	Qs

X: DON'T CARE

NC: NO CHANGE

Z: HIGH IMPEDANCE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	- 65 to 150	°C

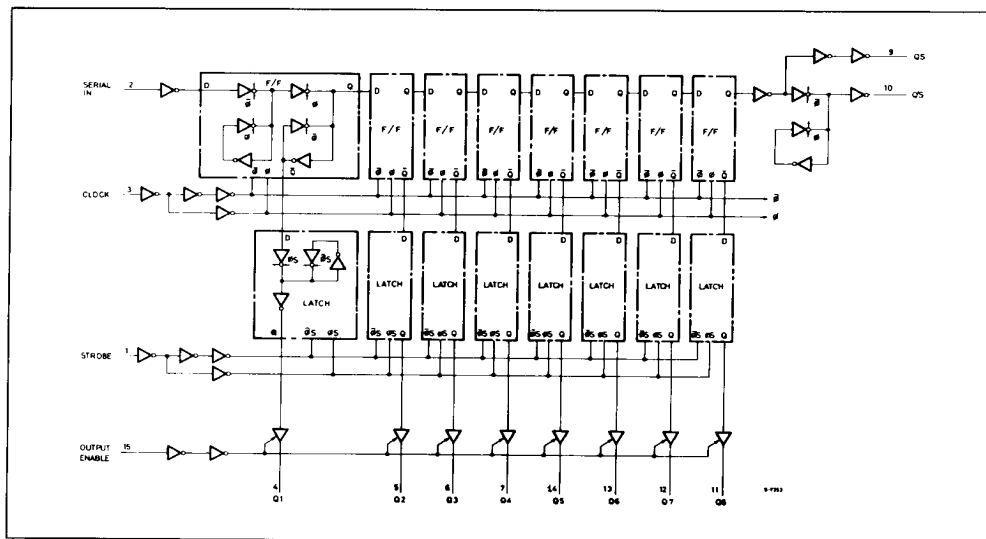
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

(*) 500 mW: $\cong$ 65°C derate to 300 mW/°C: 65°C to 85°C.

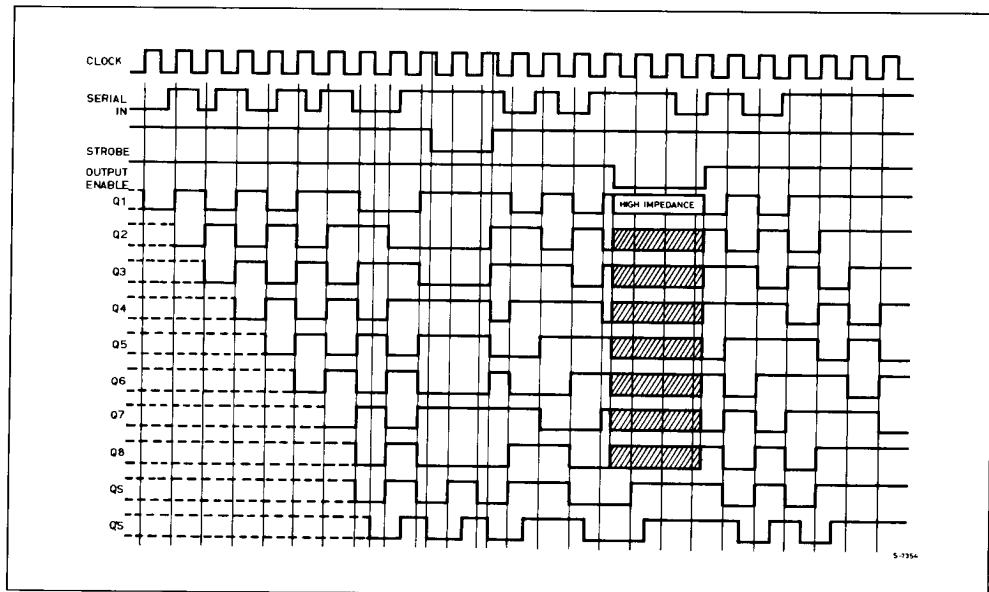
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	- 40 to 85 - 55 to 125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

LOGIC DIAGRAM



LOGIC DIAGRAM



DC SPECIFICATIONS

Symbol	Parameter	V _{CC}	Test Condition		T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0 4.5 6.0			1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V _{IL}	Low Level Input Voltage	2.0 4.5 6.0			— — —	— — —	0.5 1.35 1.8	— 1.35 1.8	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V _{OH}	High Level Output Voltage	2.0	V _I	I _O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V _{IH} or V _{IL}	— 20 µA	4.4	4.5	—	4.4	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	5.9	—	
		4.5 6.0		— 4.0 mA — 5.2 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	— —	
V _{OL}	Low Level Output Voltage	2.0	V _{IH} or V _{IL}	20 µA	—	0.0	0.1	—	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	—	0.1	
		4.5 6.0		4.0 mA 5.2 mA	— —	0.17 0.18	0.26 0.26	— —	0.33 0.33	— —	0.40 0.40	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND		—	—	± 0.1	—	± 1.0	—	± 1.0	µA
I _{OZ}	3-State Output Off-State Current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND		—	—	± 0.5	—	± 5	—	± 10	µA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND		—	—	4	—	40	—	80	µA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t _{TLH} t _{THL}	Output Transition Time		4	8	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK-QN)		31	48	ns
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK-Qs, Qs')		22	35	ns
t _{PLH}	Propagation Delay Time		23	36	ns
f _{MAX}	Maximum Clock Frequency	22	42		MHz

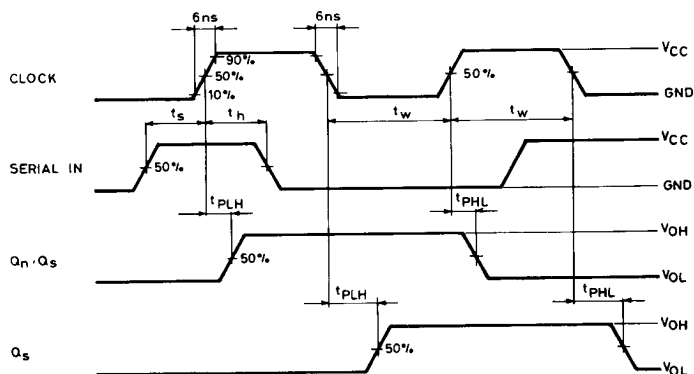
AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - Q_n)	2.0 4.5 6.0		— — —	140 35 30	270 54 46	— — —	340 68 58	— — —	405 81 69	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK, Q_s , Q_s')	2.0 4.5 6.0		— — —	104 26 22	200 40 34	— — —	250 50 43	— — —	300 60 51	ns
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE - Q_n)	2.0 4.5 6.0		— — —	135 27 23	210 42 36	— — —	265 53 45	— — —	315 63 54	ns
f_{MAX}	Maximum Clock Frequency	2.0 4.5 6.0		4 20 24	10 38 45	— — —	3.2 16 19	— — —	2.6 13 15	— — —	MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CLOCK)	2.0 4.5 6.0		— — —	35 9 8	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
$t_{W(H)}$	Minimum Pulse Width (STROBE)	2.0 4.5 6.0		— — —	35 9 8	100 20 17	— — —	125 25 21	— — —	150 30 26	ns
t_s	Minimum Set-up Time (SERIAL-IN)	2.0 4.5 6.0		— — —	26 6 5	75 15 13	— — —	95 19 16	— — —	110 22 19	ns
t_s	Minimum Set-up Time (STROBE)	2.0 4.5 6.0		— — —	50 13 11	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
t_h	Minimum Hold Time (SERIAL-IN)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_h	Minimum Hold Time (STROBE)	2.0 4.5 6.0		— — —	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	ns
t_{PZL} t_{PZH}	3-State Output Enable Time	2.0 4.5 6.0	$R_L = 1\text{k}\Omega$	— — —	76 19 16	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0 4.5 6.0	$R_L = 1\text{k}\Omega$	— — —	84 21 18	150 30 26	— — —	190 38 33	— — —	225 45 38	ns
C_{IN}	Input Capacitance			—	5	10	—	10	—	10	pF
$C_{PD} (*)$	Power Dissipation Capacitance			—	167	—	—	—	—	—	pF

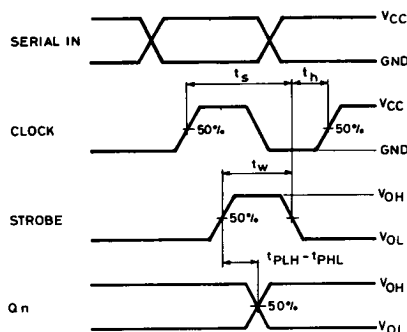
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation. $I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

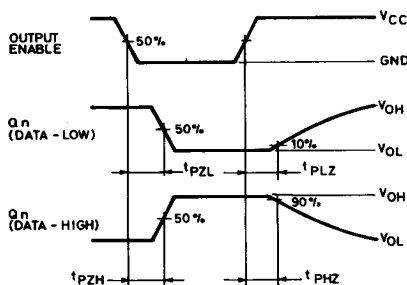
SWITCHING CHARACTERISTICS TEST WAVEFORM



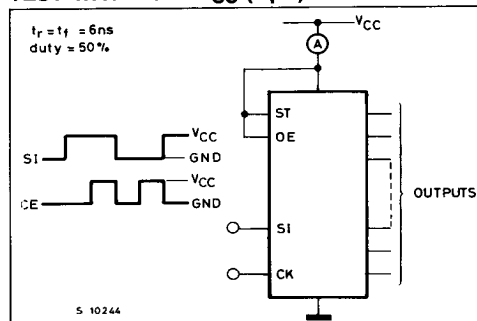
S - 10241



S - 10242



S - 10243

TEST WAVEFORM I_{CC} (Opr.)

S 10244

CPD CALCULATION

CPD is to be calculated with the following formula by using the measured value of I_{CC} (Opr.) in the test circuit opposite.

$$C_{PD} = \frac{I_{CC}(\text{Opr.})}{f_{IN} \cdot V_{CC}}$$

In determining the typical value of C_{PD} , a relatively high frequency of 1MHz was applied to f_{IN} , in order to eliminate any error caused by the quiescent supply current.