Ultraprecision, Low Noise, 2.048 V/2.500 V/ 3.00 V/5.00 V XFET® Voltage References

ADR420/ADR421/ADR423/ADR425

FEATURES

- Low noise (0.1 Hz to 10 Hz)
  - ADR420: 1.75 µV p-p
  - ADR421: 1.75 µV p-p
  - ADR423: 2.0 µV p-p
  - ADR425: 3.4 µV p-p
- Low temperature coefficient: 3 ppm/°C
- Long-term stability: 50 ppm/1,000 hours
- Load regulation: 70 ppm/mA
- Line regulation: 35 ppm/V
- Low hysteresis: 40 ppm typical
- Wide operating range
  - ADR420: 4 V to 18 V
  - ADR421: 4.5 V to 18 V
  - ADR423: 5 V to 18 V
  - ADR425: 7 V to 18 V
- Quiescent current: 0.5 mA maximum
- High output current: 10 mA
- Wide temperature range: −40°C to +125°C

APPLICATIONS

- Precision data acquisition systems
- High resolution converters
- Battery-powered instrumentation
- Portable medical instruments
- Industrial process control systems
- Precision instruments
- Optical network control circuits

PIN CONFIGURATION

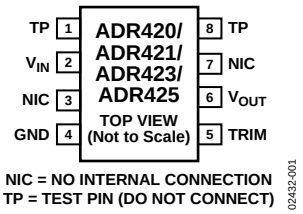

Figure 1. 8-Lead SOIC, 8-Lead MSOP

GENERAL DESCRIPTION

The ADR42x are a series of ultraprecision, second-generation eXtra implanted junction FET (XFET) voltage references featuring low noise, high accuracy, and excellent long-term stability in SOIC and MSOP footprints.

Patented temperature drift curvature correction technique and XFET technology minimize nonlinearity of the voltage change with temperature. The XFET architecture offers superior accuracy and thermal hysteresis to the band gap references. It also operates at lower power and lower supply headroom than the buried Zener references.

The superb noise and the stable and accurate characteristics of the ADR42x make them ideal for precision conversion applications such as optical networks and medical equipment. The ADR42x trim terminal can also be used to adjust the output voltage over a ±0.5% range without compromising any other performance. The ADR42x series voltage references offer two electrical grades and are specified over the extended industrial temperature range of −40°C to +125°C. Devices have 8-lead SOIC or 30% smaller, 8-lead MSOP packages.

ADR42x PRODUCTS

Table 1.

Model	Output Voltage (V_O)	Initial Accuracy		Temperature Coefficient (ppm/°C)
		mV	%	
ADR420	2.048	1, 3	0.05, 0.15	3, 10
ADR421	2.50	1, 3	0.04, 0.12	3, 10
ADR423	3.00	1.5, 4	0.04, 0.13	3, 10
ADR425	5.00	2, 6	0.04, 0.12	3, 10

Rev. G

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ADR420 ELECTRICAL SPECIFICATIONS

@ V_{IN} = 5.0 V to 15.0 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage, A Grade	V_O		2.045	2.048	2.051	V
Initial Accuracy	V_{OERR}		−3		+3	mV
			−0.15		+0.15	%
Output Voltage, B Grade	V_O		2.047	2.048	2.049	V
Initial Accuracy	V_{OERR}		−1		+1	mV
			−0.05		+0.05	%
Temperature Coefficient A Grade,	TCV_O	−40°C < TA < +125°C		2	10	ppm°C
Temperature Coefficient, B Grade				1	3	ppm/°C
Supply Voltage Headroom	$V_{IN} – V_O$		2			V
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 5 V to 18 V		10	35	ppm/V
		−40°C < TA < +125°C				
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA			70	ppm/mA
		−40°C < TA < +125°C				
Quiescent Current	I_{IN}	No load		390	500	µA
		−40°C < TA < +125°C			600	µA
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		1.75		µV p-p
Voltage Noise Density	e_N	1 kHz		60		nV/√Hz
Turn-On Settling Time	t_R			10		µs
Long-Term Stability	ΔV_O	1,000 hours		50		ppm
Output Voltage Hysteresis	V_{O_HYS}			40		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 10 kHz		75		dB
Short Circuit to GND	I_{SC}			27		mA

ADR421 ELECTRICAL SPECIFICATIONS

@ V_{IN} = 5.0 V to 15.0 V, T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage, A Grade	V_O		2.497	2.500	2.503	V
Initial Accuracy	V_{OERR}		−3		+3	mV
			−0.12		+0.12	%
Output Voltage, B Grade	V_O		2.499	2.500	2.501	V
Initial Accuracy	V_{OERR}		−1		+1	mV
			−0.04		+0.04	%
Temperature Coefficient, A Grade	TCV_O	−40°C < TA < +125°C		2	10	ppm/°C
Temperature Coefficient, B Grade				1	3	ppm/°C
Supply Voltage Headroom	$V_{IN} - V_O$		2			V
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 5 V to 18 V		10	35	ppm/V
		−40°C < TA < +125°C				
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA			70	ppm/mA
		−40°C < TA < +125°C				
Quiescent Current	I_{IN}	No load		390	500	µA
		−40°C < TA < +125°C			600	µA
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		1.75		µV p-p
Voltage Noise Density	e_N	1 kHz		80		nV/√Hz
Turn-On Settling Time	t_R			10		µs
Long-Term Stability	ΔV_O	1,000 hours		50		ppm
Output Voltage Hysteresis	V_{O_HYS}			40		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 10 kHz		75		dB
Short Circuit to GND	I_{SC}			27		mA

ADR423 ELECTRICAL SPECIFICATIONS

@ V_{IN} = 5.0 V to 15.0 V, T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage, A Grade	V_O		2.996	3.000	3.004	V
Initial Accuracy	V_{OERR}		−4		+4	mV
			−0.13		+0.13	%
Output Voltage, B Grade	V_O		2.9985	3.000	3.0015	V
Initial Accuracy	V_{OERR}		−1.5		+1.5	mV
			−0.04		+0.04	%
Temperature Coefficient, A Grade	TCV_O	−40°C < TA < +125°C		2	10	ppm/°C
Temperature Coefficient, B Grade				1	3	ppm/°C
Supply Voltage Headroom	$V_{IN} - V_O$		2			V
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 5 V to 18 V		10	35	ppm/V
		−40°C < TA < +125°C				
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA			70	ppm/mA
		−40°C < TA < +125°C				
Quiescent Current	I_{IN}	No load		390	500	µA
		−40°C < TA < +125°C			600	µA
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_N	1 kHz		90		nV/√Hz
Turn-On Settling Time	t_R			10		µs
Long-Term Stability	ΔV_O	1,000 hours		50		ppm
Output Voltage Hysteresis	V_{O_HYS}			40		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 10 kHz		75		dB
Short Circuit to GND	I_{SC}			27		mA

ADR425 ELECTRICAL SPECIFICATIONS

@ V_{IN} = 7.0 V to 15.0 V, T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage, A Grade	V_O		4.994	5.000	5.006	V
Initial Accuracy	V_{OERR}		−6		+6	mV
			−0.12		+0.12	%
Output Voltage, B Grade	V_O		4.998	5.000	5.002	V
Initial Accuracy	V_{OERR}		−2		+2	mV
			−0.04		+0.04	%
Temperature Coefficient, A Grade	TCV_O	−40°C < TA < +125°C		2	10	ppm/°C
Temperature Coefficient, B Grade				1	3	ppm/°C
Supply Voltage Headroom	$V_{IN} - V_O$		2			V
Line Regulation	$\Delta V_O/\Delta V_{IN}$	V_{IN} = 7 V to 18 V		10	35	ppm/V
		−40°C < TA < +125°C				
Load Regulation	$\Delta V_O/\Delta I_{LOAD}$	I_{LOAD} = 0 mA to 10 mA			70	ppm/mA
		−40°C < TA < +125°C				
Quiescent Current	I_{IN}	No load		390	500	µA
		−40°C < TA < +125°C			600	µA
Voltage Noise	e_N p-p	0.1 Hz to 10 Hz		3.4		µV p-p
Voltage Noise Density	e_N	1 kHz		110		nV/√Hz
Turn-On Settling Time	t_R			10		µs
Long-Term Stability	ΔV_O	1,000 hours		50		ppm
Output Voltage Hysteresis	V_{O_HYS}			40		ppm
Ripple Rejection Ratio	RRR	f_{IN} = 10 kHz		75		dB
Short Circuit to GND	I_{SC}			27		mA

ABSOLUTE MAXIMUM RATINGS

These ratings apply at 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
Supply Voltage	18 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range R, RM Packages	−65°C to +150°C
Operating Temperature Range ADR42x	−40°C to +125°C
Junction Temperature Range R, RM Packages	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7.

Package Type	θ_{JA}[1]	Unit
8-Lead MSOP (RM)	190	°C/W
8-Lead SOIC (R)	130	°C/W

[1] θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for devices soldered in the circuit board for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

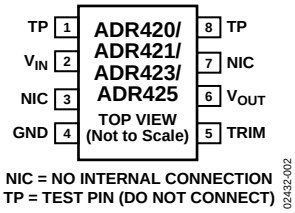


Figure 2. Pin Configuration for 8-Lead SOIC

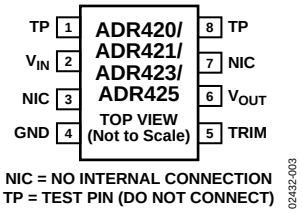


Figure 3. Pin Configuration for 8-Lead MSOP

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8	TP	Test Pin. There are actual connections in TP pins but they are reserved for factory testing purposes. Users should not connect anything to TP pins; otherwise, the device may not function properly.
2	V_{IN}	Input Voltage.
3, 7	NIC	No Internal Connect. NICs have no internal connections.
4	GND	Ground Pin = 0 V.
5	TRIM	Trim Terminal. It can be used to adjust the output voltage over a ±0.5% range without affecting the temperature coefficient.
6	V_{OUT}	Output Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

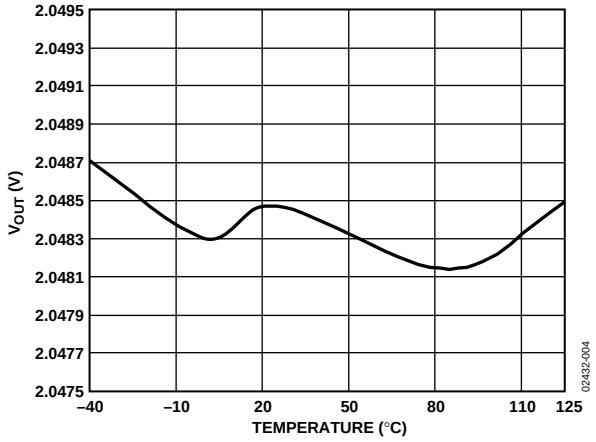


Figure 4. ADR420 Typical Output Voltage vs. Temperature

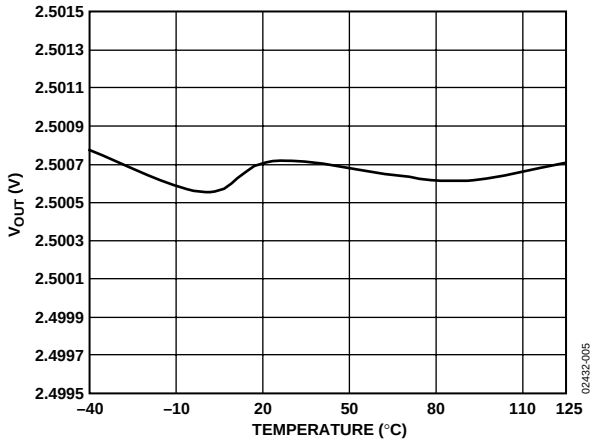


Figure 5. ADR421 Typical Output Voltage vs. Temperature

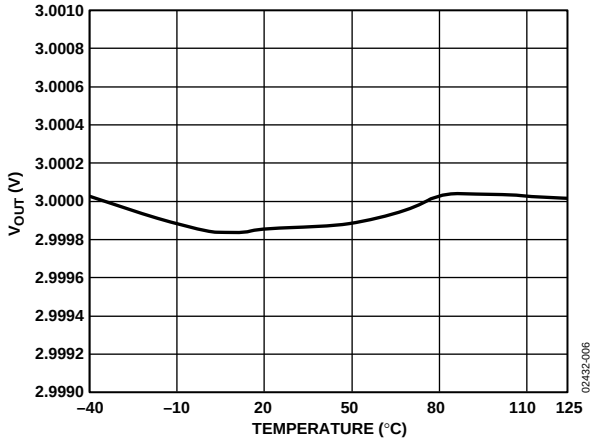


Figure 6. ADR423 Typical Output Voltage vs. Temperature

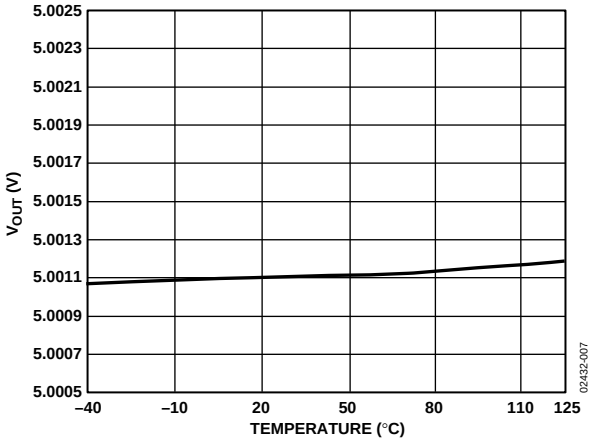


Figure 7. ADR425 Typical Output Voltage vs. Temperature

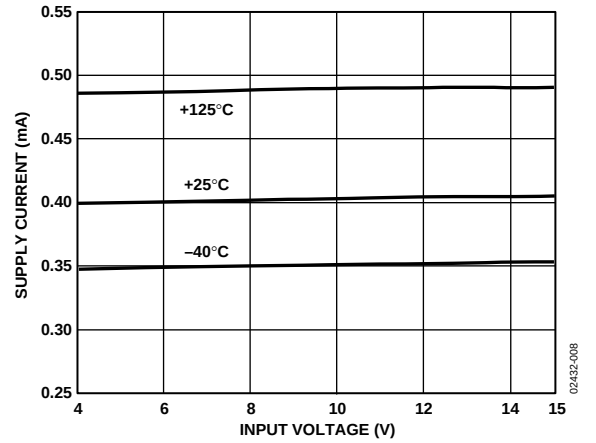


Figure 8. ADR420 Supply Current vs. Input Voltage

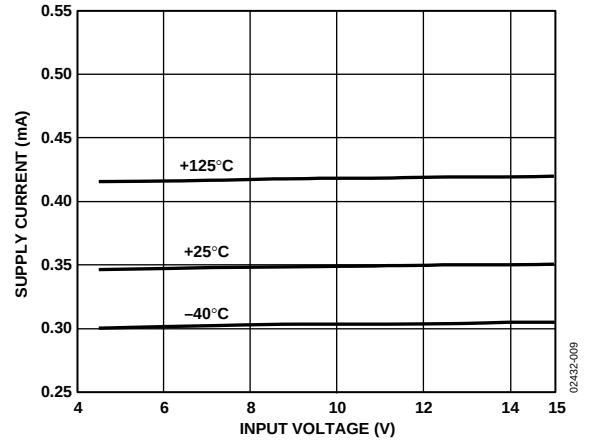


Figure 9. ADR421 Supply Current vs. Input Voltage

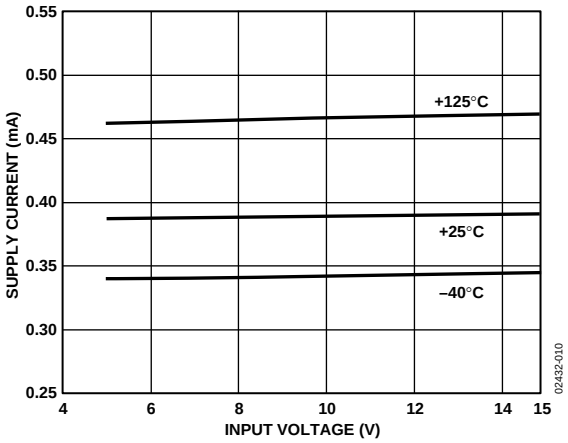


Figure 10. ADR423 Supply Current vs. Input Voltage

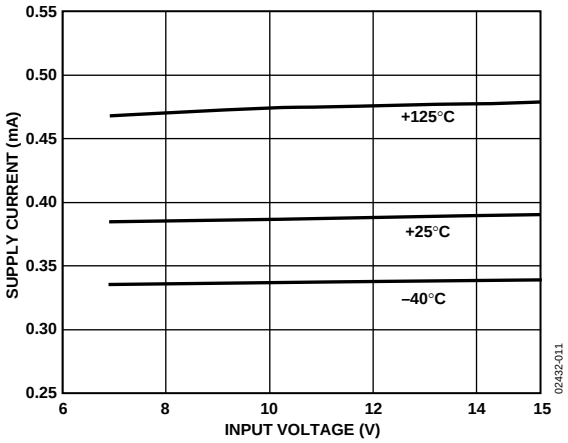


Figure 11. ADR425 Supply Current vs. Input Voltage

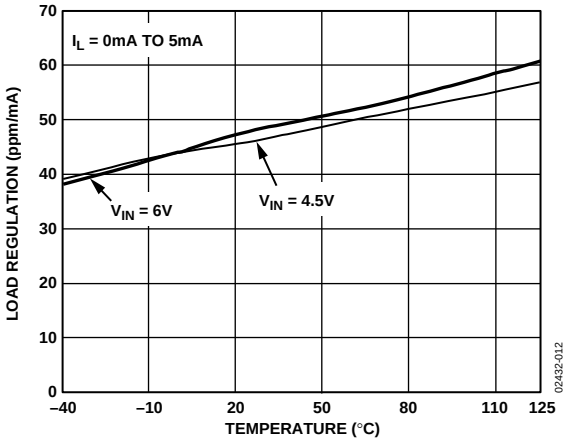


Figure 12. ADR420 Load Regulation vs. Temperature

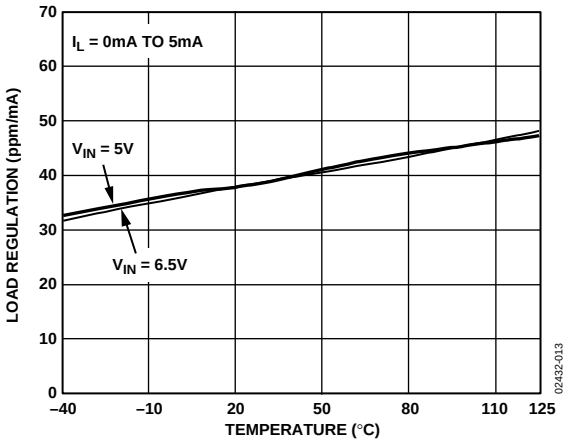


Figure 13. ADR421 Load Regulation vs. Temperature

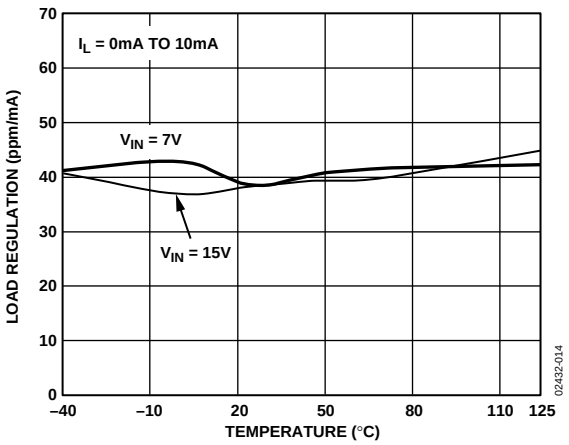


Figure 14. ADR423 Load Regulation vs. Temperature

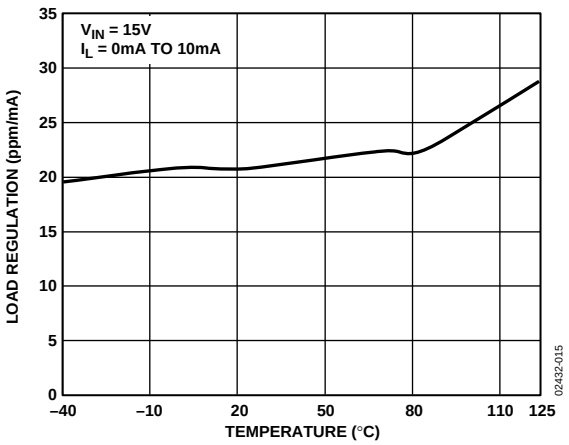


Figure 15. ADR425 Load Regulation vs. Temperature

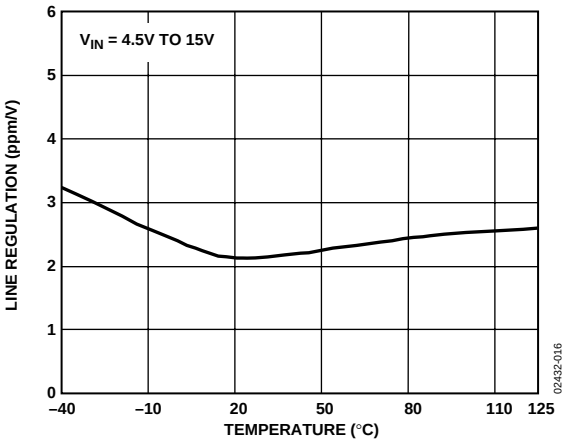


Figure 16. ADR420 Line Regulation vs. Temperature

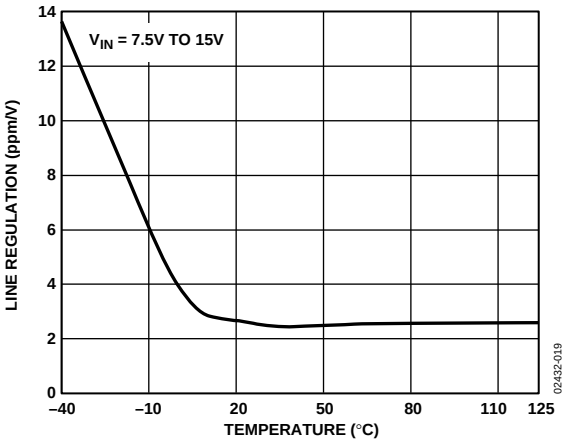


Figure 19. ADR425 Line Regulation vs. Temperature

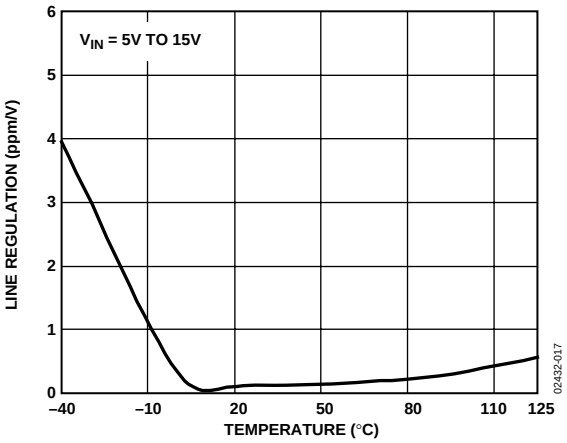


Figure 17. ADR421 Line Regulation vs. Temperature

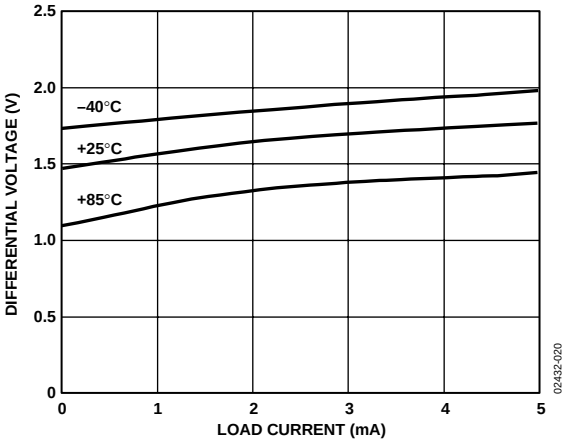


Figure 20. ADR420 Minimum Input/Output Voltage Differential vs. Load Current

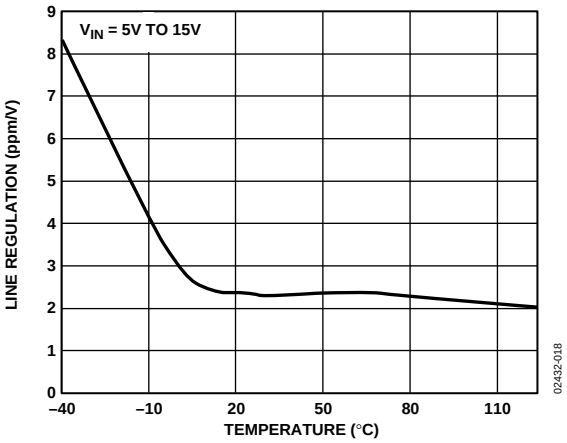


Figure 18. ADR423 Line Regulation vs. Temperature

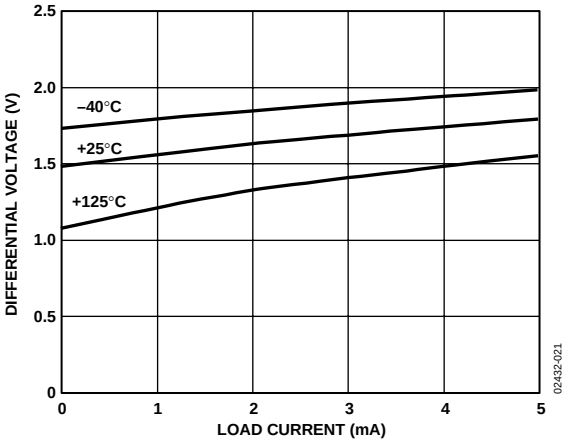


Figure 21. ADR421 Minimum Input/Output Voltage Differential vs. Load Current

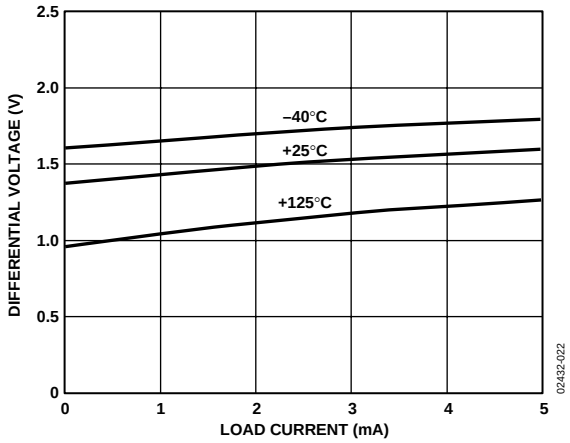


Figure 22. ADR423 Minimum Input/Output Voltage Differential vs. Load Current

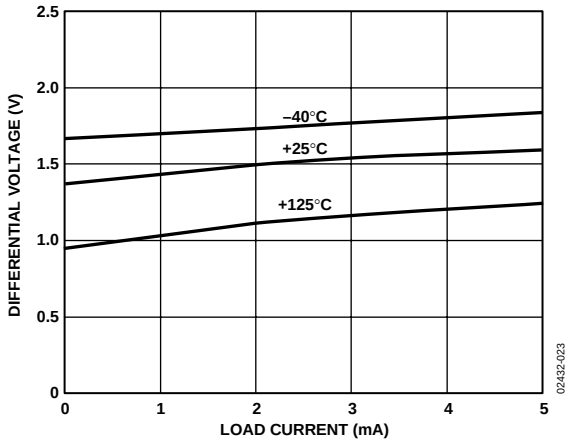


Figure 23. ADR425 Minimum Input/Output Voltage Differential vs. Load Current

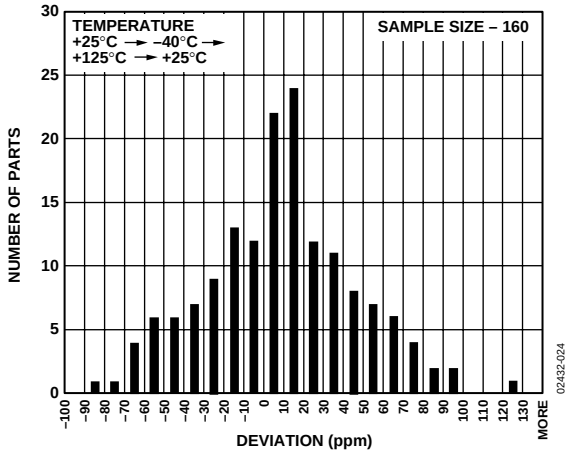


Figure 24. ADR421 Typical Hysteresis

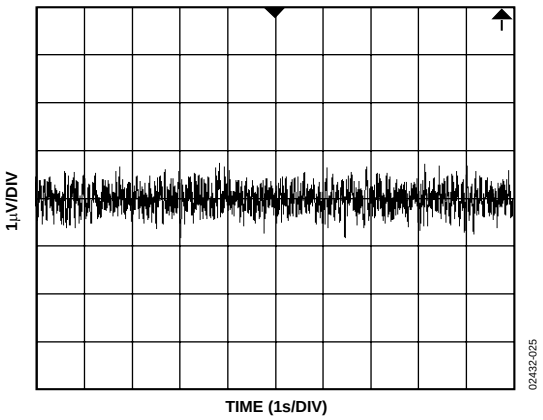


Figure 25. ADR421 Typical Noise Voltage 0.1 Hz to 10 Hz

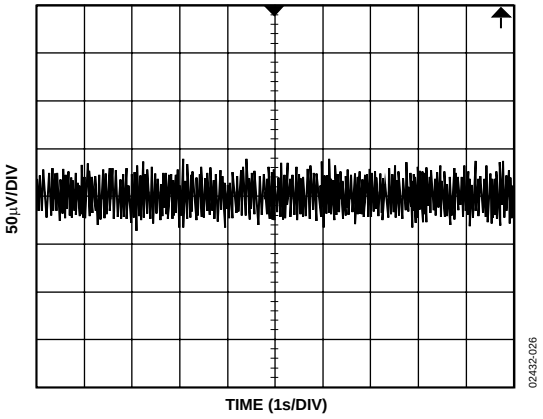


Figure 26. Typical Noise Voltage 10 Hz to 10 kHz

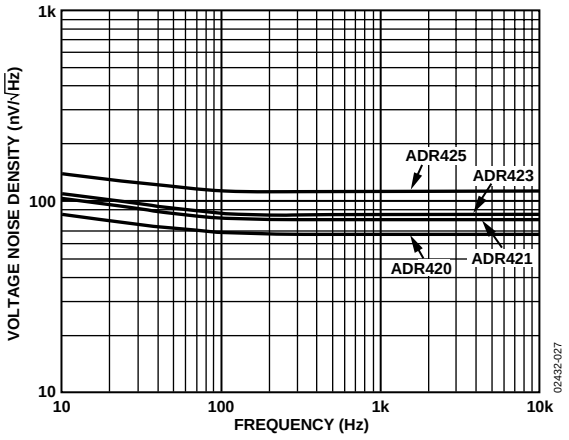


Figure 27. Voltage Noise Density vs. Frequency

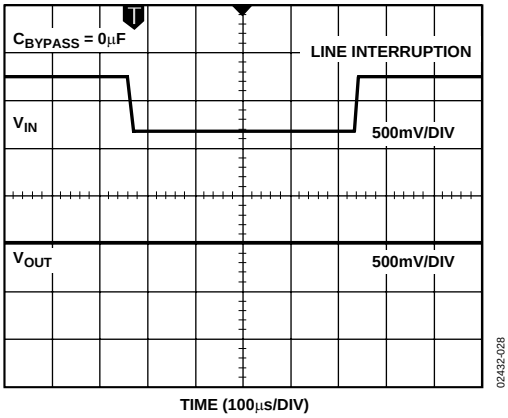


Figure 28. ADR421 Line Transient Response, no C_{BYPASS}

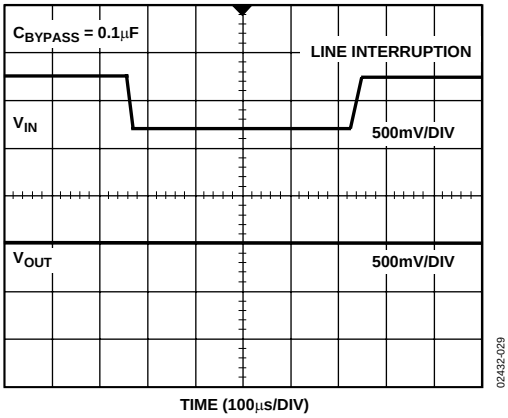


Figure 29. ADR421 Line Transient Response, C_{BYPASS} = 0.1 µF

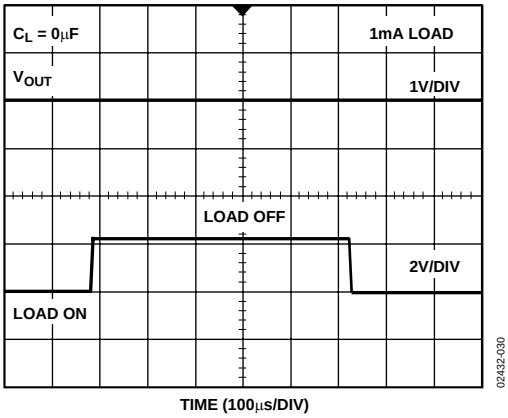


Figure 30. ADR421 Load Transient Response, no C_L

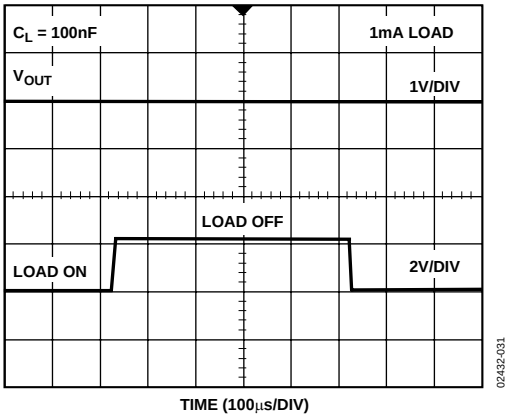


Figure 31. ADR421 Load Transient Response, CL = 100 nF

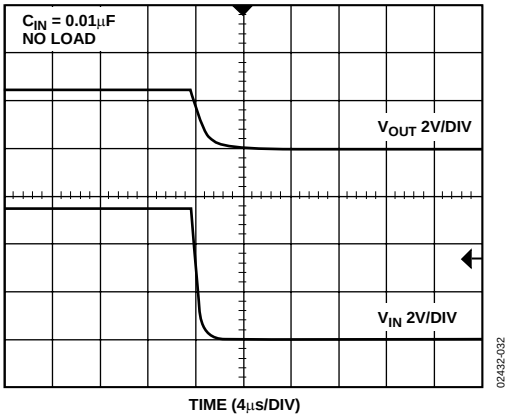


Figure 32. ADR421 Turn-Off Response

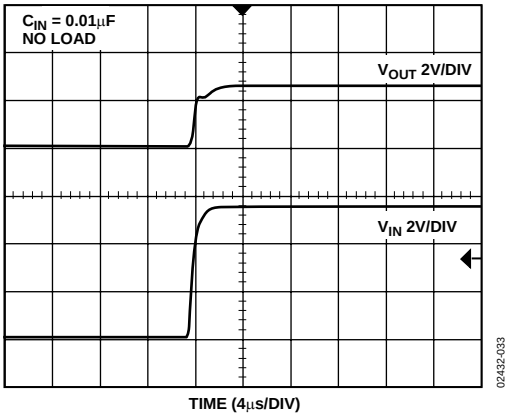


Figure 33. ADR421 Turn-On Response

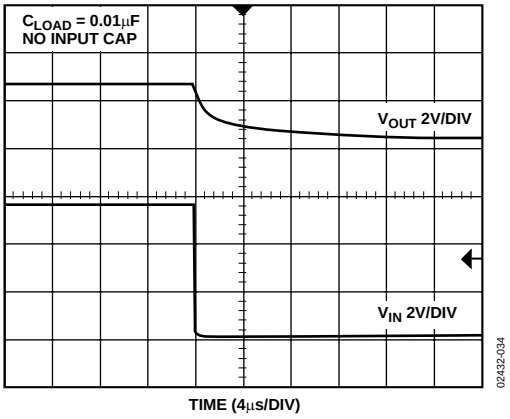


Figure 34. ADR421 Turn-Off Response

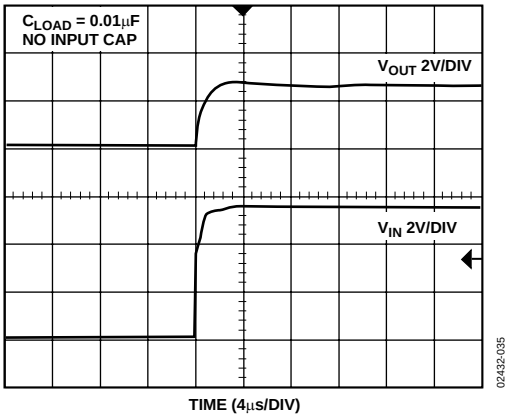


Figure 35. ADR421 Turn-On Response

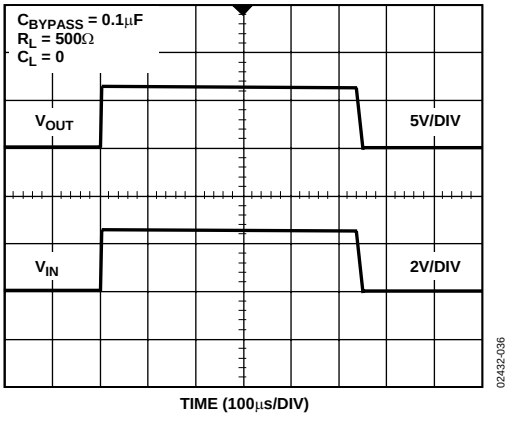


Figure 36. ADR421 Turn-On/Turn-Off Response

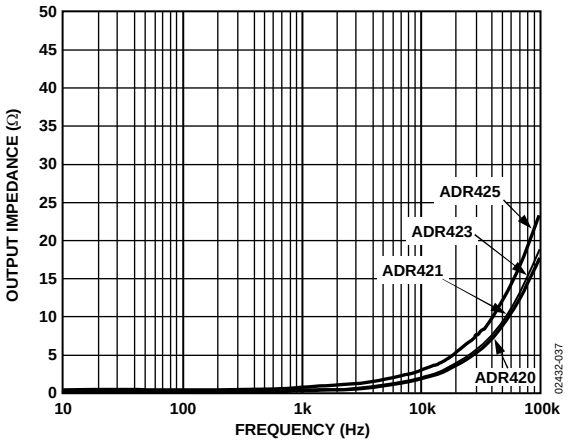


Figure 37. Output Impedance vs. Frequency

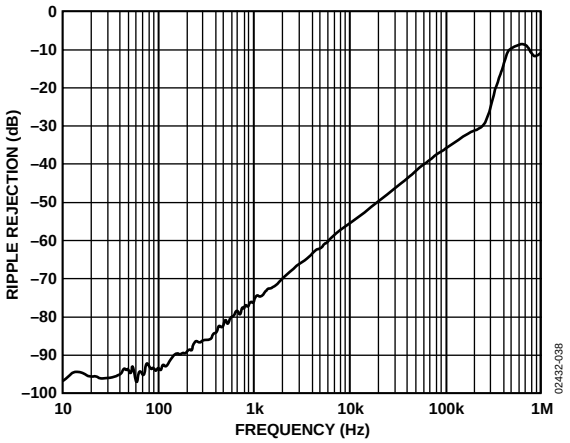


Figure 38. Ripple Rejection vs. Frequency

PARAMETER DEFINITIONS

Temperature Coefficient
The change of output voltage over the operating temperature range is normalized by the output voltage at 25°C, and expressed in ppm/°C as

$$TCV_O(ppm/°C) = \frac{V_O(T_2) - V_O(T_1)}{V_O(25°C) \times (T_2 - T_1)} \times 10^6$$

where:
V_O (25°C) = V_O at 25°C.
V_O (T_1) = V_O at Temperature 1.
V_O (T_2) = V_O at Temperature 2.

Line Regulation
The change in output voltage due to a specified change in input voltage. It includes the effects of self-heating. Line regulation is expressed in either percent-per-volt, parts-per-million per volt, or microvolts-per-volt change in input voltage.

Load Regulation
The change in output voltage due to a specified change in load current. It includes the effects of self-heating. Load regulation is expressed in either microvolts-per-milliampere, parts-per-million per milliampere, or ohms of dc output resistance.

Long-Term Stability
Typical shift of output voltage at 25°C on a sample of parts subjected to operation life test of 1,000 of hours at 125°C

$$\Delta V_O = V_O(t_0) - V_O(t_1)$$

$$\Delta V_O(ppm) = \frac{V_O(t_0) - V_O(t_1)}{V_O(t_0)} \times 10^6$$

where:
V_O (t_0) = V_O at 25°C at Time 0.
V_O (t_1) = V_O at 25°C after 1,000 hours operation at 125°C.

Thermal Hysteresis
The change of output voltage after the device is cycled through temperatures from +25°C to −40°C to +125°C and back to +25°C. This is a typical value from a sample of parts put through such a cycle

$$V_{O\_HYS} = V_O(25°C) - V_{O\_TC}$$

$$V_{O\_HYS}(ppm) = \frac{V_O(25°C) - V_{O\_TC}}{V_O(25°C)} \times 10^6$$

where:
V_O (25°C) = V_O at 25°C.
V_{O_TC} = V_O at 25 °C after temperature cycle at +25°C to −40°C to +125°C and back to +25°C.

Input Capacitor
Input capacitors are not required on the ADR42x. There is no limit for the value of the capacitor used on the input, but a 1 µF to 10 µF capacitor on the input improves transient response in applications where the supply suddenly changes. An additional 0.1 µF capacitor in parallel also helps to reduce noise from the supply.

Output Capacitor
The ADR42x do not need output capacitors for stability under any load condition. An output capacitor, typically 0.1 µF, filters out any low level noise voltage and does not affect the operation of the part. On the other hand, the load transient response can be improved with an additional 1 µF to 10 µF output capacitor in parallel. A capacitor here acts as a source of stored energy for sudden increase in load current. The only parameter that degrades by adding an output capacitor is the turn-on time, and it depends on the size of the selected capacitor.

THEORY OF OPERATION

The ADR42x series of references uses a new reference generation technique known as XFET (eXtra implanted junction FET). This technique yields a reference with low supply current, good thermal hysteresis, and exceptionally low noise. The core of the XFET reference consists of two junction field-effect transistors (JFET), one having an extra channel implant to raise its pinch-off voltage. By running the two JFETs at the same drain current, the difference in pinch-off voltage can be amplified and used to form a highly stable voltage reference.

The intrinsic reference voltage is about 0.5 V with a negative temperature coefficient of about −120 ppm/°C. This slope is essentially constant to the dielectric constant of silicon and can be closely compensated by adding a correction term generated in the same fashion as the proportional-to-temperature (PTAT) term used to compensate band gap references. The primary advantage over a band gap reference is that the intrinsic temperature coefficient is approximately 30 times lower (therefore requiring less correction). This results in much lower noise because most of the noise of a band gap reference comes from the temperature compensation circuitry.

Figure 39 shows the basic topology of the ADR42x series. The temperature correction term is provided by a current source with a value designed to be proportional to absolute temperature. The general equation is

$$V_{OUT} = G \times (\Delta V_P - R1 \times I_{PTAT}) \quad (1)$$

where:
G is the gain of the reciprocal of the divider ratio.
ΔV_P is the difference in pinch-off voltage between the two JFETs.
I_{PTAT} is the positive temperature coefficient correction current.

ADR42x are created by on-chip adjustment of R2 and R3 to achieve 2.048 V or 2.500 V at the reference output, respectively.

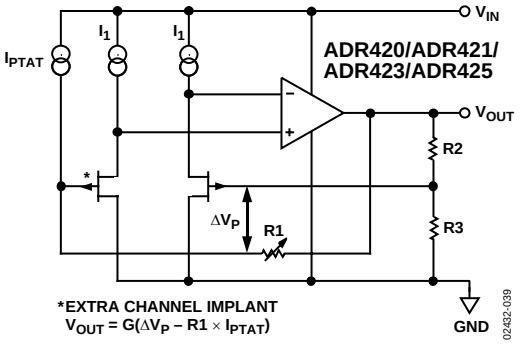


Figure 39. Simplified Schematic

DEVICE POWER DISSIPATION CONSIDERATIONS

The ADR42x family of references is guaranteed to deliver load currents to 10 mA with an input voltage that ranges from 4.5 V to 18 V. When these devices are used in applications at higher currents, the following equation should be used to account for the temperature effects due to power dissipation increases:

$$T_J = P_D \times \theta_{JA} + T_A \quad (2)$$

where:
T_J and T_A are the junction and ambient temperatures, respectively.
P_D is the device power dissipation.
θ_{JA} is the device package thermal resistance.

BASIC VOLTAGE REFERENCE CONNECTIONS

Voltage references, in general, require a bypass capacitor connected from V_{OUT} to GND. The circuit in Figure 40 illustrates the basic configuration for the ADR42x family of references. Other than a 0.1 μF capacitor at the output to help improve noise suppression, a large output capacitor at the output is not required for circuit stability.

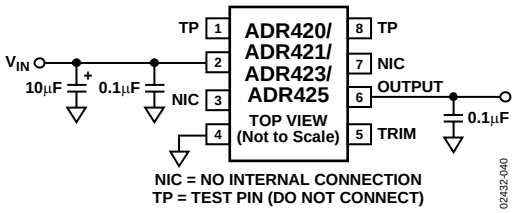


Figure 40. Basic Voltage Reference Configuration

NOISE PERFORMANCE

The noise generated by ADR42x references is typically less than 2 μV p-p over the 0.1 Hz to 10 Hz band for the ADR420, ADR421, and ADR423. Figure 25 shows the 0.1 Hz to 10 Hz noise of the ADR421, which is only 1.75 μV p-p. The noise measurement is made with a band-pass filter made of a 2-pole high-pass filter with a corner frequency at 0.1 Hz and a 2-pole low-pass filter with a corner frequency at 10 Hz.

TURN-ON TIME

At power-up (cold start), the time required for the output voltage to reach its final value within a specified error band is defined as the turn-on settling time. Two components typically associated with this are the time for the active circuits to settle and the time for the thermal gradients on the chip to stabilize. Figure 32 to Figure 36 show the turn-on settling time for the ADR421.

APPLICATIONS

OUTPUT ADJUSTMENT

The ADR42x trim terminal can be used to adjust the output voltage over a ±0.5% range. This feature allows the system designer to trim system errors out by setting the reference to a voltage other than the nominal. This is also helpful if the part is used in a system at temperature to trim out any error. Adjustment of the output has a negligible effect on the temperature performance of the device. To avoid degrading temperature coefficients, both the trimming potentiometer and the two resistors need to be low temperature coefficient types, preferably <100 ppm/°C.

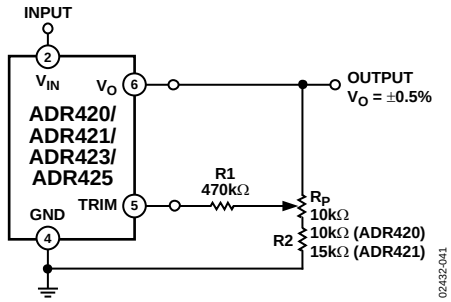


Figure 41. Output Trim Adjustment

REFERENCE FOR CONVERTERS IN OPTICAL NETWORK CONTROL CIRCUITS

In the high capacity, all-optical router network of Figure 42, arrays of micromirrors direct and route optical signals from fiber to fiber, without first converting them to electrical form, which reduces the communication speed. The tiny micro-mechanical mirrors are positioned so that each is illuminated by a single wave length that carries unique information and can be passed to any desired input and output fiber. The mirrors are tilted by the dual-axis actuators controlled by precision analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) within the system. Due to the microscopic movement of the mirrors, not only is the precision of the converters important, but the noise associated with these controlling converters is extremely critical, because total noise within the system can be multiplied by the numbers of converters used. Consequently, the exceptional low noise of the ADR42x is necessary to maintain the stability of the control loop for this application.

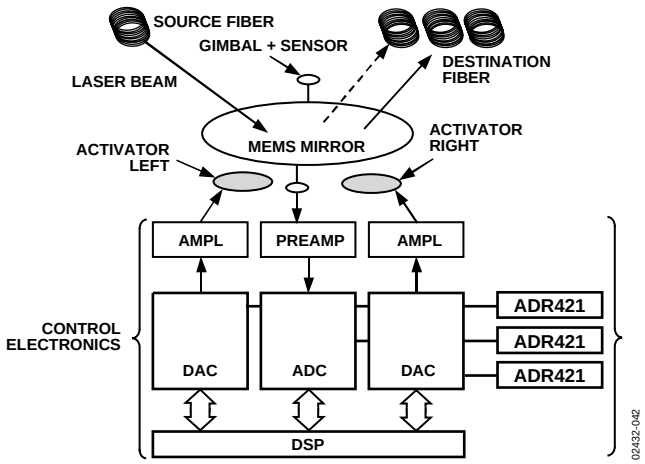


Figure 42. All-Optical Router Network

A NEGATIVE PRECISION REFERENCE WITHOUT PRECISION RESISTORS

In many current-output CMOS DAC applications where the output signal voltage must be of the same polarity as the reference voltage, a current-switching DAC is often reconfigured into a voltage-switching DAC with a 1.25 V reference, an op amp, a pair of resistors, and an additional operational amplifier at the output to reinvert the signal. A negative voltage reference should be used because an additional operational amplifier is not required for either reinversion (current-switching mode) or amplification (voltage-switching mode) of the DAC output voltage. In general, any positive voltage reference can be converted into a negative voltage reference through the use of an operational amplifier and a pair of matched resistors in an inverting configuration. The disadvantage to this approach is that the largest single source of error in the circuit is the relative matching of the resistors used.

A negative reference can easily be generated by adding a precision op amp and configuring as shown in Figure 43. V_{OUT} is at virtual ground and, therefore, the negative reference can be taken directly from the output of the op amp. The op amp must be dual-supply, low offset and have rail-to-rail capability if negative supply voltage is close to the reference output.

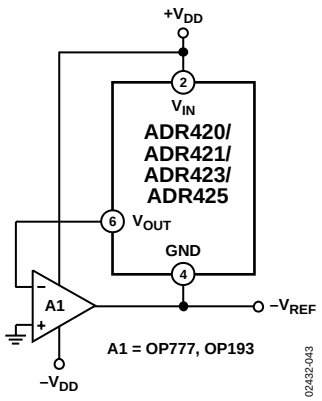


Figure 43. Negative Reference

HIGH VOLTAGE FLOATING CURRENT SOURCE

The circuit in Figure 44 can be used to generate a floating current source with minimal self-heating. This particular configuration can operate on high supply voltages determined by the breakdown voltage of the N-channel JFET.

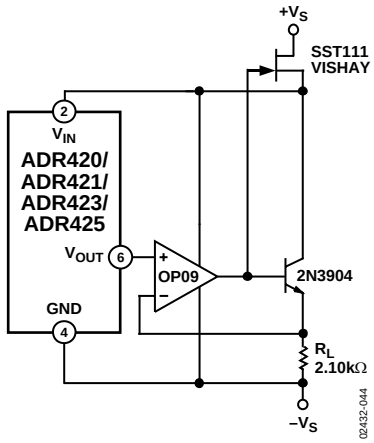


Figure 44. High Voltage Floating Current Source

KELVIN CONNECTIONS

In many portable instrumentation applications where PC board cost and area are important considerations, circuit interconnects are often narrow. These narrow lines can cause large voltage drops if the voltage reference is required to provide load currents to various functions. In fact, a circuit's interconnects can exhibit a typical line resistance of 0.45 mΩ/square (1 oz. Cu, for example). Force and sense connections, also referred to as Kelvin connections, offer a convenient method of eliminating the effects of voltage drops in circuit wires. Load currents flowing through wiring resistance produce an error ($V_{ERROR} = R \times I_L$) at the load. However, the Kelvin connection in Figure 45 overcomes the problem by including the wiring resistance within the forcing loop of the op amp. Because the op amp senses the load voltage, op amp loop control forces the output to compensate for the wiring error and to produce the correct voltage at the load.

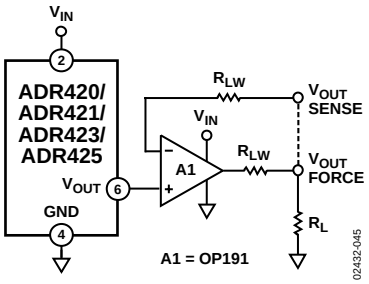


Figure 45. Advantage of Kelvin Connection

DUAL-POLARITY REFERENCES

Dual-polarity references can easily be made with an op amp and a pair of resistors. In order not to defeat the accuracy obtained by the ADR42x, it is imperative to match the resistance tolerance and the temperature coefficient of all components.

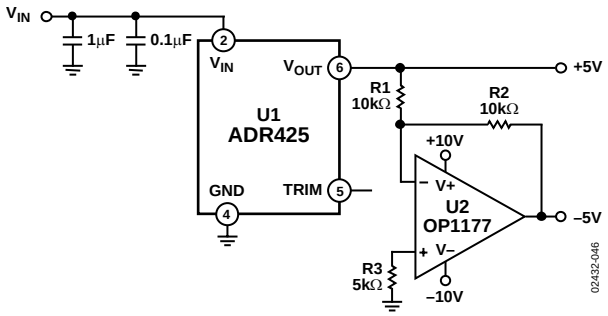


Figure 46. +5 V and –5 V Reference Using ADR425

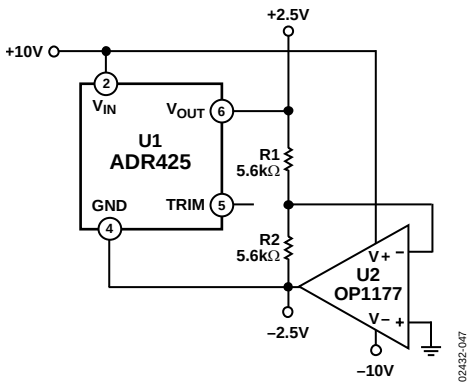


Figure 47. +2.5 V and –2.5 V Reference Using ADR425

PROGRAMMABLE CURRENT SOURCE

Together with a digital potentiometer and a Howland current pump, the ADR425 forms the reference source for a programmable current as

$$I_L = \frac{\left(\frac{R2_A + R2_B}{R1}\right)}{R2_B} \times V_W \quad (3)$$

and

$$VW = \frac{D}{2^N} \times V_{REF} \quad (4)$$

where:
D = Decimal equivalent of the input code.
N = Number of bits.

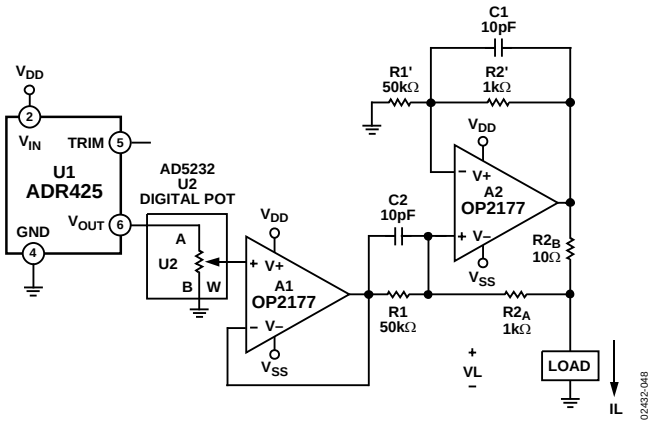


Figure 48. Programmable Current Source

R1' and R2' must be equal to R1 and $R2_A + R2_B$, respectively. Theoretically, $R2_B$ can be made as small as needed to achieve the current needed within A2 output current driving capability. In the example shown in Figure 48, OP2177 is able to deliver a maximum of 10 mA. Because the current pump uses both positive and negative feedback, Capacitors C1 and C2 are needed to ensure that negative feedback prevails and, therefore, avoids oscillation. This circuit also allows bidirectional current flow if the inputs V_A and V_B of the digital potentiometer are supplied with the dual-polarity references as previously shown.

PROGRAMMABLE DAC REFERENCE VOLTAGE

With a multichannel DAC, such as the quad, 12-bit voltage output AD7398, one of its internal DACs, and an ADR42x voltage reference can be used as a common programmable V_{REFX} for the rest of the DACs. The circuit configuration is shown in Figure 49. The relationship of V_{REFX} to V_{REF} depends on the digital code and the ratio of R1 and R, and is given by

$$V_{REFX} = \frac{V_{REF} \times \left(1 + \frac{R2}{R1}\right)}{\left(1 + \frac{D}{2^N} \times \frac{R2}{R1}\right)} \quad (5)$$

where:
D = Decimal equivalent of input code.
N = Number of bits.
V_{REF} = Applied external reference.
V_{REFX} = Reference voltage for DACs A to D.

Table 9. V_{REFX} vs. R1 and R2

R1, R2	Digital Code	V_{REF}
R1 = R2	0000 0000 0000	2 V_{REF}
R1 = R2	1000 0000 0000	1.3 V_{REF}
R1 = R2	1111 1111 1111	V_{REF}
R1 = 3R2	0000 0000 0000	4 V_{REF}
R1 = 3R2	1000 0000 0000	1.6 V_{REF}
R1 = 3R2	1111 1111 1111	V_{REF}

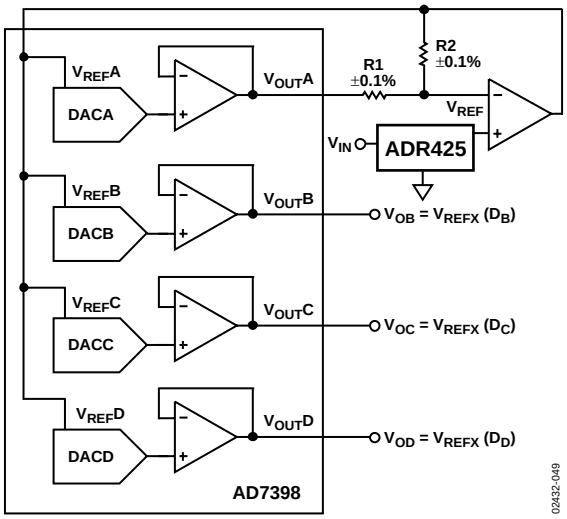


Figure 49. Programmable DAC Reference

PRECISION VOLTAGE REFERENCE FOR DATA CONVERTERS

The ADR42x family has a number of features that make it ideal for use with ADCs and DACs. The exceptionally low noise, tight temperature coefficient, and high accuracy characteristics make the ADR42x ideal for low noise applications such as cellular base station applications.

AD7701 is an example of an ADC that is well suited for the ADR42x. The ADR421 is used as the precision reference for the converter in Figure 50. The AD7701 is a 16-bit ADC with on-chip digital filtering intended for measuring wide dynamic range and low frequency signals, such as those representing chemical, physical, or biological processes. It contains a charge-balancing (Σ-Δ) ADC, calibration microcontroller with on-chip static RAM, clock oscillator, and serial communications port.

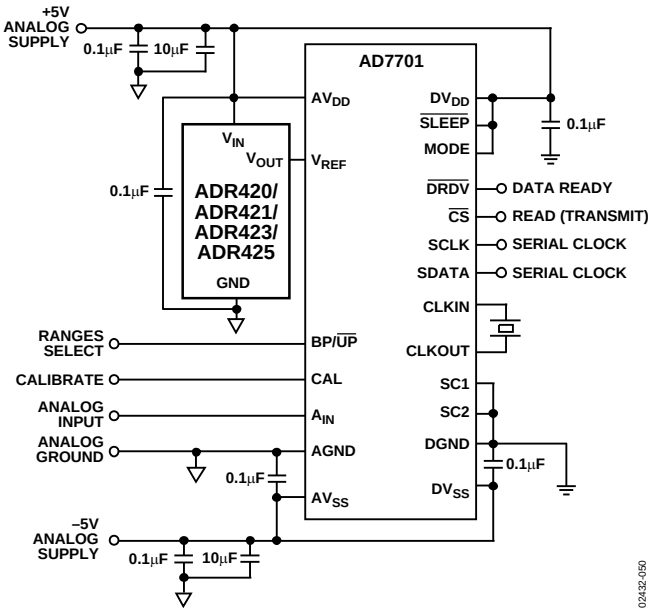


Figure 50. Voltage Reference for 16-Bit ADC AD7701

PRECISION BOOSTED OUTPUT REGULATOR

A precision voltage output with boosted current capability can be realized with the circuit shown in Figure 51. In this circuit, U2 forces V_O to be equal to V_{REF} by regulating the turn on of N1. Therefore, the load current is furnished by V_{IN}. In this configuration, a 50 mA load is achievable at V_{IN} of 5 V. Moderate heat is generated on the MOSFET, and higher current can be achieved by replacing the larger device. In addition, for a heavy capacitive load with step input, a buffer may be added at the output to enhance the transient response.

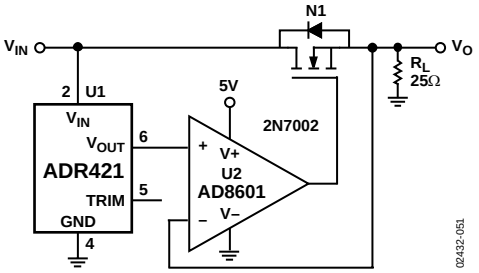
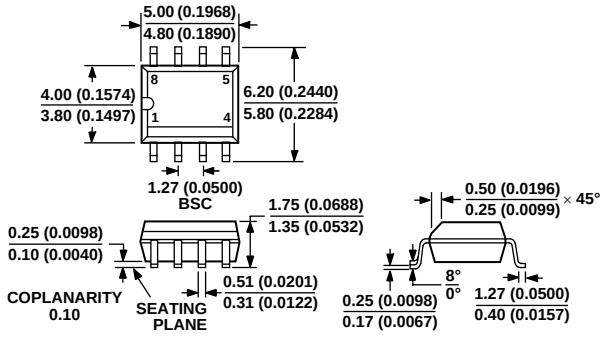


Figure 51. Precision Boosted Output Regulator

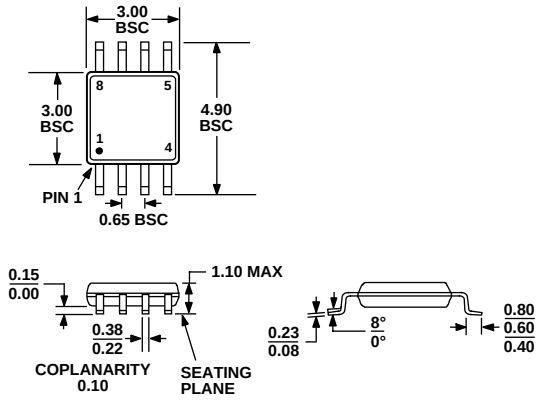
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 52. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 53. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temp Range (°C)	Package Description	Package Option	Top Mark	Output Voltage (V_O)	Initial Accuracy mV	Initial Accuracy %	Temp Co. (ppm/°C)
ADR420AR	−40 to +125	SOIC_N	R-8	ADR420	2.048	3	0.15	10
ADR420AR-REEL7	−40 to +125	SOIC_N	R-8	ADR420	2.048	3	0.15	10
ADR420ARZ[1]	−40 to +125	SOIC_N	R-8	ADR420	2.048	3	0.15	10
ADR420ARZ-REEL7[1]	−40 to +125	SOIC_N	R-8	ADR420	2.048	3	0.15	10
ADR420ARM	−40 to +125	MSOP	RM-8	R4A	2.048	3	0.15	10
ADR420ARM-REEL7	−40 to +125	MSOP	RM-8	R4A	2.048	3	0.15	10
ADR420ARMZ[1]	−40 to +125	MSOP	RM-8	L0C	2.048	3	0.15	10
ADR420ARMZ-REEL7[1]	−40 to +125	MSOP	RM-8	L0C	2.048	3	0.15	10
ADR420BR	−40 to +125	SOIC_N	R-8	ADR420	2.048	1	0.05	3
ADR420BR-REEL7	−40 to +125	SOIC_N	R-8	ADR420	2.048	1	0.05	3
ADR420BRZ[1]	−40 to +125	SOIC_N	R-8	ADR420	2.048	1	0.05	3
ADR420BRZ-REEL7[1]	−40 to +125	SOIC_N	R-8	ADR420	2.048	1	0.05	3
ADR421AR	−40 to +125	SOIC_N	R-8	ADR421	2.50	3	0.12	10
ADR421AR-REEL7	−40 to +125	SOIC_N	R-8	ADR421	2.50	3	0.12	10
ADR421ARZ[1]	−40 to +125	SOIC_N	R-8	ADR421	2.50	3	0.12	10
ADR421ARZ-REEL7[1]	−40 to +125	SOIC_N	R-8	ADR421	2.50	3	0.12	10
ADR421ARM	−40 to +125	MSOP	RM-8	R5A	2.50	3	0.12	10
ADR421ARM-REEL7	−40 to +125	MSOP	RM-8	R5A	2.50	3	0.12	10
ADR421ARMZ[1]	−40 to +125	MSOP	RM-8	R06	2.50	3	0.12	10
ADR421ARMZ-REEL7[1]	−40 to +125	MSOP	RM-8	R06	2.50	3	0.12	10
ADR421BR	−40 to +125	SOIC_N	R-8	ADR421	2.50	1	0.04	3
ADR421BR-REEL7	−40 to +125	SOIC_N	R-8	ADR421	2.50	1	0.04	3
ADR421BRZ[1]	−40 to +125	SOIC_N	R-8	ADR421	2.50	1	0.04	3
ADR421BRZ-REEL7[1]	−40 to +125	SOIC_N	R-8	ADR421	2.50	1	0.04	3
ADR423AR	−40 to +125	SOIC_N	R-8	ADR423	3.00	4	0.13	10
ADR423AR-REEL7	−40 to +125	SOIC_N	R-8	ADR423	3.00	4	0.13	10
ADR423ARZ[1]	−40 to +125	SOIC_N	R-8	ADR423	3.00	4	0.13	10
ADR423ARZ-REEL7[1]	−40 to +125	SOIC_N	R-8	ADR423	3.00	4	0.13	10
ADR423ARM	−40 to +125	MSOP	RM-8	R6A	3.00	4	0.13	10
ADR423ARM-REEL7	−40 to +125	MSOP	RM-8	R6A	3.00	4	0.13	10
ADR423BR	−40 to +125	SOIC_N	R-8	ADR423	3.00	1.5	0.04	3
ADR423BR-REEL7	−40 to +125	SOIC_N	R-8	ADR423	3.00	1.5	0.04	3
ADR423ARMZ[1]	−40 to +125	MSOP	RM-8	R0U	3.00	4	0.13	10
ADR423ARMZ-REEL7[1]	−40 to +125	MSOP	RM-8	R0U	3.00	4	0.13	10
ADR423BRZ[1]	−40 to +125	SOIC_N	R-8	ADR423	3.00	1.5	0.04	3
ADR423BRZ-REEL7[1]	−40 to +125	SOIC_N	R-8	ADR423	3.00	1.5	0.04	3
ADR425AR	−40 to +125	SOIC_N	R-8	ADR425	5.00	6	0.12	10
ADR425AR-REEL7	−40 to +125	SOIC_N	R-8	ADR425	5.00	6	0.12	10
ADR425ARZ[1]	−40 to +125	SOIC_N	R-8	ADR425	5.00	6	0.12	10
ADR425ARZ-REEL7[1]	−40 to +125	SOIC_N	R-8	ADR425	5.00	6	0.12	10
ADR425ARM	−40 to +125	MSOP	RM-8	R7A	5.00	6	0.12	10
ADR425ARM-REEL7	−40 to +125	MSOP	RM-8	R7A	5.00	6	0.12	10
ADR425ARMZ[1]	−40 to +125	MSOP	RM-8	R0V	5.00	6	0.12	10
ADR425ARMZ-REEL7[1]	−40 to +125	MSOP	RM-8	R0V	5.00	6	0.12	10
ADR425BR	−40 to +125	SOIC_N	R-8	ADR425	5.00	2	0.04	3
ADR425BR-REEL7	−40 to +125	SOIC_N	R-8	ADR425	5.00	2	0.04	3
ADR425BRZ[1]	−40 to +125	SOIC_N	R-8	ADR425	5.00	2	0.04	3
ADR425BRZ-REEL7[1]	−40 to +125	SOIC_N	R-8	ADR425	5.00	2	0.04	3

[1] Z = Pb-free part.

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