

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM6P36TU

○ Power Management Switches

- 1.5-V drive
- Low ON-resistance: $R_{on} = 3.60 \Omega$ (max) (@ $V_{GS} = -1.5$ V)
: $R_{on} = 2.70 \Omega$ (max) (@ $V_{GS} = -1.8$ V)
: $R_{on} = 1.60 \Omega$ (max) (@ $V_{GS} = -2.8$ V)
: $R_{on} = 1.31 \Omega$ (max) (@ $V_{GS} = -4.5$ V)

Absolute Maximum Ratings (Ta = 25 °C)

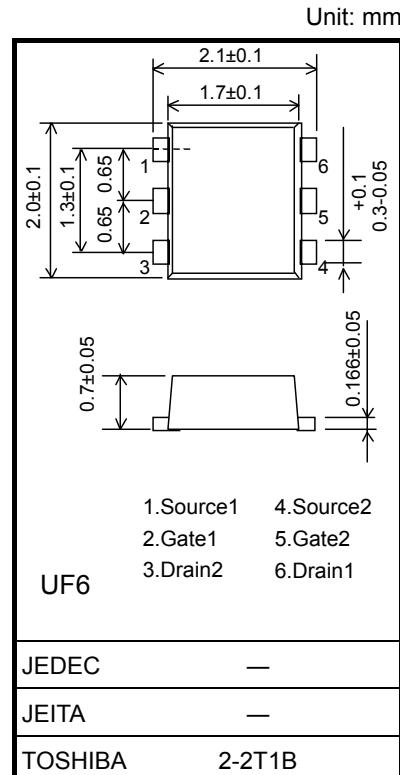
Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	-20	V
Gate-source voltage	V_{GSS}	± 8	V
Drain current	DC	I_D	mA
	Pulse	I_{DP}	
Drain power dissipation	P_D (Note1)	500	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

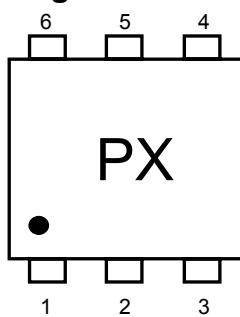
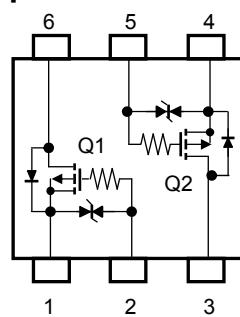
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: Total rating

Mounted on an FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm²)



Weight: 7.0 mg (typ.)

Marking**Equivalent Circuit (top view)****Handling Precaution**

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Usage Considerations

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below -1 mA for the SSM6P36TU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device.

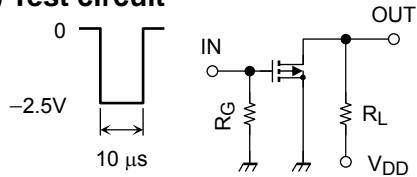
Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage	V (BR) DSS	Id = -1 mA, VGS = 0 V	-20	—	—	V
	V (BR) DSX	Id = -1 mA, VGS = 8 V	-12	—	—	
Drain cutoff current	IdSS	VDS = -16 V, VGS = 0 V	—	—	-10	μA
Gate leakage current	IGSS	VGS = ±8 V, VDS = 0 V	—	—	±1	μA
Gate threshold voltage	Vth	VDS = -3 V, Id = -1 mA	-0.3	—	-1.0	V
Forward transfer admittance	Yfs	VDS = -3 V, Id = -100mA (Note2)	190	—	—	mS
Drain-source ON-resistance	RDS (ON)	Id = -100mA, VGS = -4.5 V (Note2)	—	0.95	1.31	Ω
		Id = -80mA, VGS = -2.8 V (Note2)	—	1.22	1.60	
		Id = -40mA, VGS = -1.8 V (Note2)	—	1.80	2.70	
		Id = -30mA, VGS = -1.5 V (Note2)	—	2.23	3.60	
Input capacitance	Ciss	VDS = -10 V, VGS = 0 V, f = 1 MHz	—	43	—	pF
Output capacitance	Coss		—	10.3	—	
Reverse transfer capacitance	Crss		—	6.1	—	
Total Gate Charge	Qg	VDS = -10 V, Id = -330mA VGS = -4 V	—	1.2	—	nC
Gate-Source Charge	Qgs		—	0.85	—	
Gate-Drain Charge	Qgd		—	0.35	—	
Switching time	Turn-on time	t _{on}	VDD = -10 V, Id = -100mA VGS = 0 to -2.5 V, RG = 50Ω	—	90	ns
	Turn-off time	t _{off}		—	200	
Drain-source forward voltage	V _{DSF}	Id = 330mA, VGS = 0 V (Note2)	—	0.88	1.2	V

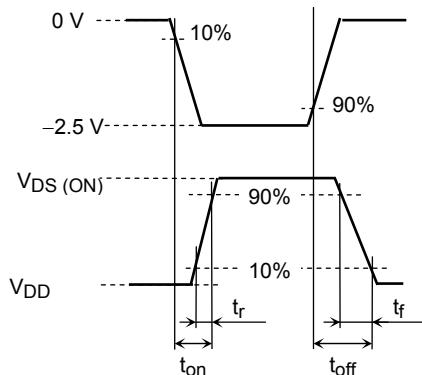
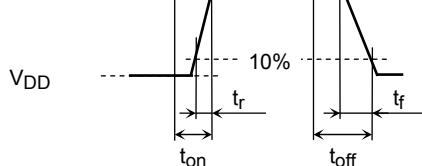
Note2: Pulse test

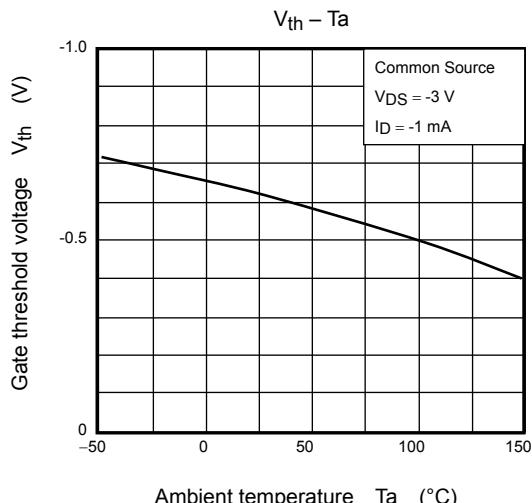
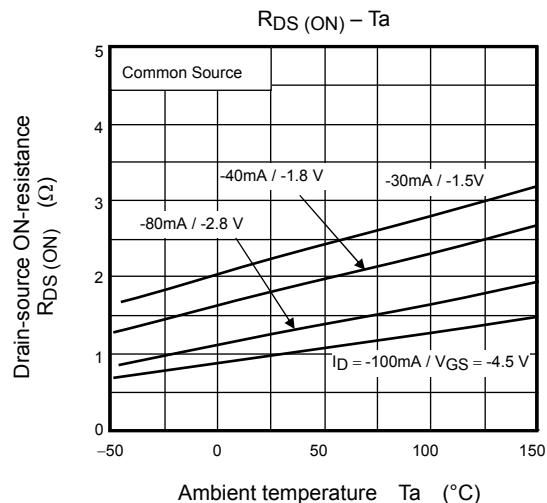
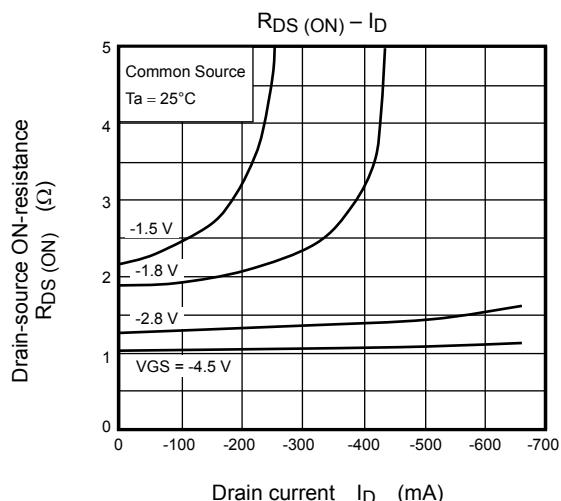
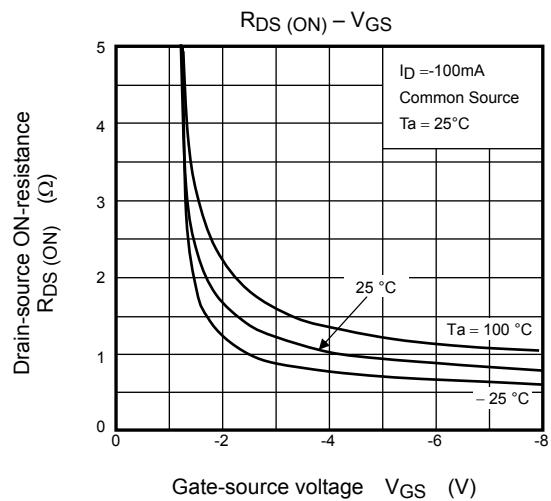
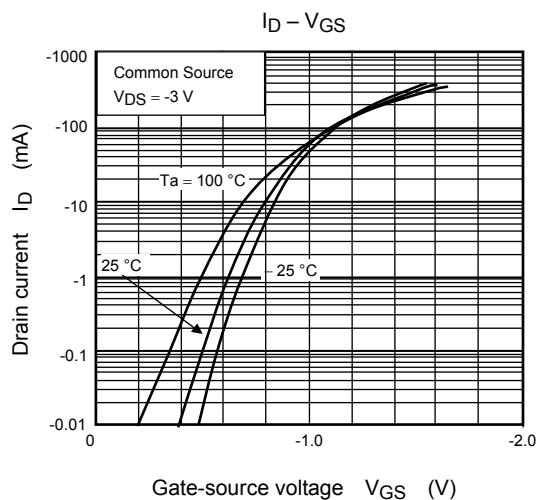
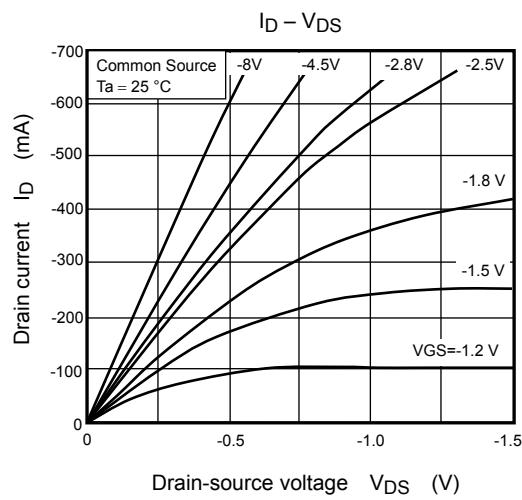
Switching Time Test Circuit

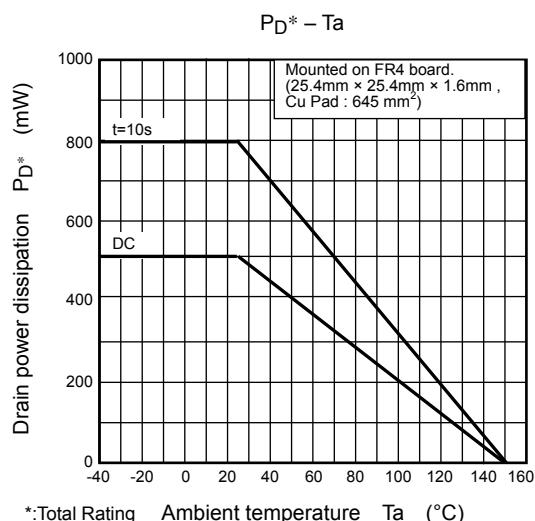
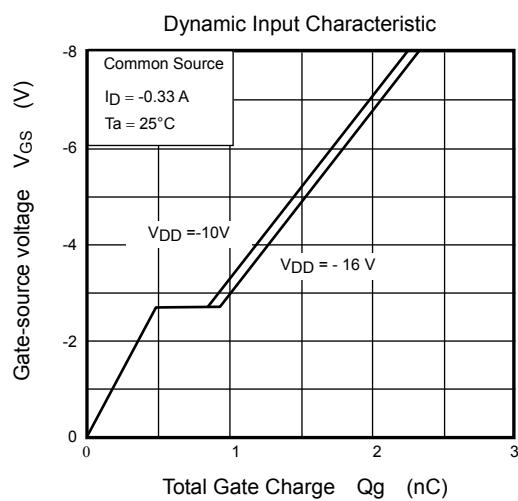
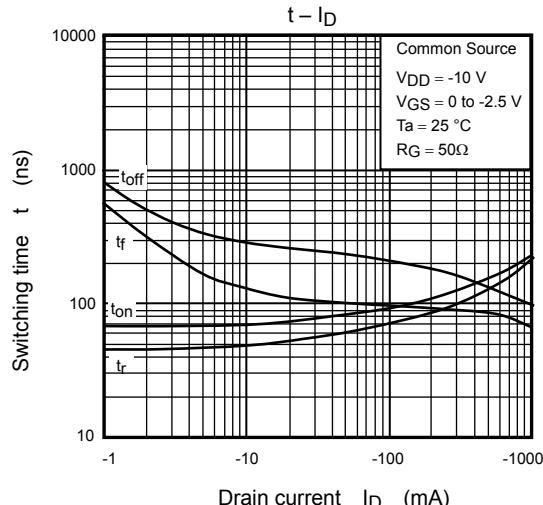
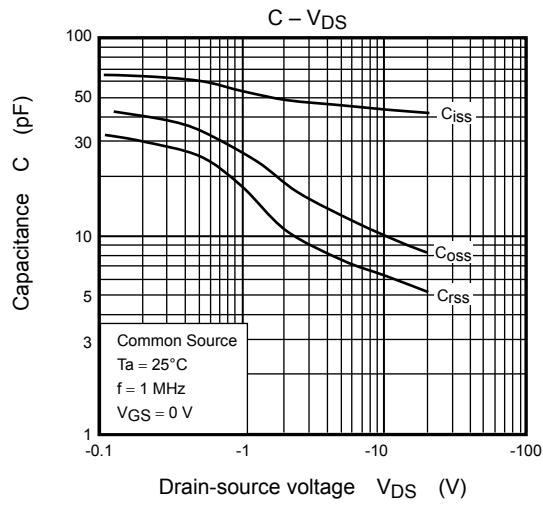
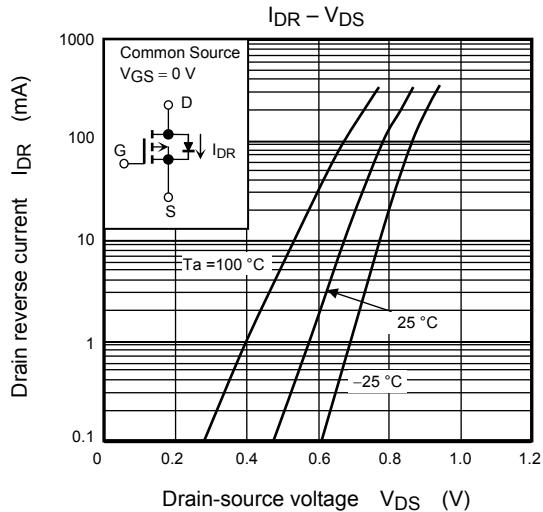
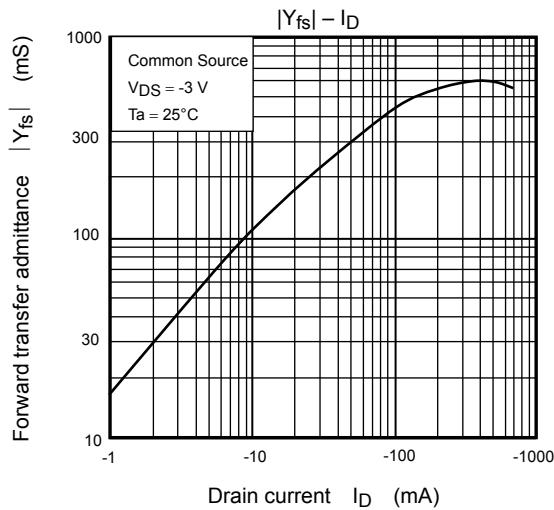
(a) Test circuit



$V_{DD} = -10 \text{ V}$
 Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5 \text{ ns}$
 $(Z_{out} = 50 \Omega)$
 Common Source
 $T_a = 25^\circ\text{C}$

(b) V_{IN} (c) V_{OUT} 





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