T-46-23-10

CY7C161A
CY7C162A

CYPRESS SEMICONDUCTOR

16,384 x 4 Static R/W RAM Separate I/O

Features

- Automatic power-down when deselected
- Transparent write (7C161A)
- CMOS for optimum speed/power
- High speed
  - 15 ns t_{AA}
- Low active power
  - 550 mW
- Low standby power
  - 220 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge.

Functional Description

The CY7C161A and CY7C162A are high-performance CMOS static RAMs organizes as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 60% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}_1$, $\overline{CE}_2$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

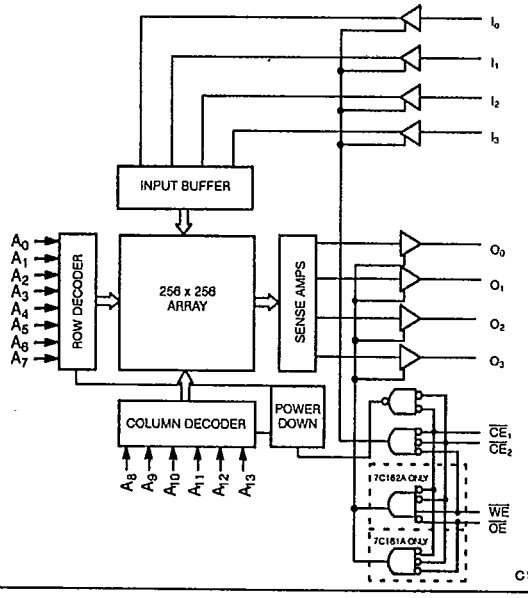
Reading the device is accomplished by taking the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high-impedance state when write enable ($\overline{WE}$) is LOW (7C162A only), or one of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) are HIGH.

A die coat is used to insure alpha immunity.

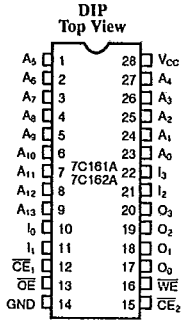
2

Logic Block Diagram

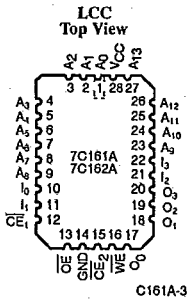


C161A-1

Pin Configurations



C161A-2



C161A-3

Selection Guide

		7C161A-15 7C162A-15	7C161A-20 7C162A-20	7C161A-25 7C162A-25	7C161A-35 7C162A-35	7C161A-45 7C162A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	100	100	100	100
	Military		100	100	100	100
Maximum Standby Current (mA)	Commercial	40/20	20	30/20	30/20	30/20
	Military		40/20	40/20	30/20	30/20

CY7C161A
CY7C162A

T-46-23-10

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to + 7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	−55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C161A-15 7C162A-15 Min.	7C161A-15 7C162A-15 Max.	7C161A-20 7C162A-20 Min.	7C161A-20 7C162A-20 Max.	7C161A-25 7C162A-25 Min.	7C161A-25 7C162A-25 Max.	7C161A-35,45 7C162A-35,45 Min.	7C161A-35,45 7C162A-35,45 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			−3.0	0.8	−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		115		100		100		100	mA
			Mil				100		100		100	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%	Com'l		40		40		30		30	mA
			Mil				40		40		30	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Com'l		20		20		20		20	mA
			Mil				20		20		20	

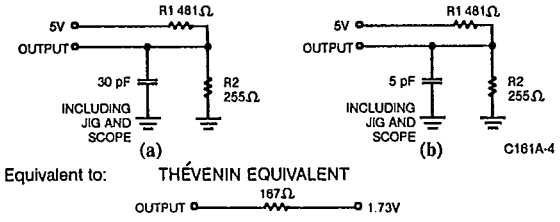
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

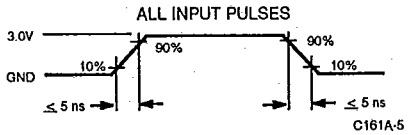
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



T-46-23-10

Switching Characteristics Over the Operating Range[2,6,7]

Parameters	Description	7C161A–15 7C162A–15		7C161A–20 7C162A–20		7C161A–25 7C162A–25		7C161A–35 7C162A–35		7C161A–45 7C162A–45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to HIGH Z		8		8		10		12		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE[10]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8] (7C162A)	5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9] (7C162A)		7		7		7		10		15	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C161A)		15		20		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C161A)		15		20		20		30		35	ns

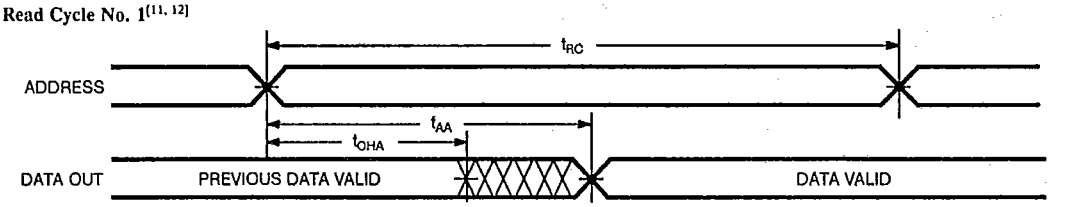
Notes:

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in the Switching Characteristics and Waveforms sections.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
9. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE}_1$, $\overline{CE}_2$ = V_{IL}.
13. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{CE}_2$ transition LOW.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C162A only).

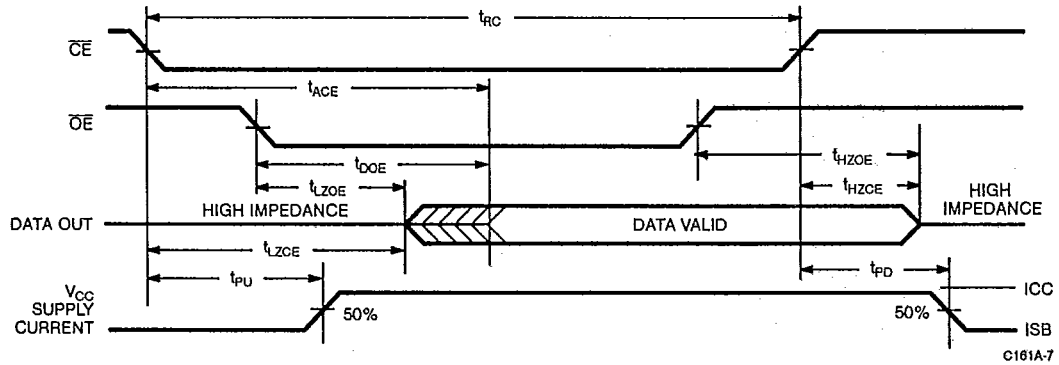
T-46-23-10

Switching Waveforms[7]

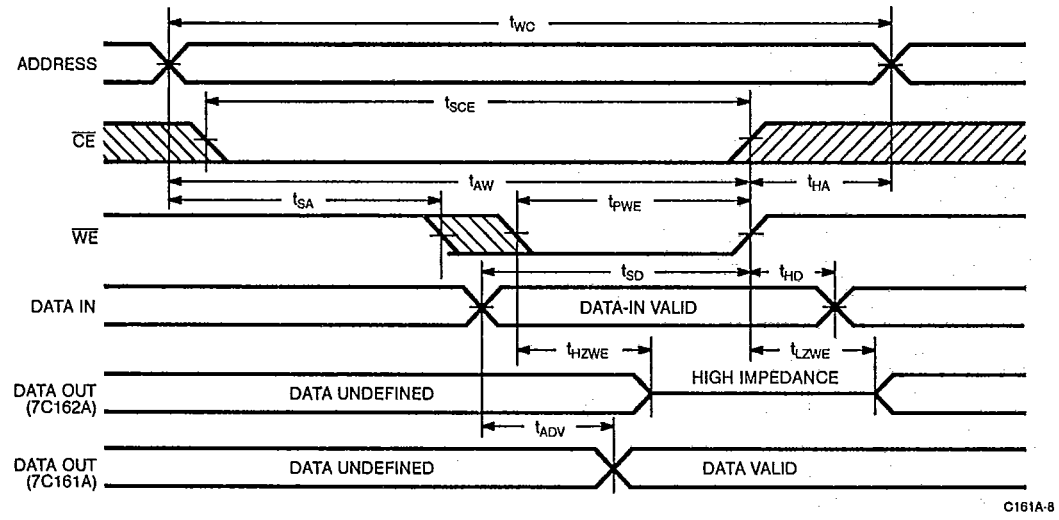
Read Cycle No. 1[11, 12]



Read Cycle No. 2[11, 13]



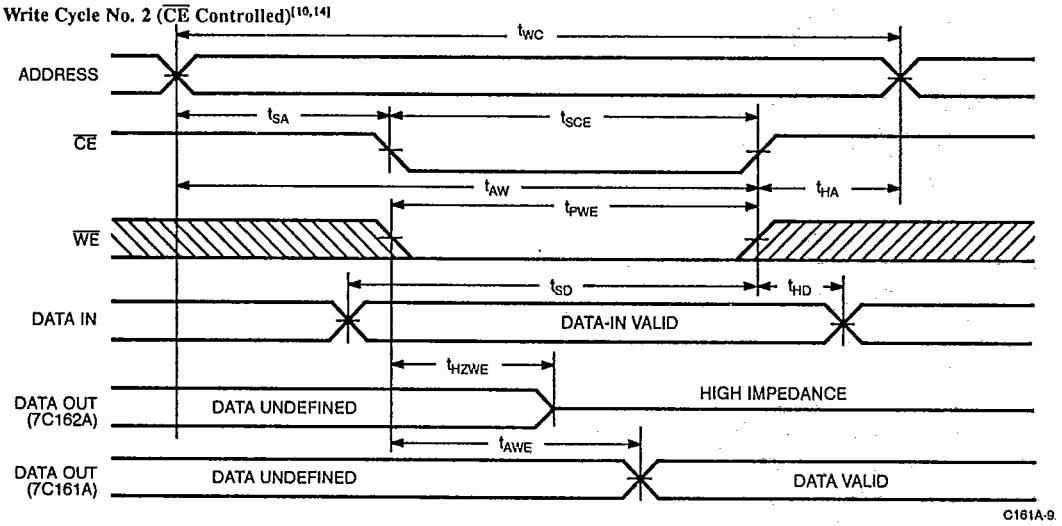
Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]



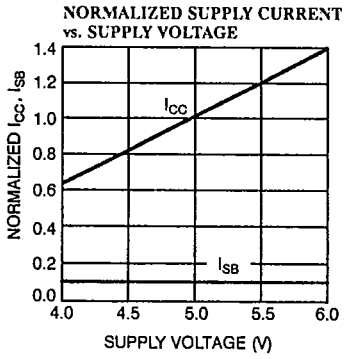
T-46-23-10

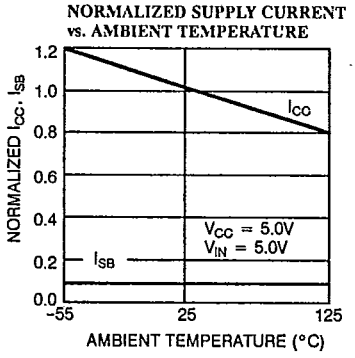
Switching Waveforms (continued)

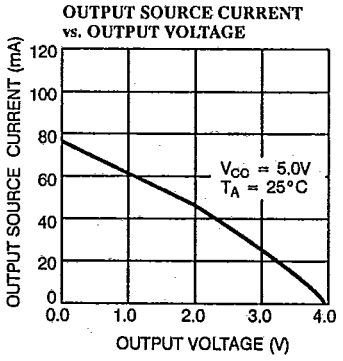
Write Cycle No. 2 ($\overline{CE}$ Controlled)[10, 14]

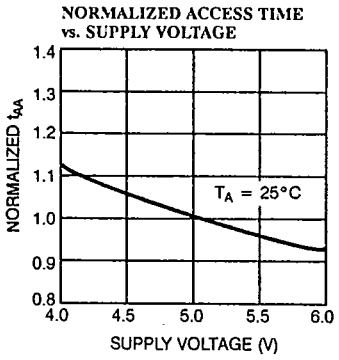


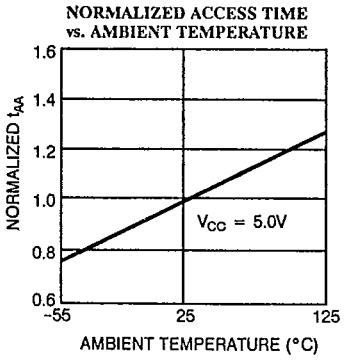
Typical DC and AC Characteristics

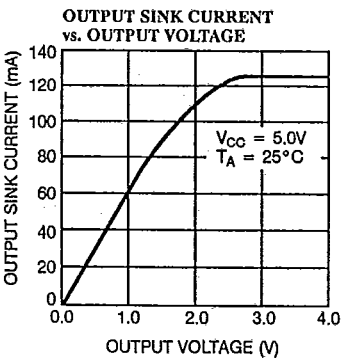








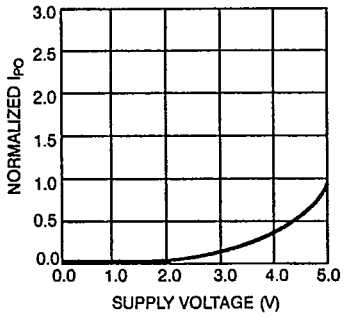




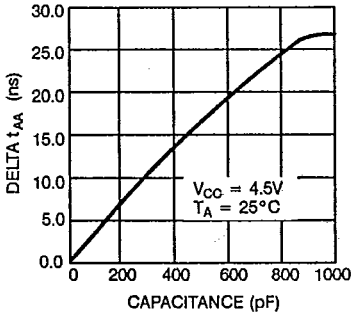
T-46-23-10

Typical DC and AC Characteristics (continued)

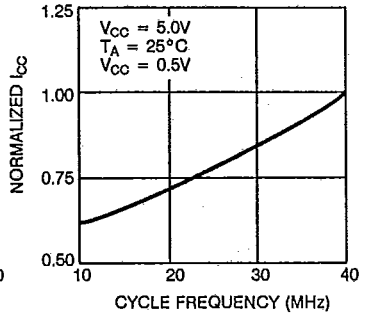
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



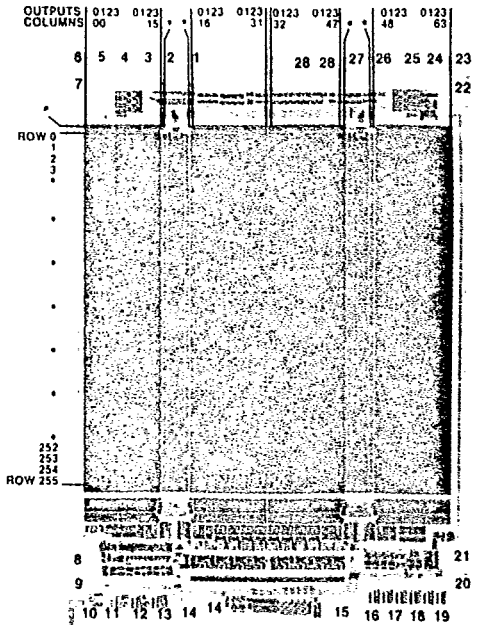
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Bit Map



Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27

CYPRESS SEMICONDUCTOR

T-46-23-10

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C161A-15PC	P21	Commercial
	CY7C161A-15VC	V21	
	CY7C161A-15DC	D22	
	CY7C161A-15LC	L54	
20	CY7C161A-20PC	P21	Commercial
	CY7C161A-20VC	V21	
	CY7C161A-20DC	D22	
	CY7C161A-20LC	L54	
	CY7C161A-20DMB	D22	Military
	CY7C161A-20LMB	L54	
25	CY7C161A-25PC	P21	Commercial
	CY7C161A-25VC	V21	
	CY7C161A-25DC	D22	
	CY7C161A-25LC	L54	
	CY7C161A-25DMB	D22	Military
	CY7C161A-25LMB	L54	
35	CY7C161A-35PC	P21	Commercial
	CY7C161A-35VC	V21	
	CY7C161A-35DC	D22	
	CY7C161A-35LC	L54	
	CY7C161A-35DMB	D22	Military
	CY7C161A-35LMB	L54	
45	CY7C161A-45PC	P21	Commercial
	CY7C161A-45VC	V21	
	CY7C161A-45DC	D22	
	CY7C161A-45LC	L54	
	CY7C161A-45DMB	D22	Military
	CY7C161A-45LMB	L54	

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C162A-15PC	P21	Commercial
	CY7C162A-15VC	V21	
	CY7C162A-15DC	D22	
	CY7C162A-15LC	L54	
20	CY7C162A-20PC	P21	Commercial
	CY7C162A-20VC	V21	
	CY7C162A-20DC	D22	
	CY7C162A-20LC	L54	
	CY7C162A-20DMB	D22	Military
	CY7C162A-20LMB	L54	
	CY7C162A-20KMB	K74	
25	CY7C162A-25PC	P21	Commercial
	CY7C162A-25VC	V21	
	CY7C162A-25DC	D22	
	CY7C161A-25LC	L54	
	CY7C162A-25DMB	D22	Military
	CY7C162A-25LMB	L54	
	CY7C162A-25KMB	K74	
35	CY7C162A-35PC	P21	Commercial
	CY7C162A-35VC	V21	
	CY7C162A-35DC	D22	
	CY7C162A-35LC	L54	
	CY7C162A-35DMB	D22	Military
	CY7C162A-35LMB	L54	
	CY7C162A-35KMB	K74	
45	CY7C162A-45PC	P21	Commercial
	CY7C162A-45VC	V21	
	CY7C162A-45DC	D22	
	CY7C162A-45LC	L54	
	CY7C162A-45DMB	D22	Military
	CY7C162A-45LMB	L54	
	CY7C162A-45KMB	K74	

T-46-23-10

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9. 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[15]	7, 8, 9, 10, 11
t_{ADV}[15]	7, 8, 9, 10, 11

Notes:
15. 7C161A only.

Document #: 38-00116