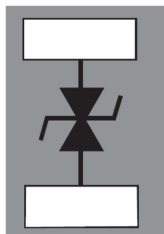


## Low clamping and low capacitance bidirectional single line ESD protection



0201 package



### Features

- Low clamping voltage  $V_{CL} = 18\text{ V}$
- Bidirectional device
- Low leakage current
- 0201 package
- Ultra-low PCB area:  $0.18\text{ mm}^2$
- **ECOPACK2** compliant
- Exceeds IEC 61000-4-2 level 4 standard:
  - $\pm 25\text{ kV}$  (air discharge)
  - $\pm 20\text{ kV}$  (contact discharge)

### Applications

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones and accessories
- Tablets and notebooks
- Portable multimedia devices and accessories
- Wearable, home automation, healthcare
- Highly integrated systems

### Description

The **ESDALC14-1BU2** is a bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for applications where both reduced line capacitance and board space saving are required.

#### Product status link

[ESDALC14-1BU2](#)

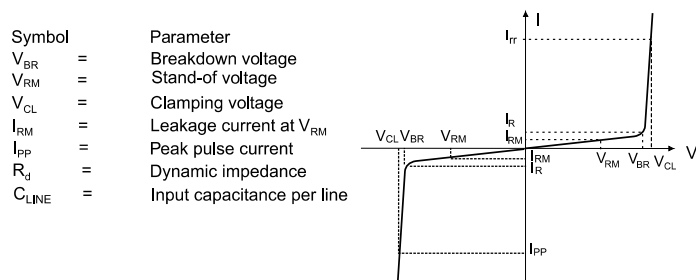
#### Product summary

Order code	ESDALC14-1BU2
Package	ST0201
Packing	Tape and reel

# 1 Characteristics

**Table 1. Absolute maximum ratings ( $T_{amb} = 25\text{ °C}$ )**

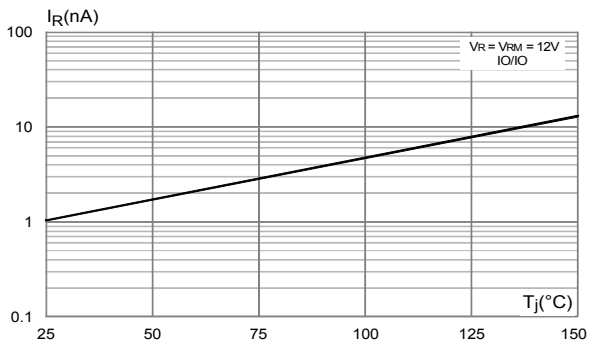
Symbol	Parameter		Value	Unit
$V_{PP}$	Peak pulse voltage	IEC 61000-4-2 contact discharge	20	kV
		IEC 61000-4-2 air discharge	25	
$P_{PP}$	Peak pulse power dissipation (8/20 $\mu$ s)		100	W
$I_{PP}$	Peak pulse current (8/20 $\mu$ s)		5	A
$T_j$	Maximum operating junction temperature range		-55 to +150	°C
$T_{stg}$	Storage temperature range		-65 to +150	°C
$T_L$	Maximum lead temperature for soldering during 10 s		260	°C

**Figure 1. Electrical characteristics (definitions)**

**Table 2. Electrical characteristics ( $T_{amb} = 25\text{ °C}$ )**

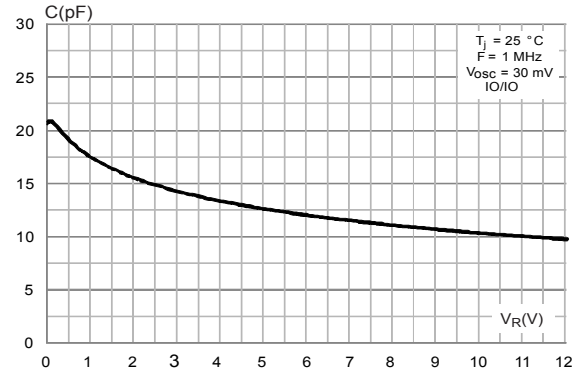
Symbol	Test condition	Min.	Typ.	Max.	Unit
$V_{BR}$	$I_R = 1\text{ mA}$	13			V
$V_{RM}$	Stand-off voltage			12	V
$I_{RM}$	$V_{RM} = 12\text{ V}$			100	nA
$V_{CL}$	8 kV contact discharge after 30 ns, IEC 61000-4-2		18		V
$V_{CL}$	8/20 $\mu$ s waveform, $I_{PP} = 5\text{ A}$		19.5		V
$R_d$	TLP - Pulse duration 100 ns - $I_{PP}$ [1A – 16A]		0.25		$\Omega$
$C_{LINE}$	F = 1 MHz, $V_{LINE} = 0\text{ V}$ , $V_{OSC} = 30\text{ mV}$		22	25	pF

## 1.1 Characteristics (curves)

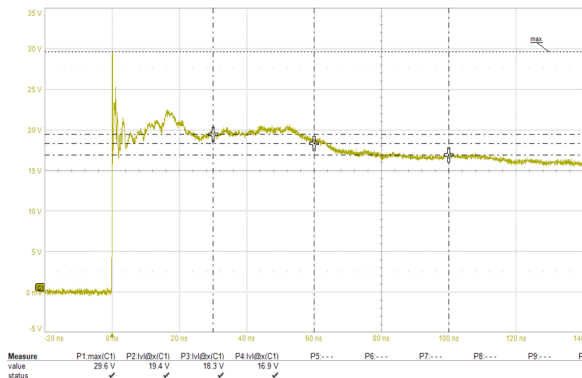
**Figure 2. Leakage current versus junction temperature (typical values)**



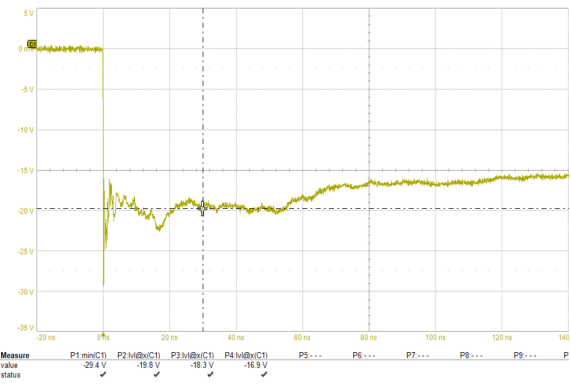
**Figure 3. Junction capacitance versus applied voltage (typical values)**



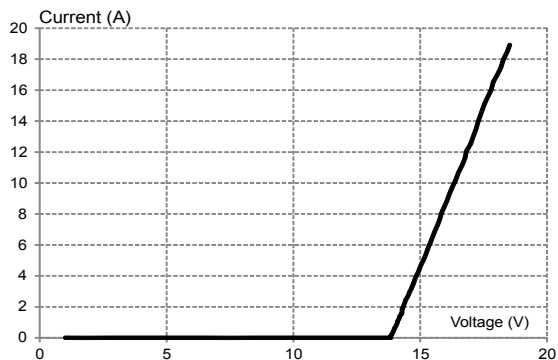
**Figure 4. ESD response to IEC 61000-4-2 (+8 kV contact discharge)**



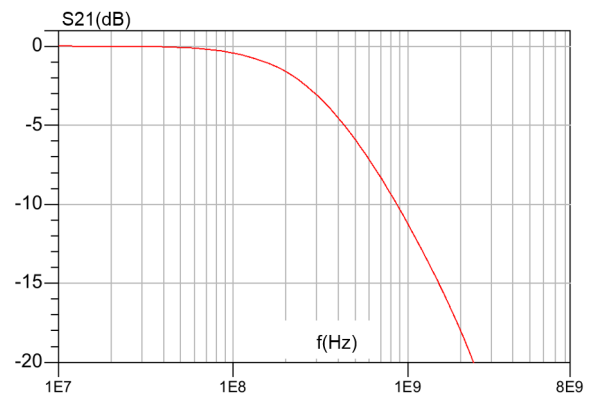
**Figure 5. ESD response to IEC 61000-4-2 (-8 kV contact discharge)**



**Figure 6. Positive TLP characteristic**



**Figure 7. S21 attenuation measurement result**

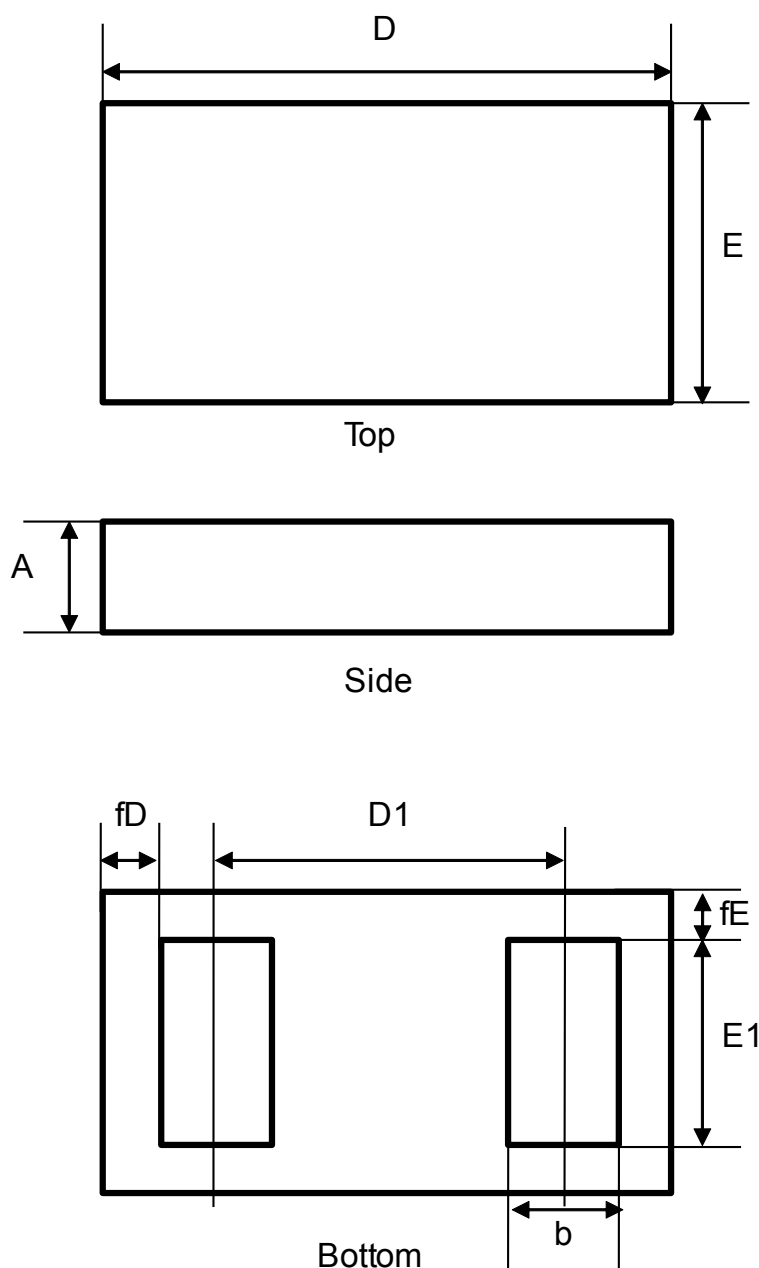


## 2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 2.1 ST0201 package information

Figure 8. ST0201 package outline

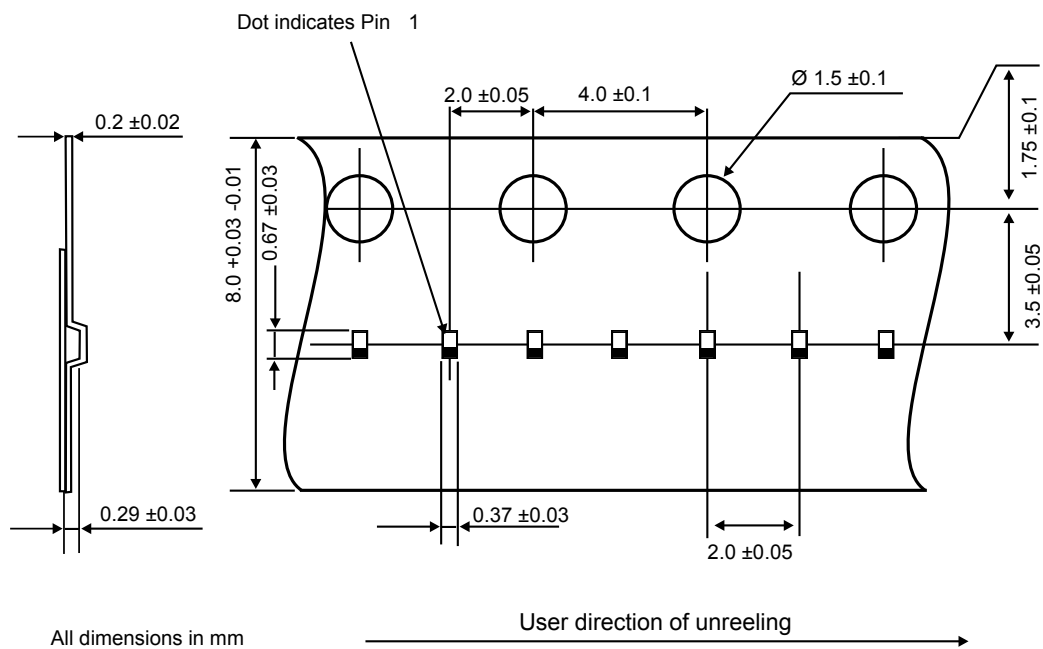


**Note:** The marking codes can be rotated by 90 ° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

**Table 3. ST0201 package mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.210	0.240	0.270
b	0.110	0.140	0.170
D	0.580	0.610	0.640
D1		0.350	
E	0.280	0.310	0.340
E1	0.160	0.190	0.220
fD		0.060	
fE		0.060	

**Figure 9. Tape and reel specification (in mm)**

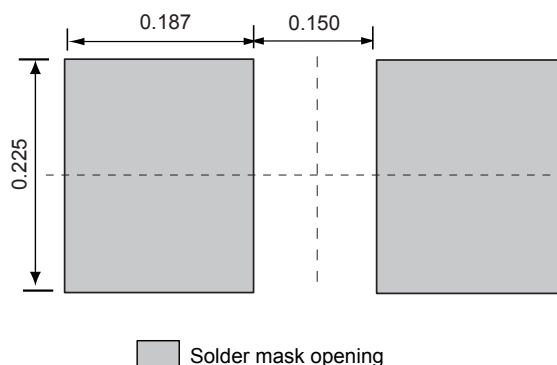


### 3 Recommendation on PCB assembly

#### 3.1 Footprint

1. Footprint in mm
  - a. SMD footprint design is recommended.

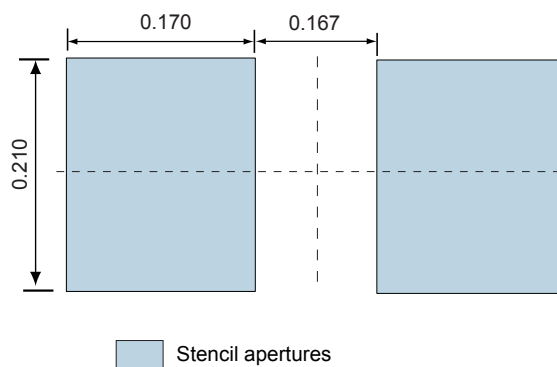
**Figure 10. Footprint in mm**



#### 3.2 Stencil opening design

1. Reference design
  - a. Stencil opening thickness: 75  $\mu\text{m}$  / 3 mils

**Figure 11. Recommended stencil window position in mm**



#### 3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38  $\mu\text{m}$ .

### 3.4 Placement

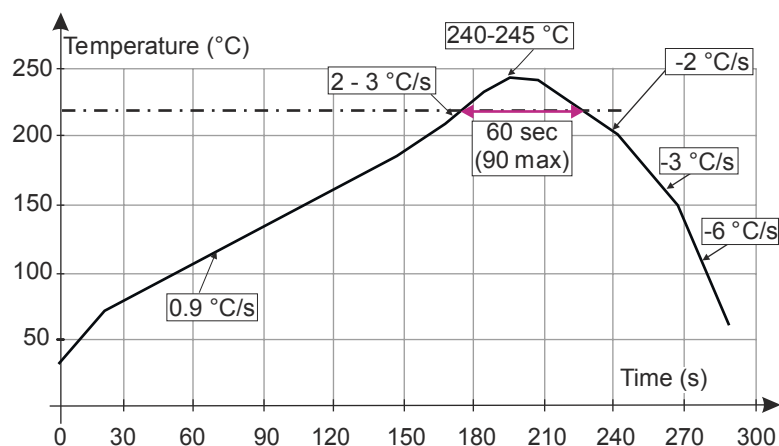
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of  $\pm 0.05$  mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

### 3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

### 3.6 Reflow profile

**Figure 12. ST ECOPACK recommended soldering reflow profile for PCB mounting**



**Note:** Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

## 4 Ordering information

**Table 4. Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ESDALC14-1BU2	V <sup>(1)</sup>	ST0201	0.120 mg	15000	Tape and reel

1. The marking can be rotated by multiples of 90° to differentiate assembly location



## Revision history

**Table 5. Document revision history**

Date	Version	Changes
07-Sep-2018	1	Initial release.
26-Mar-2020	2	Updated <a href="#">Figure 8</a> and <a href="#">Table 3</a> .

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