

283-617

W24257



32K × 8 CMOS STATIC RAM

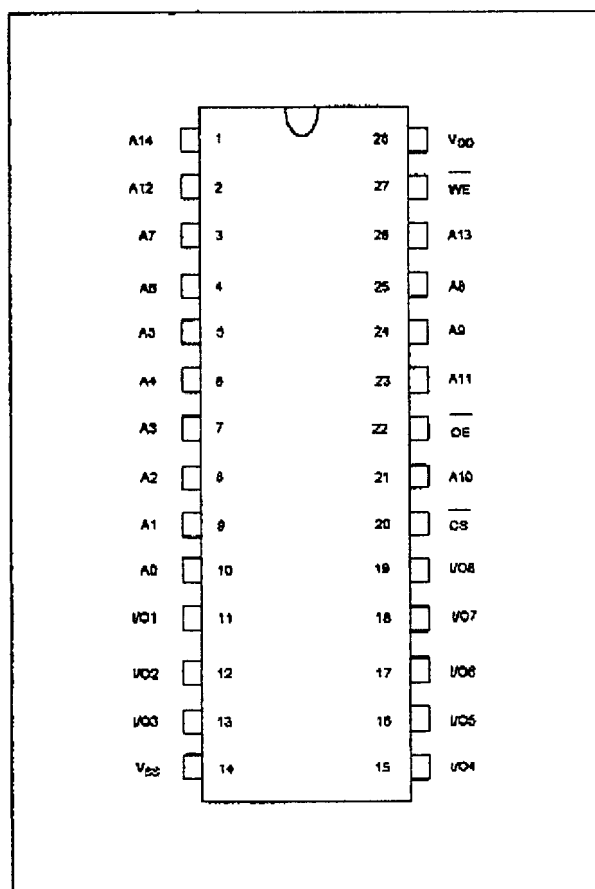
GENERAL DESCRIPTION

The W24257 is a slow speed, low power CMOS static RAM organized as 32768 × 8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

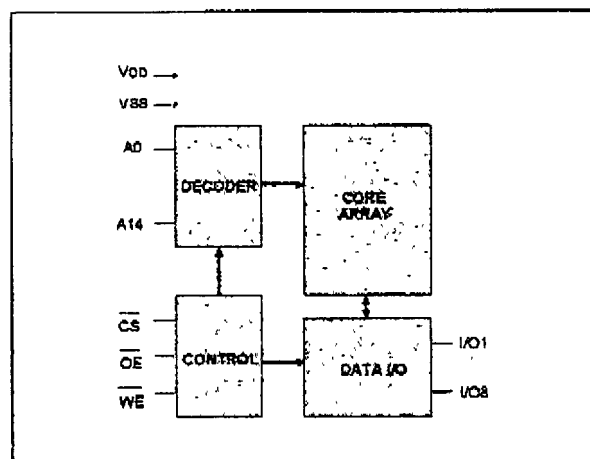
FEATURES

- Low power consumption:
 - Active: 400 mW (max.)
 - Standby: 250 μ W (max.) (LL-version)
500 μ W (max.) (L-version)
- Access time: 70/100 nS (max.)
- Single +5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min)
- Available packages: 28-pin 600 mil DIP, 330 mil SOP, 300 mil skinny DIP and SOJ

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0-A14	Address Inputs
I/O1-I/O8	Data Inputs/Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground

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TRUTH TABLE

CS	OE	WE	MODE	I/O1-I/O8	VDD CURRENT
H	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	Output Disable	High Z	IDD
L	L	H	Read	Data Out	IDD
L	X	L	Write	Data In	IDD

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to VSS Potential	-0.5 to +7.0	V
Input/Output to VSS Potential	-0.5 to VDD +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

Operating Characteristics

(VDD = 5V ±10%, VSS = 0V, TA = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Input Low Voltage	V _{IL}	-	-0.5	-	+0.8	V	
Input High Voltage	V _{IH}	-	+2.2	-	V _{DD} +0.5	V	
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-2	-	+2	μA	
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , $\overline{\text{CS}}$ = V _{IH} (min.) or $\overline{\text{OE}}$ = V _{IH} (min.) or $\overline{\text{WE}}$ = V _{IL} (max.)	-2	-	+2	μA	
Output Low Voltage	V _{OL}	I _{OL} = +4.0 mA	-	-	0.4	V	
Output High Voltage	V _{OH}	I _{OH} = -1.0 mA	2.4	-	-	V	
Operating Power	I _{DD}	$\overline{\text{CS}}$ = V _{IL} (min.), I/O = 0 mA	70	-	-	mA	
Supply Current		Cycle = min., Duty = 100%	100	-	-	mA	
Standby Power Supply Current	I _{SB}	$\overline{\text{CS}}$ = V _{IH} (min.) Cycle = min., Duty = 100%	-	-	3	mA	
	I _{SB1}	$\overline{\text{CS}}$ ≥ V _{DD} -0.2V	LL	-	-	50	μA
			L	-	-	100	μA

Note: Typical characteristics are at VDD = 5V, TA = 25° C.



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CAPACITANCE

($V_{DD} = 5V$, $T_A = 25^\circ C$, $f = 1 MHz$)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C _{IN}	V _{IN} = 0V	6	pF
Input/Output Capacitance	C _{I/O}	V _{OUT} = 0V	8	pF

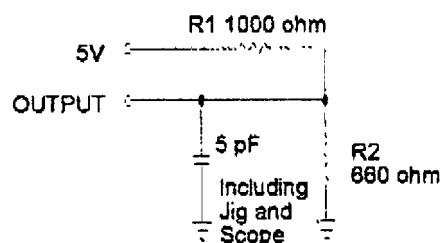
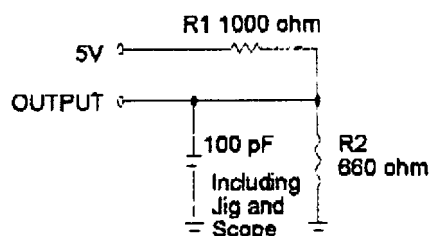
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

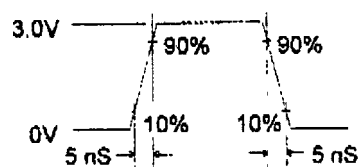
AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0.8V to 2.4V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	C _L = 100 pF, I _{OH} /I _{OL} = -1 mA/4 mA

AC Test Loads and Waveform



(For T_{CLZ}, T_{OLZ}, T_{CHZ}, T_{OHZ}, T_{WHZ}, T_{OW})



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AC Characteristics, continued

(V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

Read Cycle

PARAMETER	SYM.	W24257-70		W24257-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	70	-	100	-	nS
Address Access Time	TAA	-	70	-	100	nS
Chip Select Access Time	TACS	-	70	-	100	nS
Output Enable to Output Valid	TAOE	-	35	-	50	nS
Chip Selection to Output in Low Z	TCLZ*	10	-	10	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	5	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	30	-	35	nS
Output Disable to Output in High Z	TOHZ*	-	30	-	35	nS
Output Hold from Address Change	TOH	10	-	10	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

PARAMETER		SYM.	W24257-70		W24257-10		UNIT
			MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		TWC	70	-	100	-	nS
Chip Selection to End of Write		TcW	60	-	80	-	nS
Address Valid to End of Write		TAW	60	-	80	-	nS
Address Setup Time		TAS	0	-	0	-	nS
Write Pulse Width		TWP	45	-	60	-	nS
Write Recovery Time	$\overline{CS}$, $\overline{WE}$	TWR	0	-	0	-	nS
Data Valid to End of Write		TDW	30	-	40	-	nS
Data Hold from End of Write		TDH	0	-	0	-	nS
Write to Output in High Z		TWHZ*	-	30	-	30	nS
Output Disable to Output in High Z		TOHZ*	-	30	-	30	nS
Output Active from End of Write		TOW	0	-	0	-	nS

* These parameters are sampled but not 100% tested

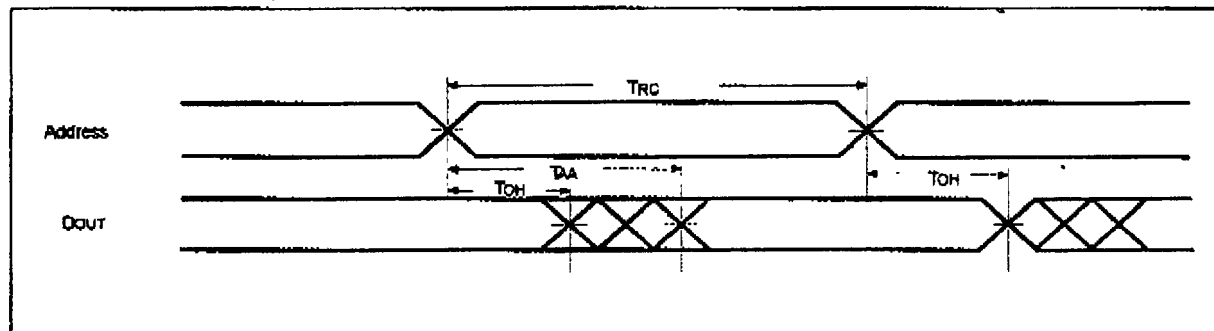
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TIMING WAVEFORMS

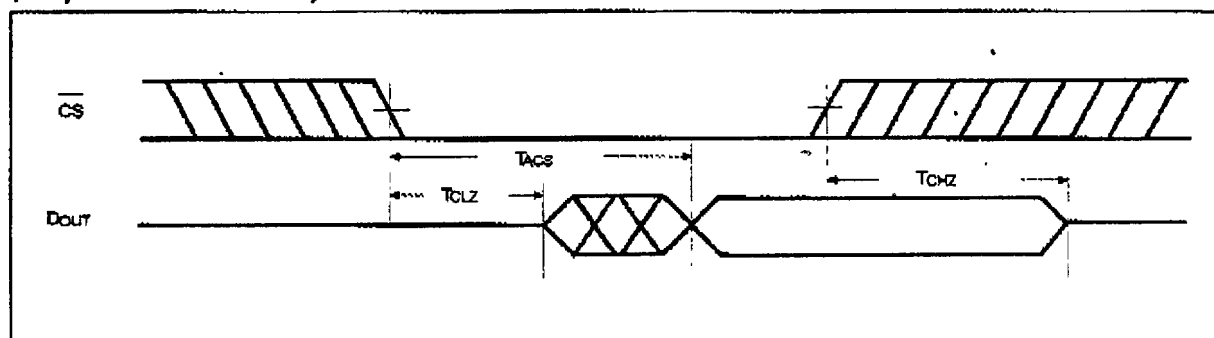
Read Cycle 1

(Address Controlled)



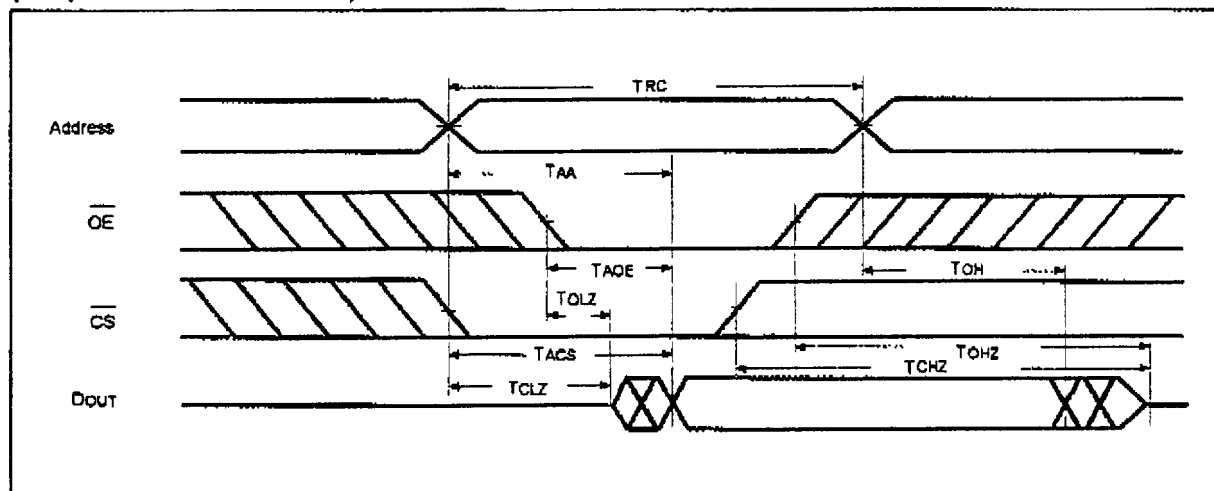
Read Cycle 2

(Chip Select Controlled)



Read Cycle 3

(Output Enable Controlled)



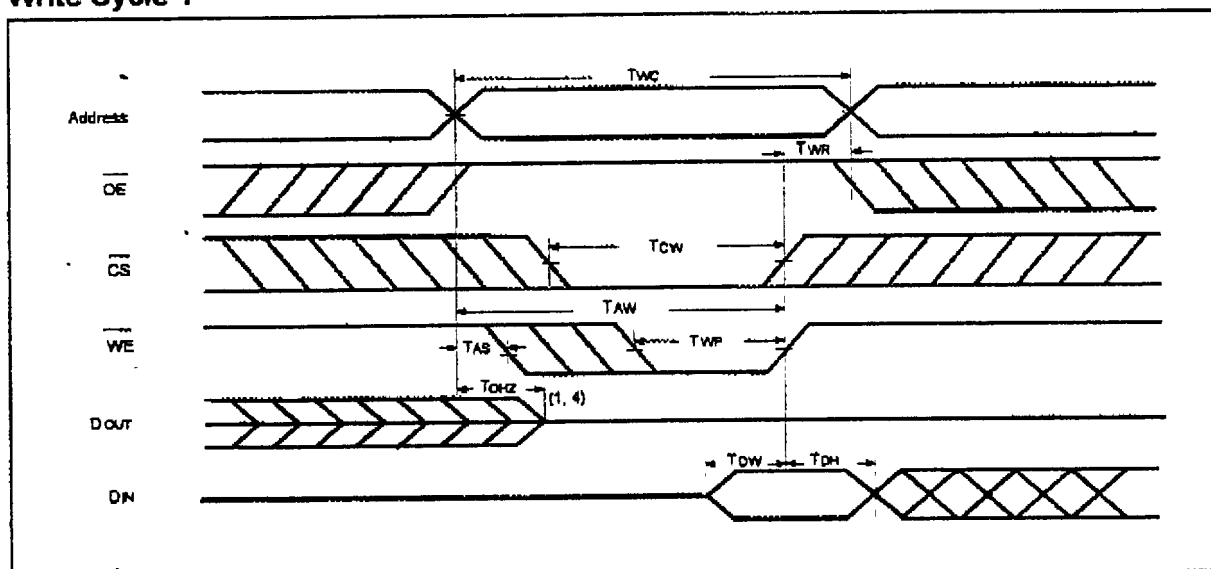
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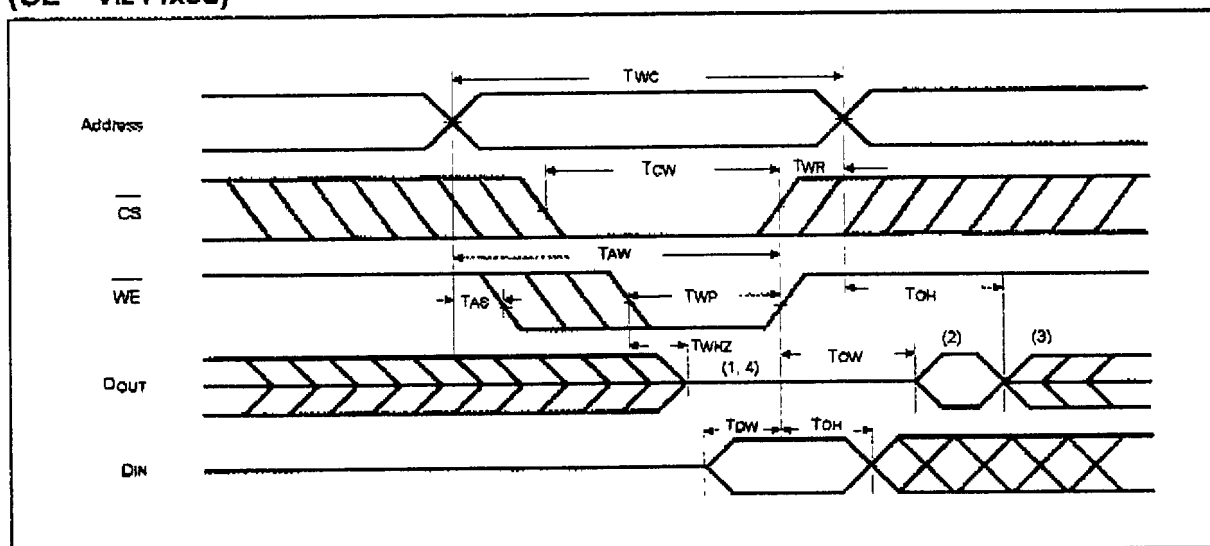


Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

(OE = V_{IL} Fixed)

Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.



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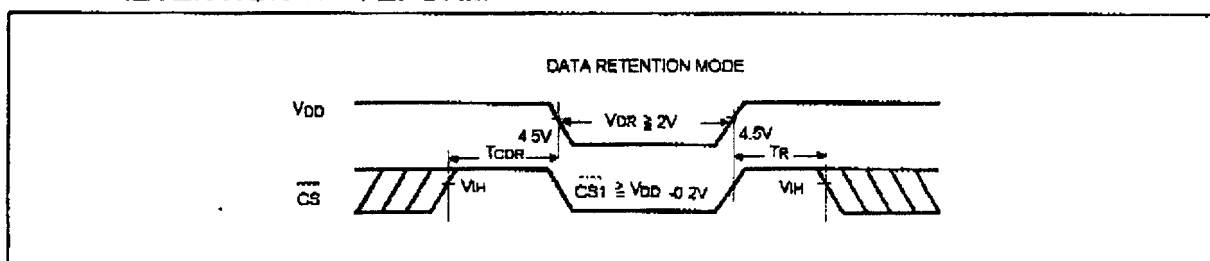
DATA RETENTION CHARACTERISTICS

($T_A = 0$ to 70°C)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD for Data Retention	VDR	$\overline{\text{CS}} \geq V_{DD} - 0.2\text{V}$	2.0	-	-	V
Data Retention Current	I _{DDDR}	$\overline{\text{CS}} \geq V_{DD} - 0.2\text{V}$ $V_{DD} = 3\text{V}$	LL	-	-	20 μA
			L	-	-	50 μA
Chip Deselect to Data Retention Time	T _{CDR}	See data retention waveform	0	-	-	nS
Operation Recovery Time	TR		TRC*	-	-	nS

TRC* = Read Cycle Time

DATA RETENTION WAVEFORM



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24257-70LL	70	80	50	600 mil DIP
W24257-70L	70	80	100	600 mil DIP
W24257-10L	100	70	100	600 mil DIP
W24257S-70LL	70	80	50	330 mil SOP
W24257S-70L	70	80	100	330 mil SOP
W24257S-10L	100	70	100	330 mil SOP
W24257K-70LL	70	80	50	300 mil Skinny
W24257K-70L	70	80	100	300 mil Skinny
W24257K-10L	100	70	100	300 mil Skinny
W24257J-70LL	70	80	50	300 mil SOJ
W24257J-70L	70	80	100	300 mil SOJ
W24257J-10L	100	70	100	300 mil SOJ

Notes:

- Winbond reserves the right to make changes to its products without prior notice.
- Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

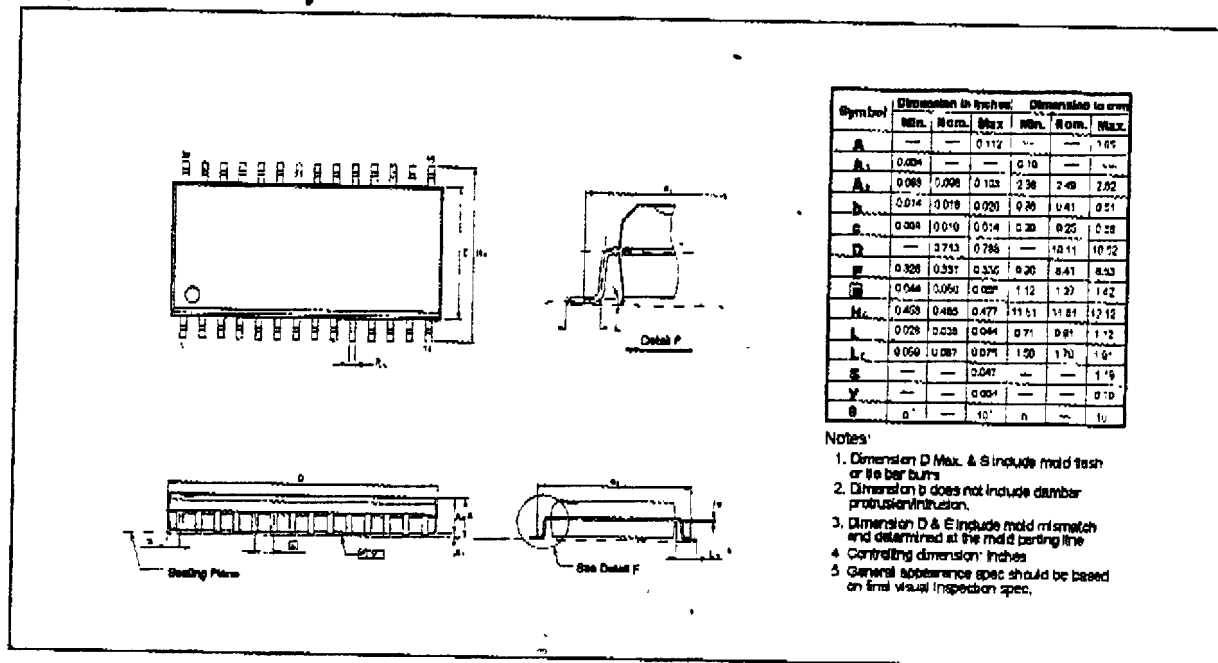
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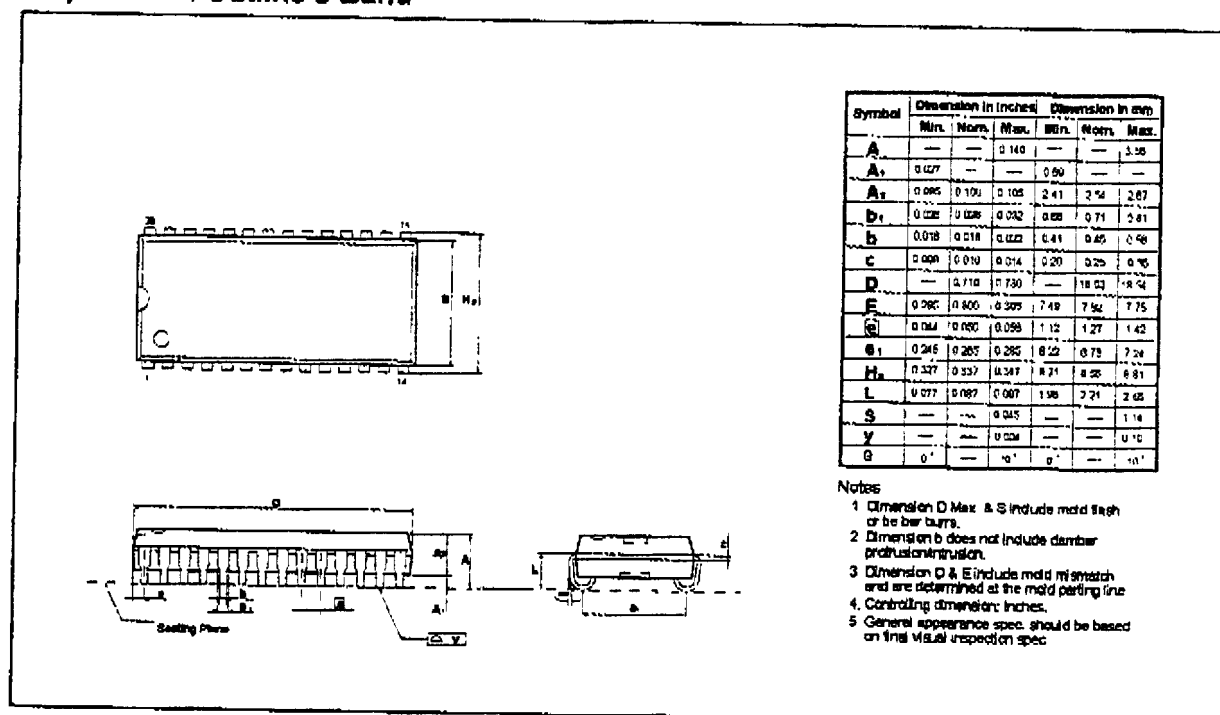
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Package Dimensions, continued

28-pin SO Wide Body



28-pin Small Outline J Band

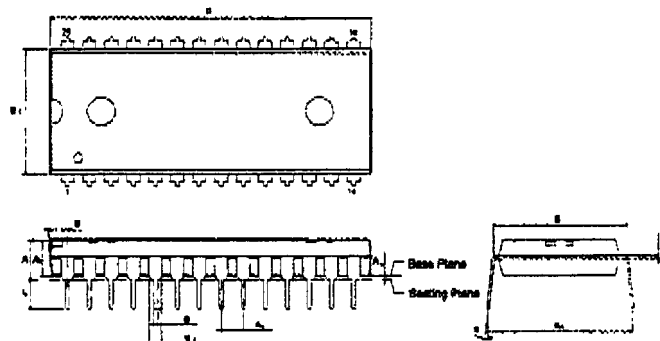


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PACKAGE DIMENSIONS

28-pin P-DIP

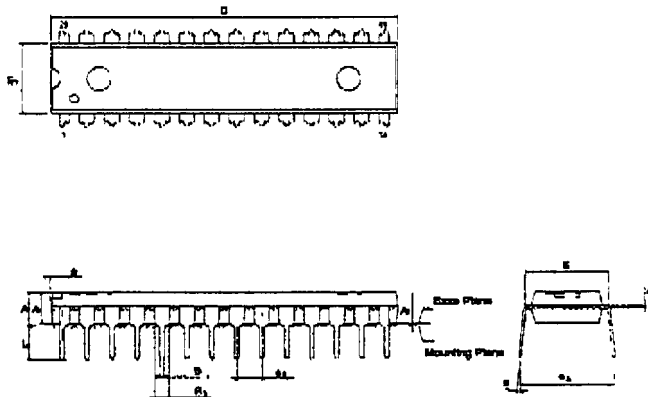


Symbol	Dimension in inches			Dimension in mm		
	Min.	Norm.	Max.	Min.	Norm.	Max.
A	—	—	1.0216	—	—	25.9
A ₁	0.016	—	—	0.25	—	—
A ₂	0.150	0.153	0.160	3.81	3.94	4.05
B	0.018	0.018	0.022	0.41	0.46	0.55
B ₁	0.058	0.060	0.064	1.47	1.52	1.63
C	0.008	0.010	0.014	0.20	0.25	0.35
D	—	1.400	1.470	—	35.68	37.34
E	0.190	0.190	0.210	4.83	4.83	5.33
E ₁	0.540	0.545	0.550	13.72	13.84	13.97
L	0.190	0.190	0.110	4.83	4.83	2.79
a	0.125	0.125	0.140	3.18	3.30	3.55
a ₁	0	—	15	0	—	15
a ₂	0.630	0.600	0.670	16.01	15.24	17.02
S	—	—	0.090	—	—	2.29

Notes:

1. Dimension D Max. & S include mold flash or be burr.
2. Dimension E₁ does not include interlead flash.
3. Dimension D & E₁ include mold mismatch and are determined at the mold parting line.
4. Dimension B₁ does not include dambar protrusion/intrusion.
5. Controlling dimension: inches.
6. General appearance spec. should be based on final visual inspection spec.

28-pin P-DIP Skinny



Symbol	Dimension in inches			Dimension in mm		
	Min.	Norm.	Max.	Min.	Norm.	Max.
A	—	—	0.175	—	—	4.43
A ₁	0.012	—	—	0.25	—	—
A ₂	0.125	0.130	0.145	3.18	3.30	3.68
B	0.016	0.016	0.022	0.41	0.46	0.55
B ₁	0.058	0.060	0.064	1.47	1.52	1.63
C	0.008	0.010	0.014	0.20	0.25	0.35
D	—	1.368	1.400	—	35.26	35.56
E	0.190	0.190	0.210	4.83	4.83	5.33
E ₁	0.540	0.545	0.550	13.72	13.84	13.97
L	0.190	0.190	0.110	4.83	4.83	2.79
a	0	—	15	0	—	15
a ₁	0.390	0.350	0.470	9.91	8.91	11.93
S	—	—	0.090	—	—	2.29

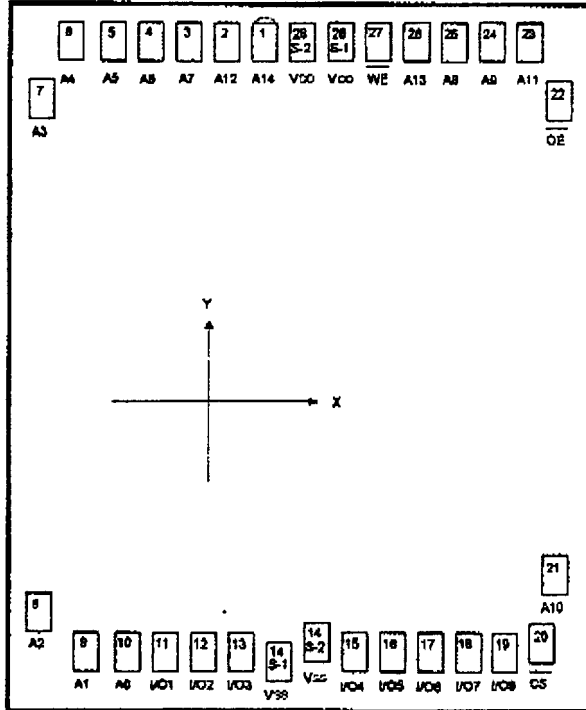
Notes:

1. Dimension D Max. & S include mold flash or be burr.
2. Dimension E₁ does not include interlead flash.
3. Dimension D & E₁ include mold mismatch and are determined at the mold parting line.
4. Dimension B₁ does not include dambar protrusion/intrusion.
5. Controlling dimension: inches.
6. General appearance spec. should be based on final visual inspection spec.

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BONDING PAD DIAGRAM



PAD NO.	X	Y
1	-127.08	2785.05
2	-377.73	2785.05
3	-628.38	2785.05
4	-879.03	2785.05
5	-1129.68	2785.05
6	-1380.33	2785.05
7	-1686.51	2640.06
8	-1682.01	-2645.91
9	-1448.10	-2802.51
10	-1090.80	-2802.51
11	-877.32	-2807.28
12	-627.84	-2807.28
13	-349.56	-2807.28
14S-1	-155.52	-2781.00
14S-2	-7.02	-2771.64
15	249.21	-2807.28
16	498.69	-2807.28
17	776.97	-2807.28
18	1026.45	-2807.28
19	1304.73	-2807.28
20	1689.30	-2802.51
21	1686.51	-2520.90
22	1686.51	2644.74
23	1459.17	2785.05
24	1208.52	2785.05
25	957.87	2785.05
26	707.22	2785.05
27	456.57	2785.05
28S-1	205.92	2771.55
28S-2	21.42	2780.91

Note: For bare chip form (C.O.B) applications, the substrate must be connected to V_{DD} or left floating in the PCB layout.