



74HC139-Q100; 74HCT139-Q100

Dual 2-to-4 line decoder/demultiplexer

Rev. 3 — 29 February 2024

Product data sheet

1. General description

The 74HC139-Q100; 74HCT139-Q100 decodes two binary weighted address inputs (nA0, nA1) to four mutually exclusive outputs (nY0 to nY3). Each decoder features an enable input (nE). When nE is HIGH all outputs are forced HIGH. The enable input can be used as the data input for a 1-to-4 demultiplexer application. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

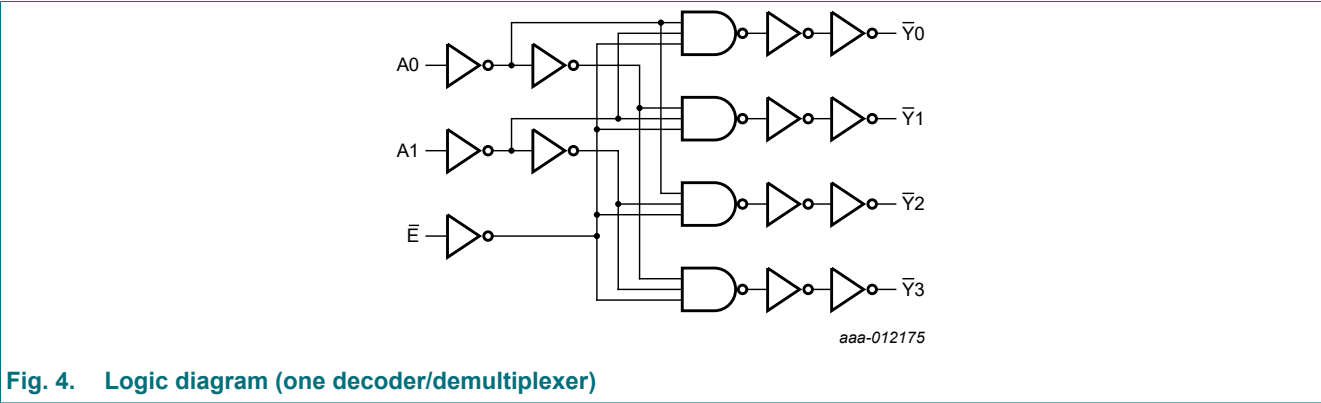
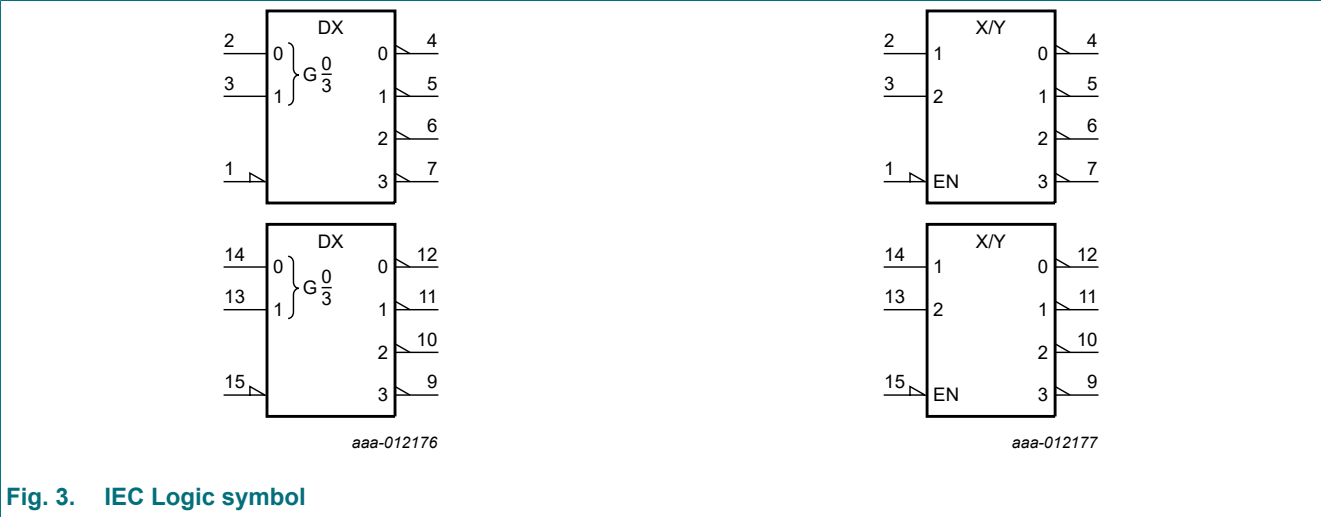
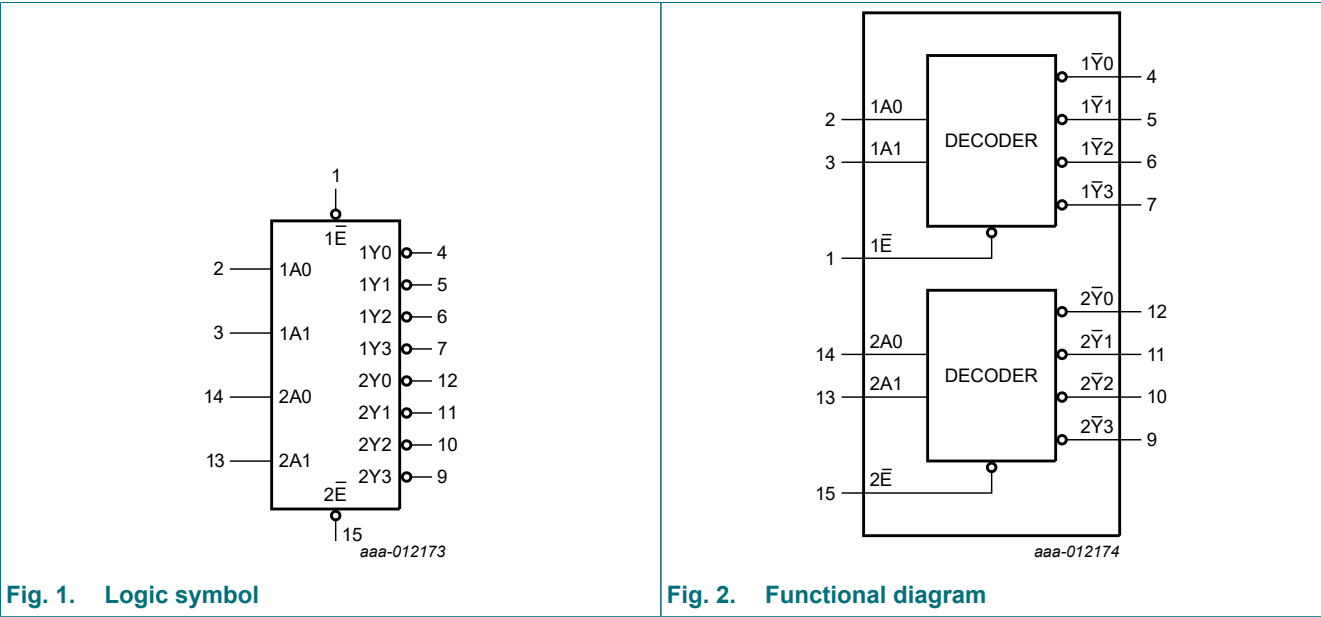
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Input levels:
 - For 74HC139-Q100: CMOS level
 - For 74HCT139-Q100: TTL level
- Demultiplexing capability
- 2 independent 2-to-4 decoders
- Multifunction capability
- Suitable for memory decoding, data routing or code conversion
- Complies with JEDEC standard no. 7A
- Active LOW mutually exclusive outputs
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

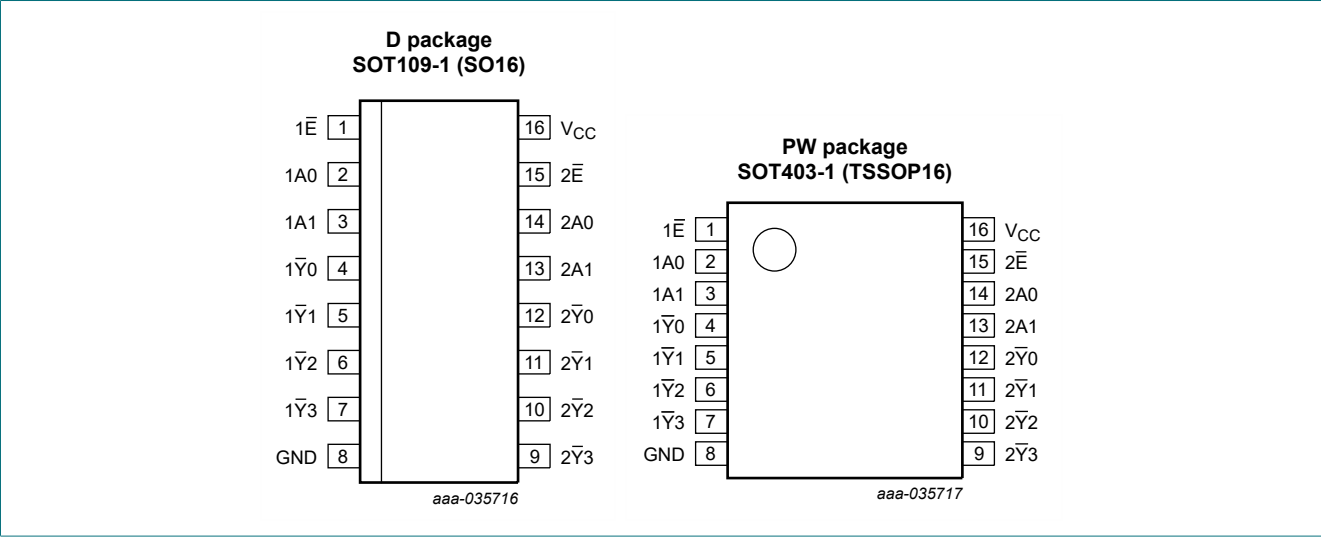
Type number	Package			
	Temperature range	Name	Description	Version
74HC139D-Q100 74HCT139D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC139PW-Q100 74HCT139PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1E, 2E	1, 15	enable input (active LOW)
1A0, 1A1	2, 3	address input
1Y0, 1Y1, 1Y2, 1Y3	4, 5, 6, 7	output (active LOW)
GND	8	ground (0 V)
2Y0, 2Y1, 2Y2, 2Y3	12, 11, 10, 9	output (active LOW)
2A0, 2A1	14, 13	address input
VCC	16	positive supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Control	Input		Output			
nE	nA1	nA0	nY3	nY2	nY1	nY0
H	X	X	H	H	H	H
L	L	L	H	H	H	L
L	L	H	H	H	L	H
L	H	L	H	L	H	H
L	H	H	L	H	H	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	-	±25	mA
I _{CC}	quiescent supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[1]	-	500	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC139-Q100			74HCT139-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC139-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 µA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 µA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.5	-	±5.0	-	±10.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT139-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.5	-	±5.0	-	±10	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A								
		per input pin; 1An inputs	-	70	252	-	315	-	343	µA
		per input pin; 2An inputs	-	70	252	-	315	-	343	µA
		per input pin; nE inputs	-	135	486	-	607.5	-	661.5	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

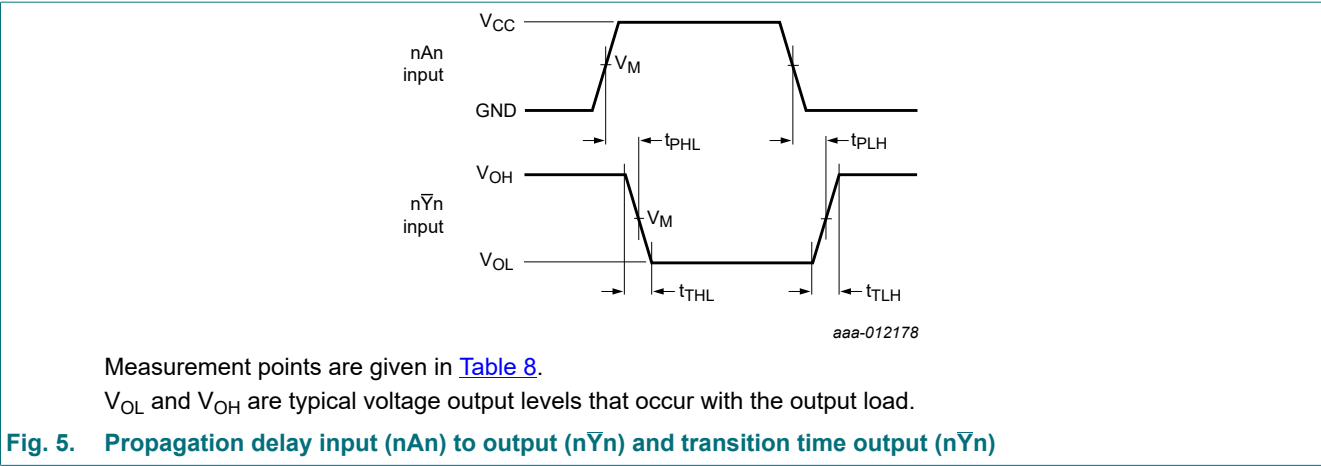
Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC139-Q100										
t _{pd}	propagation delay	nAn to nȳn; see Fig. 5 [1]								
		V _{CC} = 2.0 V	-	39	145	-	180	-	220	ns
		V _{CC} = 4.5 V	-	14	29	-	36	-	44	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	11	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	11	25	-	31	-	38	ns
		nĒ to nȳn; see Fig. 6 [1]								
		V _{CC} = 2.0 V	-	33	135	-	170	-	205	ns
		V _{CC} = 4.5 V	-	12	27	-	34	-	41	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	10	-	-	-	-	-	ns
	V _{CC} = 6.0 V	-	10	23	-	29	-	35	ns	
t _t	transition time	nȳn; see Fig. 5 and Fig. 6 [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} [3]	-	42	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT139-Q100										
t _{pd}	propagation delay	nAn to $\bar{Y}n$; see Fig. 5 [1]								
		V _{CC} = 4.5 V	-	16	34	-	43	-	51	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	13	-	-	-	-	-	ns
		n $\bar{E}$ to n $\bar{Y}n$; see Fig. 6 [1]								
		V _{CC} = 4.5 V	-	16	34	-	43	-	51	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	13	-	-	-	-	-	ns
t _t	transition time	n $\bar{Y}n$; see Fig. 5 and Fig. 6 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} - 1.5 V [3]	-	44	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [2] t_t is the same as t_{THL} and t_{TLH}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



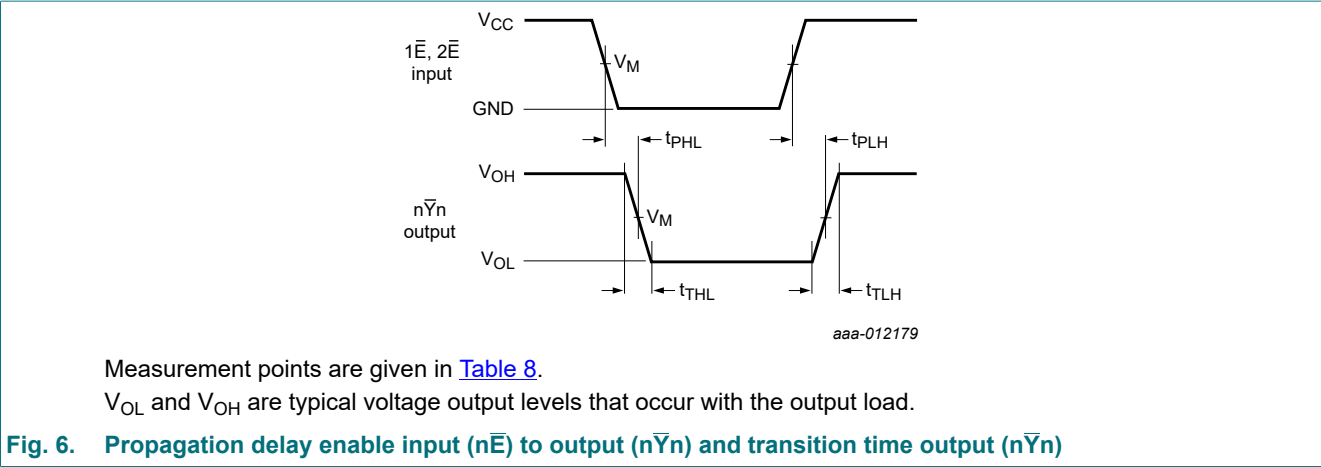


Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC139-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT139-Q100	1.3 V	1.3 V

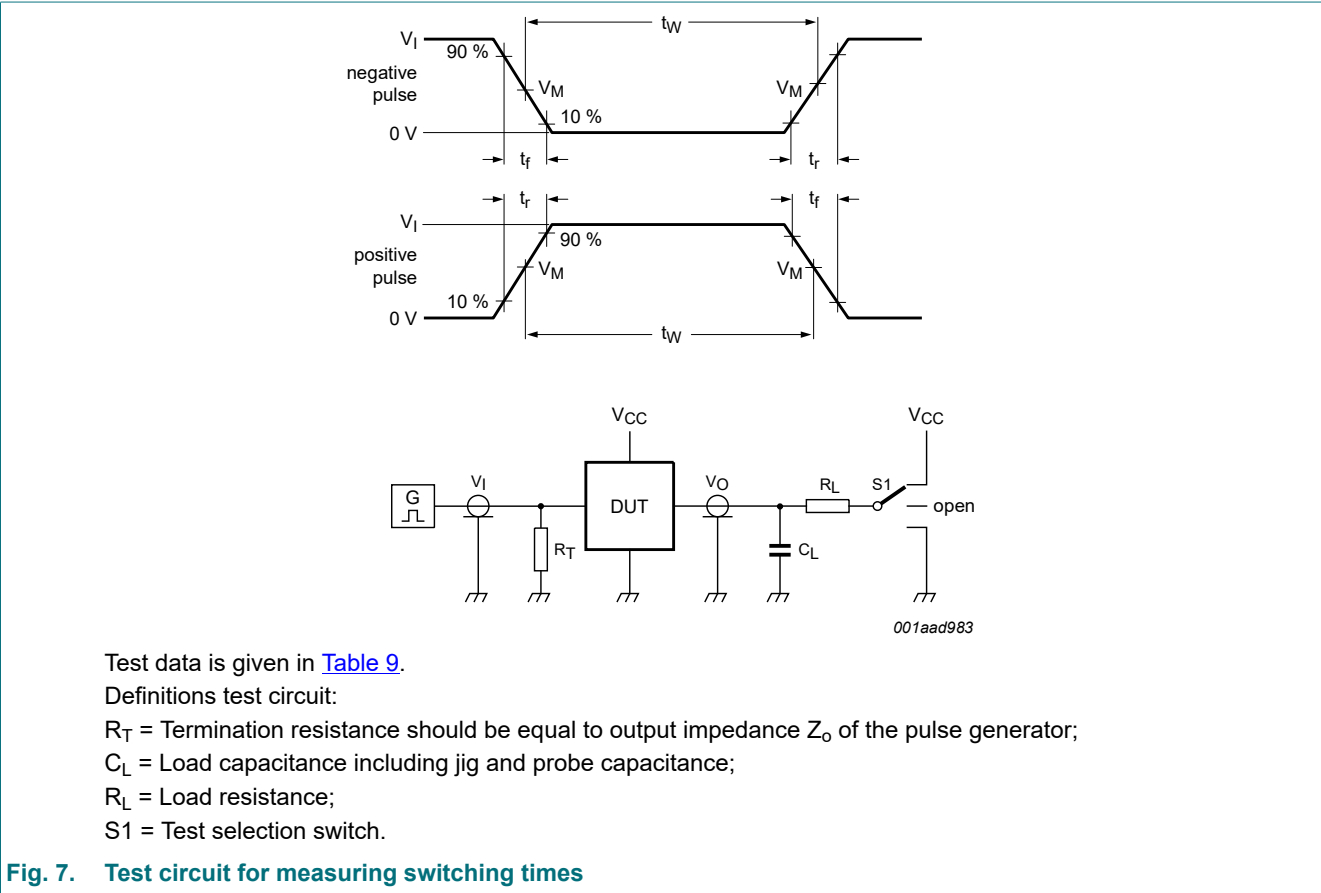


Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC139-Q100	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT139-Q100	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

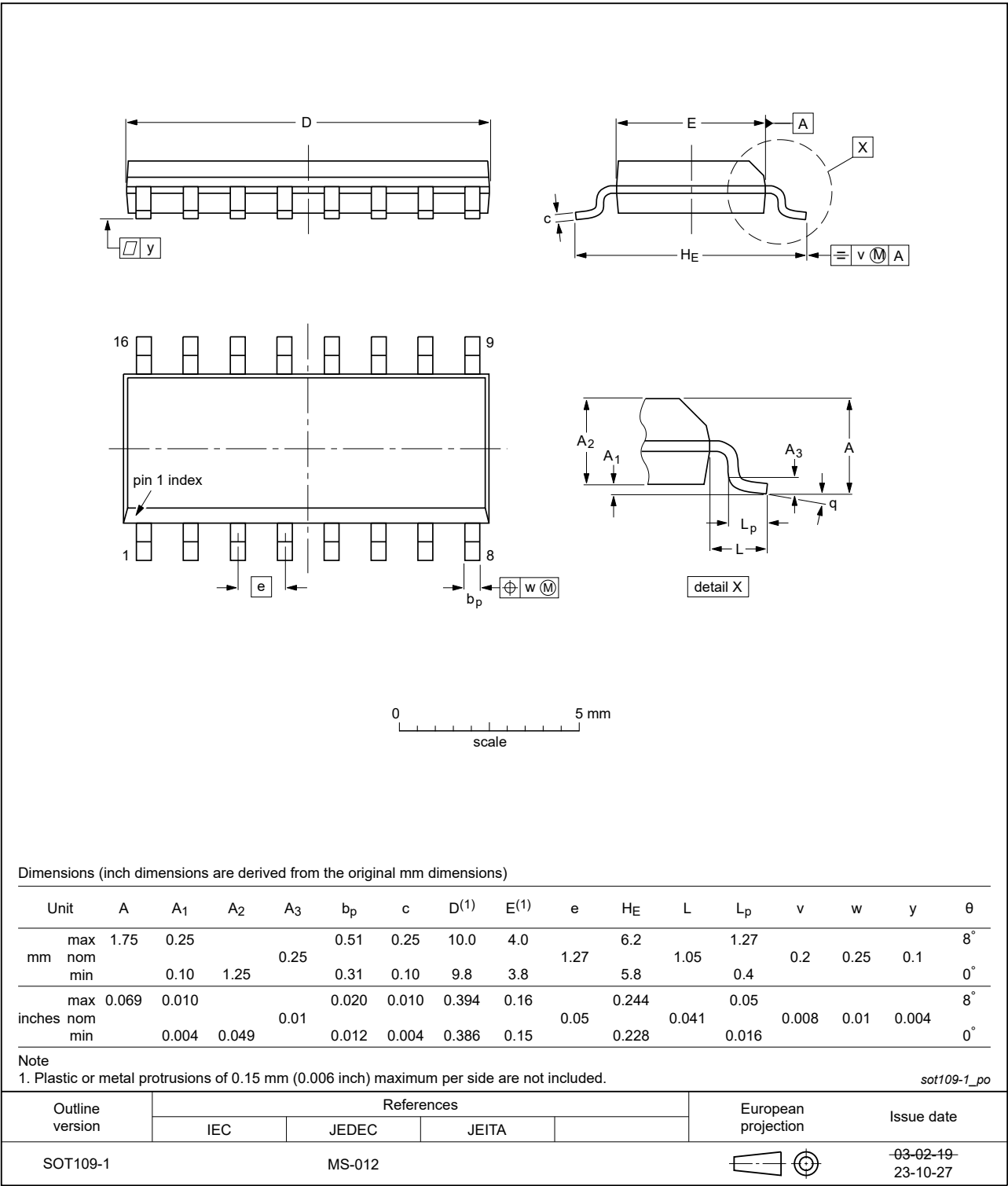


Fig. 8. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

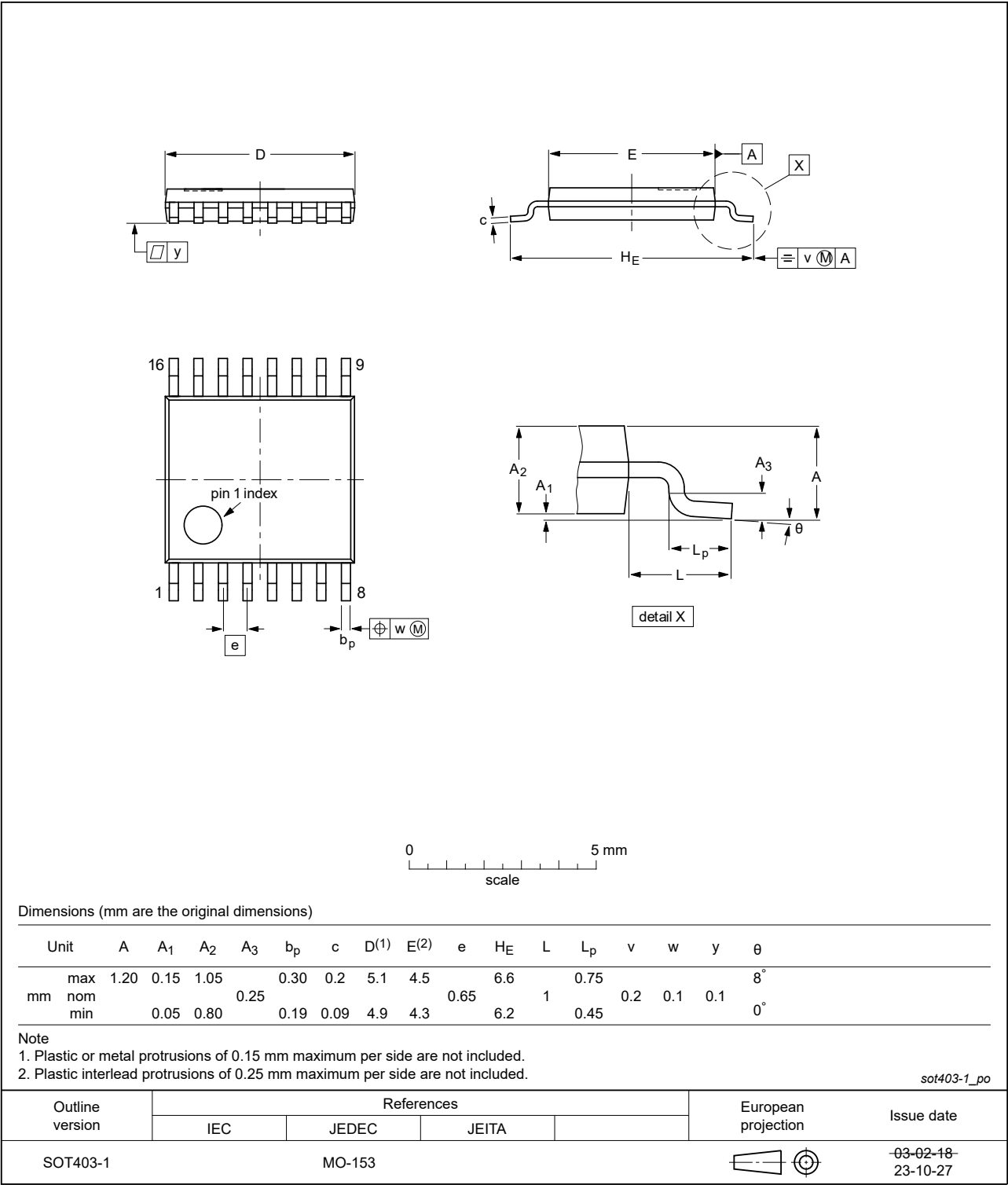


Fig. 9. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT139_Q100 v.3	20240229	Product data sheet	-	74HC_HCT139_Q100 v.2
Modifications:	- Section 2: ESD specification updated according to the latest JEDEC standard. - Fig. 8, Fig. 9: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153			
74HC_HCT139_Q100 v.2	20210114	Product data sheet	-	74HC_HCT139_Q100 v.1
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Type numbers 74HC139DB-Q100 and 74HCT139DB-Q100 (SOT338-1 / SSOP16) removed. - Section 7: Derating values for P_{tot} total power dissipation have been updated.			
74HC_HCT139_Q100 v.1	20140619	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Date of release: 29 February 2024