3A, 18V, 700kHz ACOT™ Synchronous Step-Down Converter

General Description

The RT7275/76 are high-performance 700kHz 3A step-down regulators with internal power switches and synchronous rectifiers. They feature quick transient response using their Advanced Constant On-Time (ACOT™) control architecture that provides stable operation with small ceramic output capacitors and without complicated external compensation, among other benefits. The input voltage range is from 4.5V to 18V and the output is adjustable from 0.765V to 8V.

The proprietary ACOT™ control improves upon other fast-response constant on-time architectures, achieving nearly constant switching frequency over line, load, and output voltage ranges. Since there is no internal clock, response to transients is nearly instantaneous and inductor current can ramp quickly to maintain output regulation without large bulk output capacitance. The RT7275/76 are stable with and optimized for ceramic output capacitors.

With internal 90mΩ switches and 60mΩ synchronous rectifiers, the RT7275/76 display excellent efficiency and good behavior across a range of applications, especially for low output voltages and low duty cycles. Cycle-by-cycle current limit, input under-voltage lock-out, externally-adjustable soft-start, output under- and over-voltage protection, and thermal shutdown provide safe and smooth operation in all operating conditions.

The RT7275 and RT7276 are each available in WDFN-10L 3x3 and PTSSOP-14 packages, with exposed thermal pads.

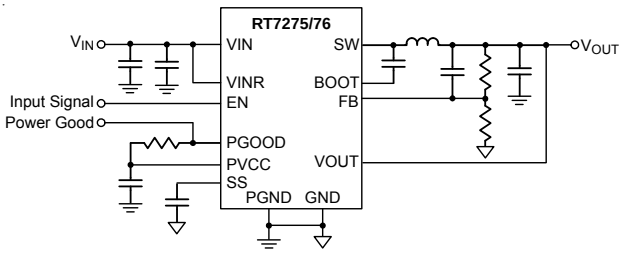
Features

- **Fast Transient Response**
- **Steady 700kHz Switching Frequency**
  - **At all Load Currents (RT7275)**
  - **Discontinuous Operating Mode at Light Load (RT7276)**
- **3A Output Current**
- **Advanced Constant On-Time (ACOT™) Control**
- **Optimized for Ceramic Output Capacitors**
- **4.5V to 18V Input Voltage Range**
- **Internal 90mΩ Switch and 60mΩ Synchronous Rectifier**
- **0.765V to 8V Adjustable Output Voltage**
- **Externally-Adjustable, Pre-Biased Compatible Soft-Start**
- **Cycle-by-Cycle Current Limit**
- **Optional Output Discharge Function (PTSSOP-14 Only)**
- **Output Over- and Under-Voltage Shut-Down**

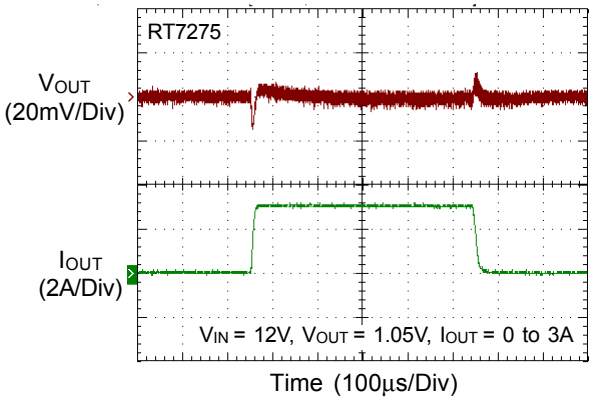
Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs
- Not Recommended for Sink/Source Applications

Simplified Application Circuit



Fast-Transient Response



Ordering Information

RT7275/76 □□

- Package Type
  - CP : TSSOP-14 (Exposed Pad)
  - QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
- Operating Mode
  - 75 : Continuous Switching Mode
  - 76 : Discontinuous Operating Mode at Light Load

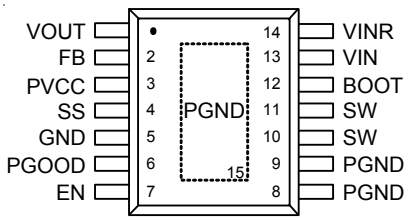
Note :

Richtek products are :

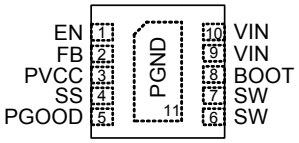
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

(TOP VIEW)



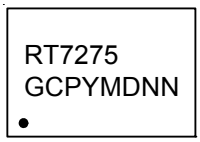
TSSOP-14 (Exposed Pad)



WDFN-10L 3x3

Marking Information

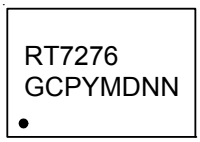
RT7275GCP



RT7275GCP : Product Number

YMDNN : Date Code

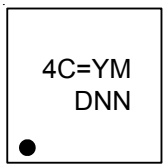
RT7276GCP



RT7276GCP : Product Number

YMDNN : Date Code

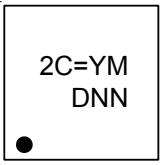
RT7275GQW



4C= : Product Code

YMDNN : Date Code

RT7276GQW



2C= : Product Code

YMDNN : Date Code

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN, VINR (TSSOP-14 (Exposed Pad)) ---------- –0.3V to 21V
- Switch Node, SW ---------- –0.8V to (V_{VIN} + 0.3V)
- Switch Node, SW (<10ns) ---------- –5V to 25V
- BOOT to SW ---------- –0.3V to 6V
- PVCC ---------- –0.3V to 6V
- PVCC to VIN (WDFN-10L 3x3) or VINR (TSSOP-14 (Exposed Pad)) ---------- –18V to 0.3V
- Other Pins ---------- –0.3V to 21V
- Power Dissipation, P_D @ T_A = 25°C
  - TSSOP-14 (Exposed Pad) ---------- 2.50W
  - WDFN-10L 3x3 ---------- 1.67W
- Package Thermal Resistance (Note 2)
  - TSSOP-14 (Exposed Pad), θ_{JA} ---------- 40°C/W
  - WDFN-10L 3x3, θ_{JA} ---------- 60°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature Range ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 4.5V to 18V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current							
Supply Current (Shutdown)			V_{EN} = 0V	--	1	10	μA
Supply Current (Quiescent)			V_{EN} = 3V, V_{FB} = 1V	--	0.7	--	mA
Logic Threshold							
EN Voltage	Logic High	V_{IH}		1.2	1.5	2	V
	Logic Low	V_{IL}		0.4	1.3	1.7	
V_{FB} Voltage and Discharge Resistance							
Feedback Threshold Voltage		V_{FB_TH}	4.5V ≤ V_{IN} ≤ 18V	0.757	0.765	0.773	V
Feedback Input Current		I_{FB}	V_{FB} = 0.8V	–0.1	0	0.1	μA
VOUT Discharge Resistance		R_{DIS}	V_{EN} = 0V, V_{VOUT} = 0.5V	--	50	100	Ω
PVCC Output							
PVCC Output Voltage		V_{PVCC}	6V ≤ V_{IN} ≤ 18V, 0 < I_{PVCC} < 5mA	4.7	5.1	5.5	V
PVCC Line Regulation			6V ≤ V_{IN} ≤ 18V, I_{PVCC} = 5mA	--	--	20	mV

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
PVCC Load Regulation			$0 < I_{PVCC} < 50mA$	--	--	40	mV
Output Current		I_{PVCC}	V_{IN} = 6V, V_{PVCC} = 4V	--	110	--	mA
On-Resistance ($R_{DS(ON)}$)							
Switch On Resistance	High-Side	$R_{DS(ON)\_H}$	For WDFN-10L 3x3	--	90	--	mΩ
	High-Side	$R_{DS(ON)\_H}$	For TSSOP-14 (Exposed Pad)	--	100	--	
	Low-Side	$R_{DS(ON)\_L}$		--	60	--	
High-Side Leakage			V_{IN} = 12V, V_{EN} = 0V	--	--	1	μA
Current Limit (upper threshold)		I_{LIM}	L_{SW} = 1.4μH	3.5	4.5	5.7	A
Thermal Shutdown							
Thermal Shutdown Threshold		T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	20	--	°C
On-Time and Off-Time Control							
On-Time		t_{ON}	V_{IN} = 12V, V_{OUT} = 1.05V	--	145	--	ns
Minimum On-Time		$t_{ON(MIN)}$		--	60	--	ns
Minimum Off-Time		$t_{OFF(MIN)}$		--	230	--	ns
Soft-Start							
SS Charge Current			V_{SS} = 0V	1.4	2	2.6	μA
SS Discharge Current			V_{SS} = 0.5V	0.05	0.1	--	mA
VIN UVLO							
UVLO Threshold			V_{VIN} / V_{VINR} rising, enable PVCC regulator	3.55	3.85	4.15	V
			Threshold hysteresis	--	0.3	--	
Power Good							
PGOOD Threshold			V_{FB} rising	85	90	95	%
			V_{FB} falling	--	85	--	
PGOOD Sink Current			PGOOD = 0.5V	--	5	--	mA
Output Under-Voltage and Over-Voltage Protection							
OVP Trip Threshold			V_{FB} rising	115	120	125	%
OVP Delay Time				--	5	--	μs
UVP Trip Threshold			V_{FB} falling	65	70	75	%
			Hysteresis	--	10	--	
UVP Delay Time				--	250	--	μs

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

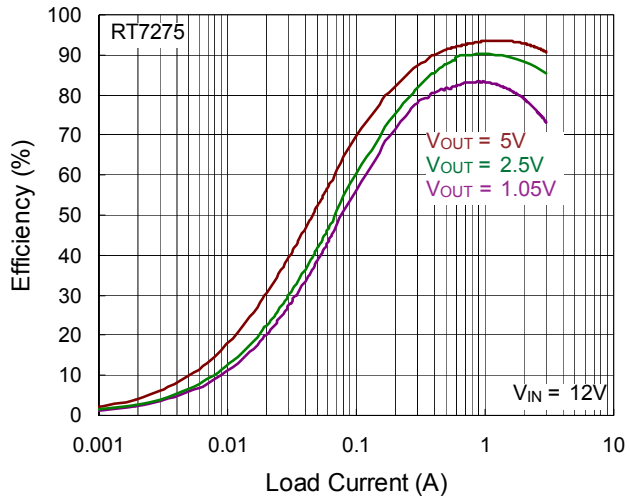
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package. The PCB copper area of exposed pad is 70mm^2.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

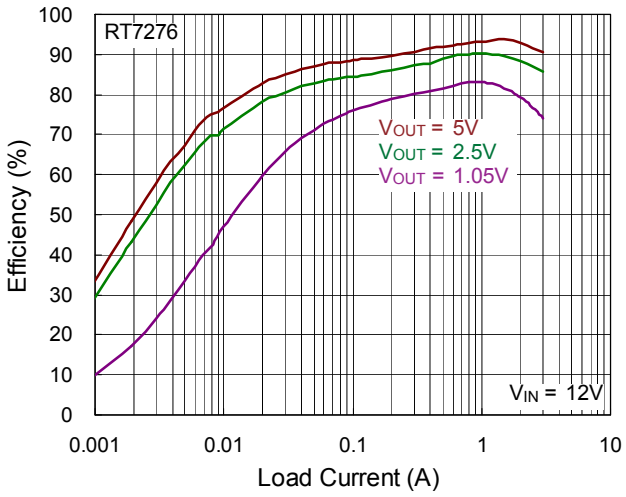
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

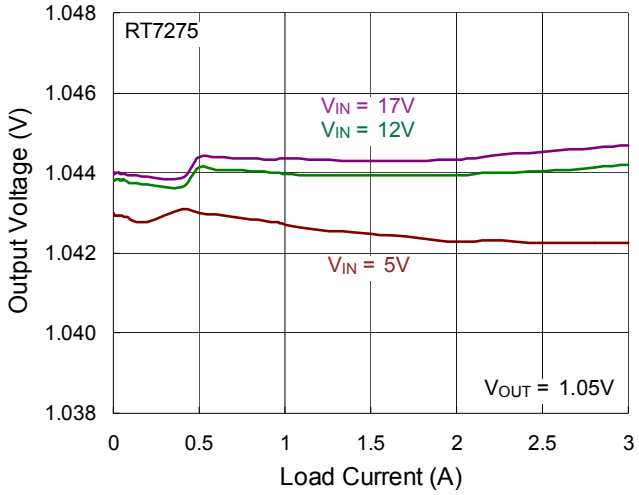
Efficiency vs. Load Current



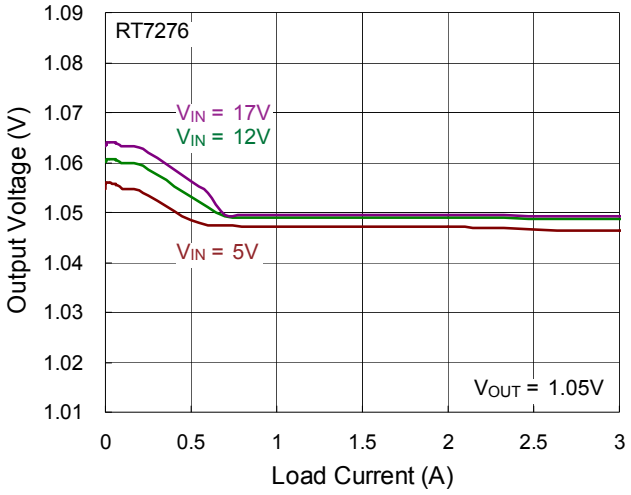
Efficiency vs. Load Current



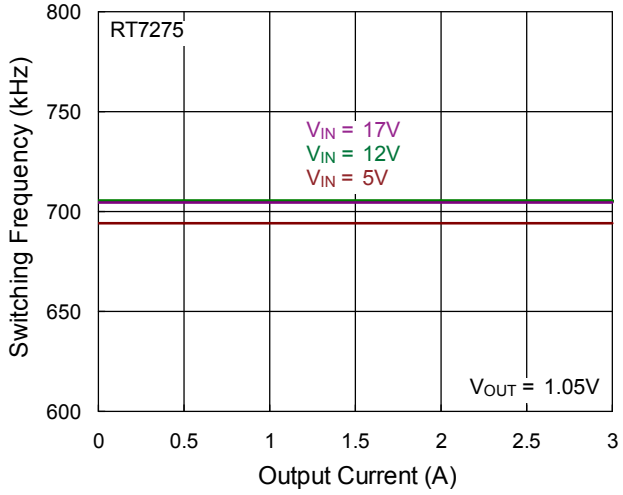
Output Voltage vs. Load Current



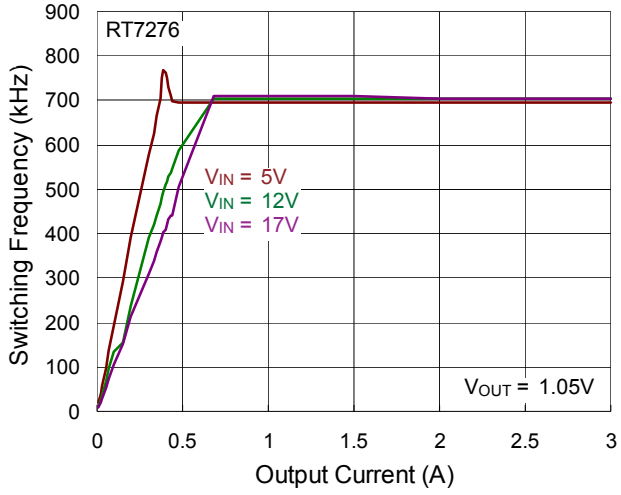
Output Voltage vs. Load Current



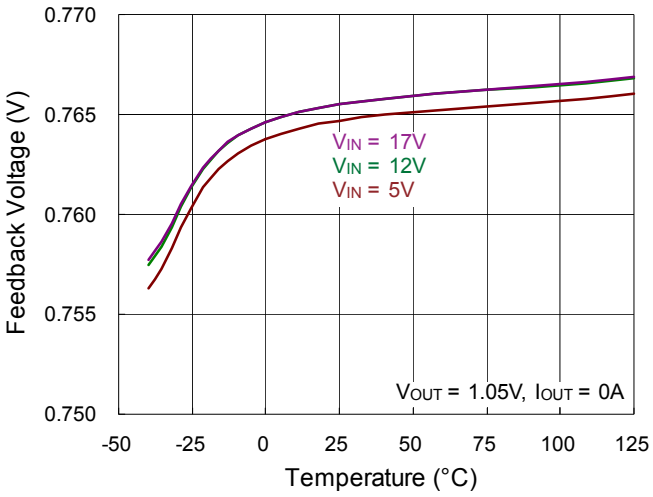
Switching Frequency vs. Load Current



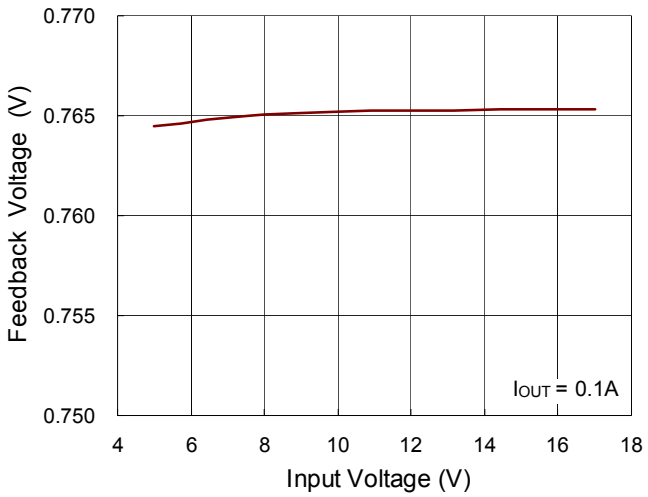
Switching Frequency vs. Output Current



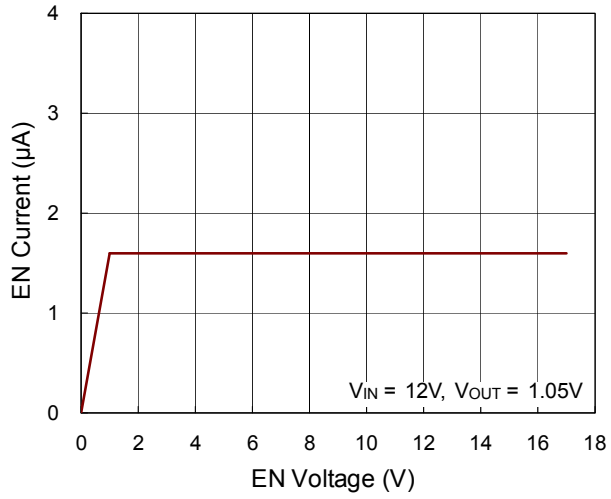
Feedback Voltage vs. Temperature



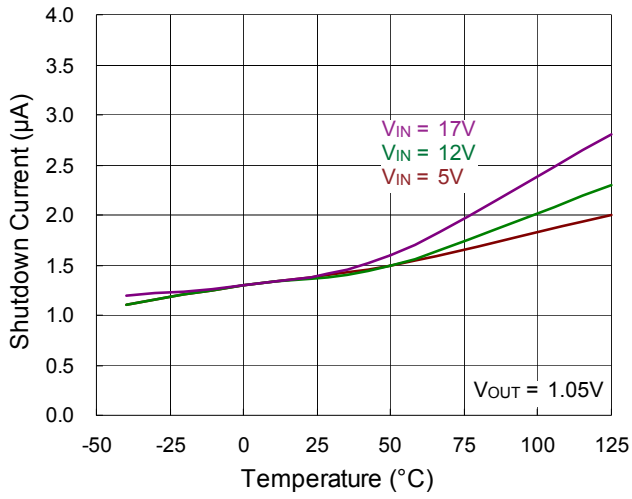
Feedback Voltage vs. Input Voltage



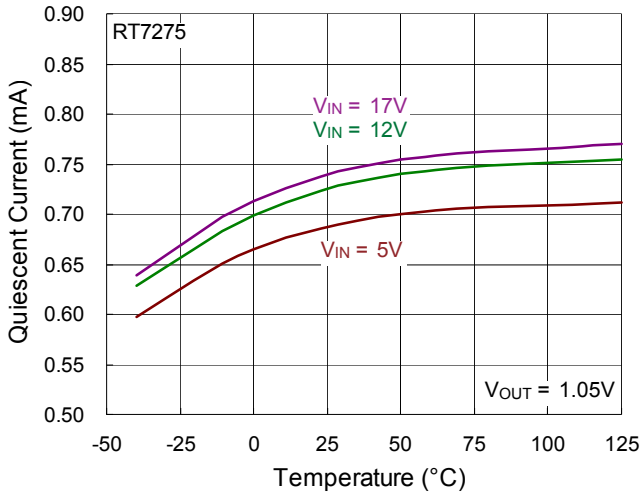
EN Current vs. EN Voltage



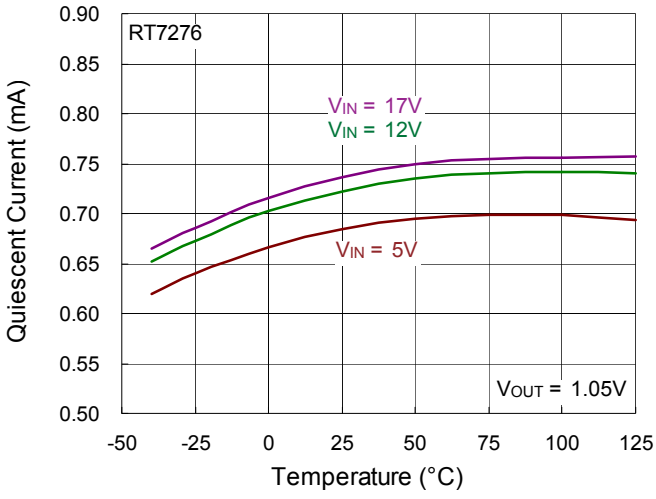
Shutdown Current vs. Temperature



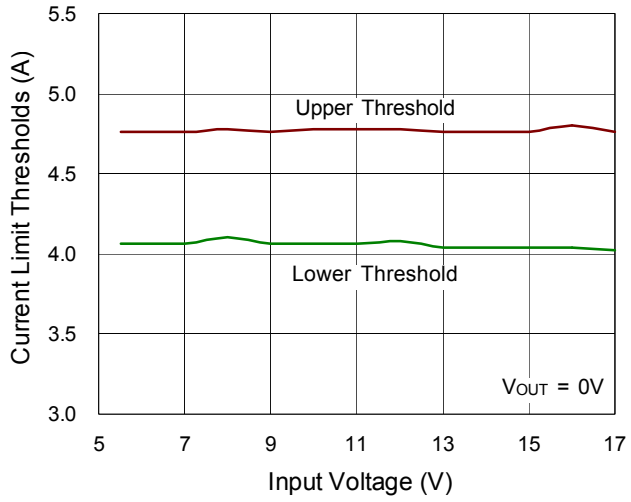
Quiescent Current vs. Temperature



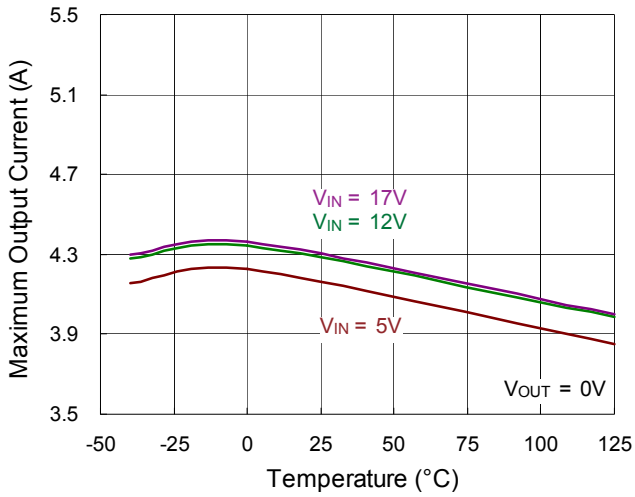
Quiescent Current vs. Temperature



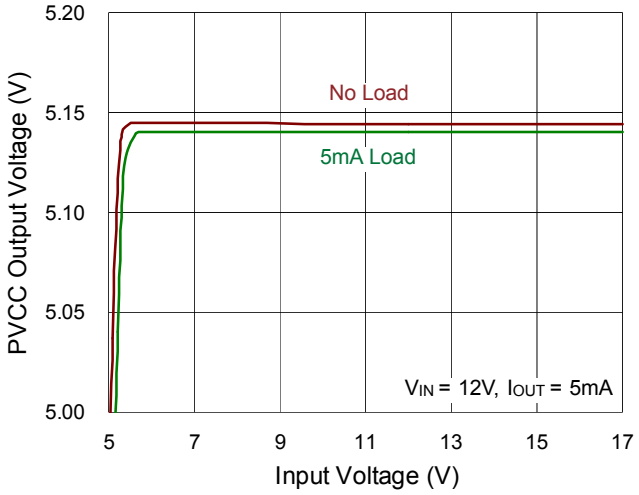
Current Limit Thresholds vs. Input Voltage



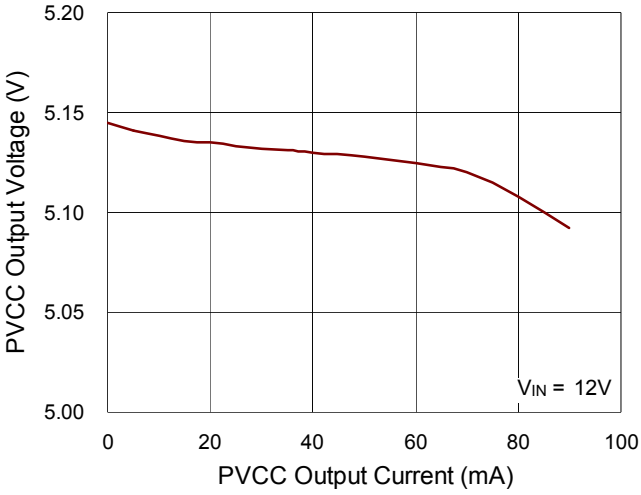
Maximum Output Current vs. Temperature



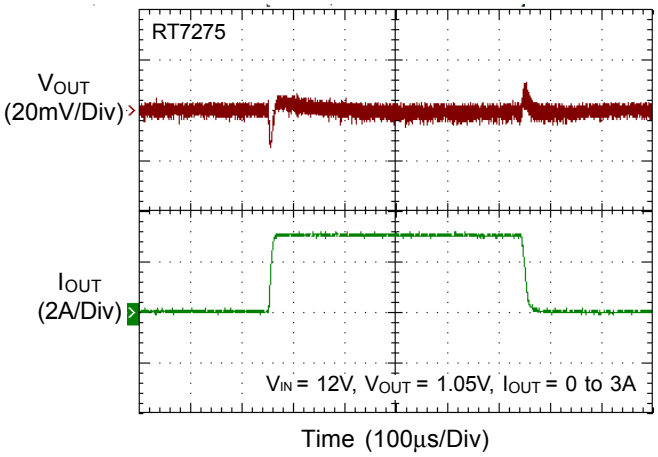
PVCC Output Voltage vs. Input Voltage



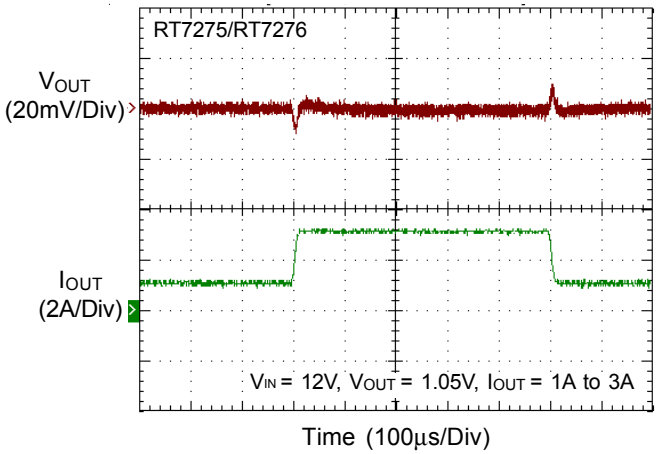
PVCC Output Voltage vs. Output Current



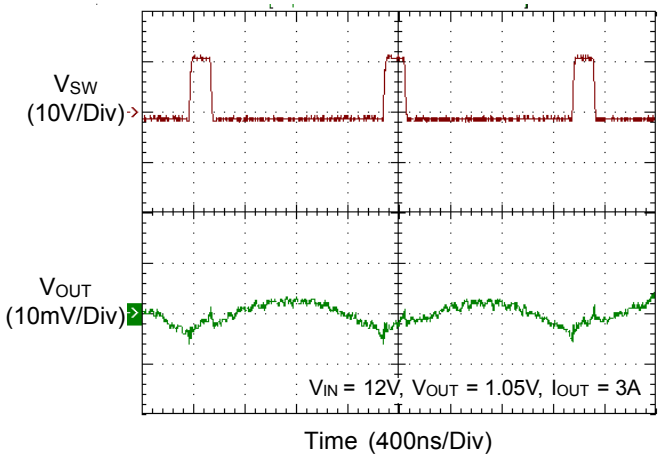
Load Transient Response



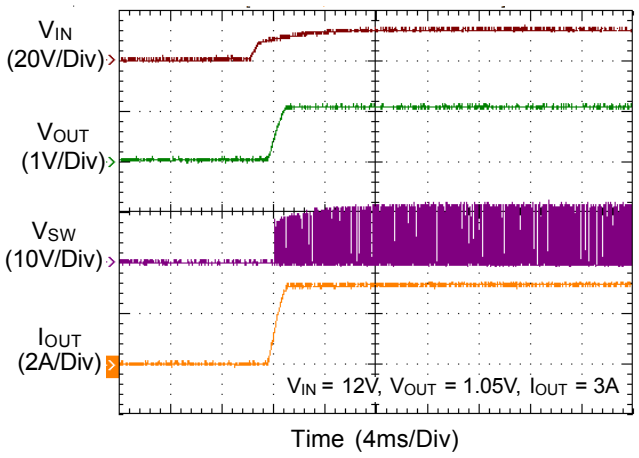
Load Transient Response



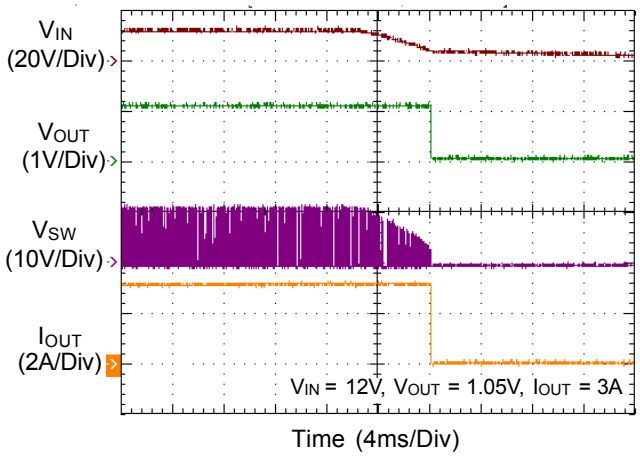
Output Ripple Voltage



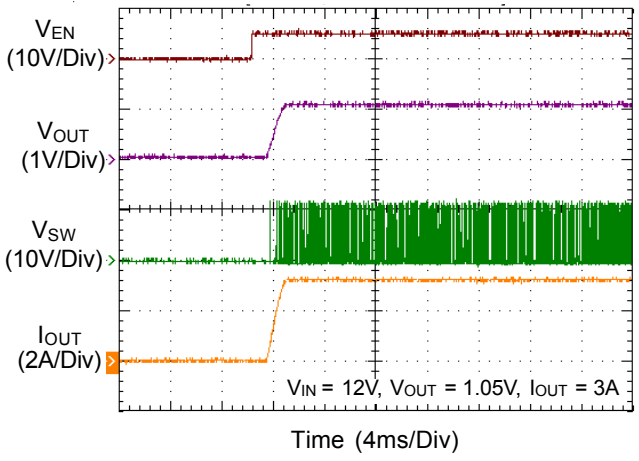
Power On from VIN



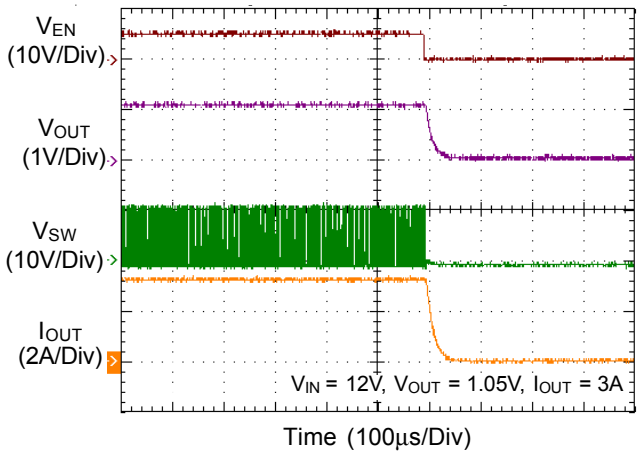
Power Off from VIN



Power On from EN



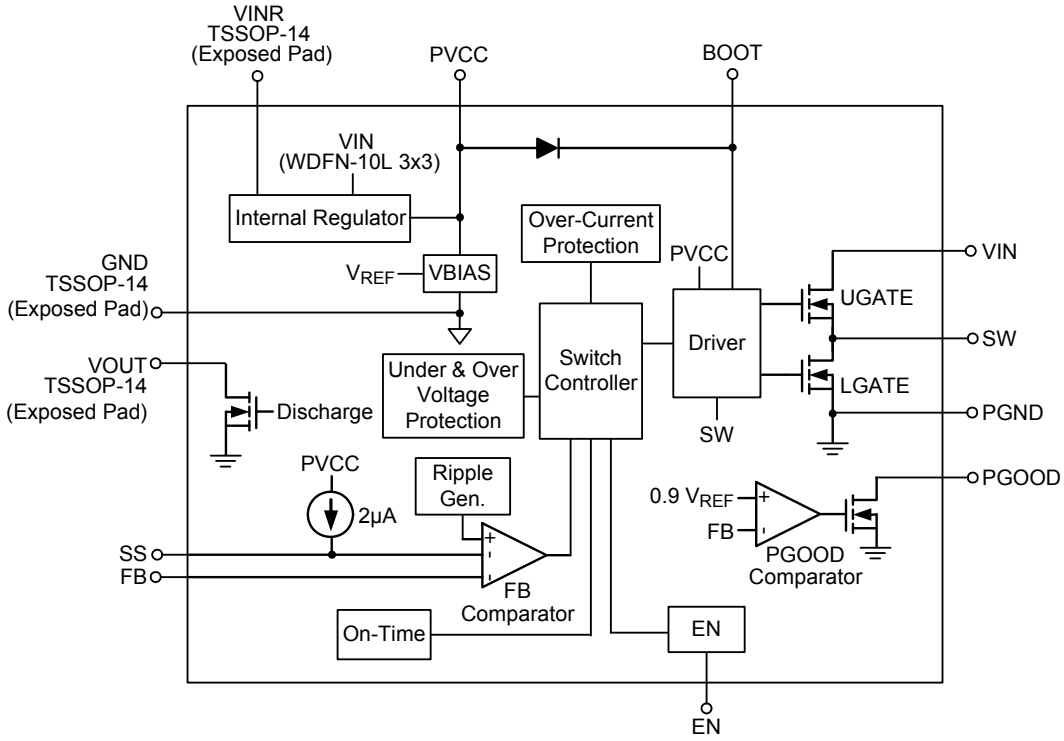
Power Off from EN



Functional Pin Description

Pin No.		Pin Name	Pin Function
TSSOP-14 (Exposed Pad)	WDFN-10L 3x3		
1	--	VOUT	Optional output voltage discharge connection. This open drain output connects to ground when the device is disabled. If output voltage discharge is desired, connect VOUT to the output voltage.
2	2	FB	Feedback input voltage. Connect FB to the midpoint of the external feedback resistive divider to sense the output voltage. Place the resistive divider within 5mm from the FB pin. The IC regulates V_{FB} at 0.765V (typical).
3	3	PVCC	Linear regulator output. PVCC is the output of the internal 5.1V linear regulator powered by VIN (WDFN-10L 3x3) or VINR (TSSOP-14 (Exposed Pad)). Connect a 1μF ceramic capacitor from PVCC to ground.
4	4	SS	Soft-start control. Connect an external capacitor between this pin and ground to set the soft-start time.
5	--	GND	Analog ground.
6	5	PGOOD	Open drain power-good output. PGOOD connects to PGND whenever V_{FB} is less than 90% of its regulation threshold (typical).
7	1	EN	Enable control input. Connect EN to a logic-high voltage to enable the IC or to a logic-low voltage to disable. Do not leave this high impedance input unconnected.
8, 9, 15 (Exposed pad)	11 (Exposed pad)	PGND	Power ground. PGND connects to the Source of the internal N-channel MOSFET synchronous rectifier and to other power ground nodes of the IC. The exposed pad and the 2 PGND pins (TSSOP-14 (Exposed Pad)) should be well soldered to the input and output capacitors and to a large PCB area for good power dissipation.
10, 11	6, 7	SW	Switching node. SW is the Source of the internal N-channel MOSFET switch and the Drain of the internal N-channel MOSFET synchronous rectifier. Connect SW to the inductor with a wide short PCB trace and minimize its area to reduce EMI.
12	8	BOOT	Bootstrap supply for high-side gate driver. Connect a 0.1μF capacitor between BOOT and SW to power the internal gate driver.
13	9, 10	VIN	Power input. VIN is the Drain of the internal N-channel MOSFET switch. Connect VIN to the input capacitor. For the WDFN-10L 3x3 package, VIN also supplies power to the internal linear regulator.
14	--	VINR	Internal linear regulator supply input. For the TSSOP-14 (Exposed Pad) package, VINR supplies power for the internal linear regulator that powers the IC. Connect VIN to the input voltage and bypass to ground with a 0.1μF ceramic capacitor.

Functional Block Diagram



Detailed Description

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The proprietary ACOT™ control scheme improves upon other constant on-time architectures, achieving nearly constant switching frequency over line, load, and output voltage ranges. The RT7275/76 are optimized for ceramic output capacitors. Since there is no internal clock, response to transients is nearly instantaneous and inductor current can ramp quickly to maintain output regulation without large bulk output capacitance.

Constant On-Time (COT) Control

The heart of any COT architecture is the on-time one-shot. Each on-time is a pre-determined "fixed" period that is triggered by a feedback comparator. This robust arrangement has high noise immunity and is ideal for low duty cycle applications. After the on-time one-shot period, there is a minimum off-time period before any further regulation decisions can be considered. This arrangement avoids the need to make any decisions during the noisy time periods just after switching events, when the switching node (SW) rises or falls. Because there is no fixed clock, the high-side switch can turn on almost immediately after load transients and further switching pulses can ramp the inductor current higher to meet load requirements with minimal delays.

Traditional current mode or voltage mode control schemes typically must monitor the feedback voltage, current signals (also for current limit), and internal ramps and compensation signals, to determine when to turn off the high-side switch and turn on the synchronous rectifier. Weighing these small signals in a switching environment is difficult to do just after switching large currents, making those architectures problematic at low duty cycles and in less than ideal board layouts.

Because no switching decisions are made during noisy time periods, COT architectures are preferable in low duty cycle and noisy applications. However, traditional COT control schemes suffer from some disadvantages that preclude their use in many cases. Many applications require a known switching frequency range to avoid interference with other sensitive circuitry. True constant on-time control, where the on-time is actually fixed, exhibits variable switching frequency. In a step-down converter, the duty factor is proportional to the output voltage and inversely proportional to the input voltage. Therefore, if the on-time is fixed, the off-time (and therefore the frequency) must change in response to changes in input or output voltage.

Modern pseudo-fixed frequency COT architectures greatly improve COT by making the one-shot on-time proportional to V_{OUT} and inversely proportional to V_{IN}. In this way, an on-time is chosen as approximately what it would be for an ideal fixed-frequency PWM in similar input/output voltage conditions. The result is a big improvement but the switching frequency still varies considerably over line and load due to losses in the switches and inductor and other parasitic effects.

Another problem with many COT architectures is their dependence on adequate ESR in the output capacitor, making it difficult to use highly-desirable, small, low-cost, but low-ESR ceramic capacitors. Most COT architectures use AC current information from the output capacitor, generated by the inductor current passing through the ESR, to function in a way like a current mode control system. With ceramic capacitors the inductor current information is too small to keep the control loop stable, like a current mode system with no current information.

ACOT™ Control Architecture

Making the on-time proportional to V_{OUT} and inversely proportional to V_{IN} is not sufficient to achieve good constant-frequency behavior for several reasons. First, voltage drops across the MOSFET switches and inductor cause the effective input voltage to be less than the measured input voltage and the effective output voltage to be greater than the measured output voltage. As the load changes, the switch voltage drops change causing a switching frequency variation with load current. Also, at light loads if the inductor current goes negative, the switch dead-time between the synchronous rectifier turn-off and the high-side switch turn-on allows the switching node to rise to the input voltage. This increases the effective on-time and causes the switching frequency to drop noticeably.

One way to reduce these effects is to measure the actual switching frequency and compare it to the desired range. This has the added benefit eliminating the need to sense the actual output voltage, potentially saving one pin connection. ACOT™ uses this method, measuring the actual switching frequency and modifying the on-time with a feedback loop to keep the average switching frequency in the desired range.

To achieve good stability with low-ESR ceramic capacitors, ACOT™ uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.

ACOT™ One-Shot Operation

The RT7275/76 control algorithm is simple to understand. The feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference the on-time one-shot is triggered, as long as the minimum off-time one-shot is clear and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allow the feedback voltage and current sense signals to settle. The minimum off-time is kept short (230ns typical) so that rapidly-repeated on-times can raise the inductor current quickly when needed.

Discontinuous Operating Mode (RT7276 Only)

After soft start, the RT7275 operates in fixed frequency mode to minimize interference and noise problems. The RT7276 uses variable-frequency discontinuous switching at light loads to improve efficiency. During discontinuous switching, the on-time is immediately increased to add "hysteresis" to discourage the IC from switching back to continuous switching unless the load increases substantially.

The IC returns to continuous switching as soon as an on-time is generated before the inductor current reaches zero. The on-time is reduced back to the length needed for 700kHz switching and encouraging the circuit to remain in continuous conduction, preventing repetitive mode transitions between continuous switching and discontinuous switching.

Current Limit

The RT7275/76 current limit is a cycle-by-cycle "valley" type, measuring the inductor current through the synchronous rectifier during the off-time while the inductor current ramps down. The current is determined by measuring the voltage between source and drain of the synchronous rectifier, adding temperature compensation for greater accuracy. If the current exceeds the upper current limit, the on-time one-shot is inhibited until the inductor current ramps down below the upper current limit plus a wide hysteresis band of about 1A and drops below the lower current limit level. Thus, only when the inductor current is well below the upper current limit is another on-time permitted. This arrangement prevents the average output current from greatly exceeding the guaranteed upper current limit value, as typically occurs with other valley-type current limits. If the output current exceeds the available inductor current (controlled by the current limit mechanism), the output voltage will drop. If it drops below the output under-voltage protection level (see next section) the IC will stop switching to avoid excessive heat.

The RT7275 also includes a negative current limit to protect the IC against sinking excessive current and possibly damaging the IC. If the voltage across the synchronous rectifier indicates the negative current is too high, the synchronous rectifier turns off until after the next high-side on-time. The RT7276 does not sink current and therefore does not need a negative current limit.

Output Over-Voltage Protection and Under-Voltage Protection

The RT7275/76 include output over-voltage protection (OVP). If the output voltage rises above the regulation level, the high-side switch naturally remains off and the synchronous rectifier turns on. If the output voltage remains high the synchronous rectifier remains on until the inductor current reaches the negative current limit (RT7275) or until it reaches zero (RT7276). If the output voltage remains high, the IC's switches remain off. If the output voltage exceeds the OVP trip threshold for longer than 5μs (typical), the IC's OVP is triggered.

The RT7275/76 include output under-voltage protection (UVP). If the output voltage drops below the UVP trip threshold for longer than 250μs (typical) the IC's UVP is triggered.

There are two different behaviors for OVP and UVP events, one for the WDFN-10L 3x3 packages and one for the TSSOP-14 (Exposed Pad) packages.

- **Hiccup Mode (WDFN-10L 3x3 Only)**
- The RT7275GQW/RT7276GQW, use hiccup mode OVP and UVP. When the protection function is triggered, the IC will shut down for a period of time and then attempt to recover automatically. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the overload or short circuit is removed. During hiccup mode, the shutdown time is determined by the capacitor at SS. A 0.5μA current source discharges V_{SS} from its starting voltage (normally V_{PVCC}). The IC remains shut down until V_{SS} reaches 0.2V, about 40ms for a 3.9nF capacitor. At that point the IC begins to charge the SS capacitor at 2μA, and a normal start-up occurs. If the fault remains, OVP and UVP protection will be enabled when V_{SS} reaches 2.2V (typical). The IC will then shut down and discharge the SS capacitor from the 2.2V level, taking about 17ms for a 3.9nF SS capacitor.

- **Latch-Off Mode (TSSOP-14 (Exposed Pad) Only)**
- The RT7275GCP/RT7276GCP, use latch-off mode OVP and UVP. When the protection function is triggered the IC will shut down. The IC stops switching, leaving both switches open, and is latched off. To restart operation, toggle EN or power the IC off and then on again.

Shut-Down, Start-Up and Enable (EN)

The enable input (EN) has a logic-low level of 0.4V. When V_{EN} is below this level the IC enters shutdown mode and supply current drops to less than 10μA. When V_{EN} exceeds its logic-high level of 2V the IC is fully operational.

Between these 2 levels there are 2 thresholds (1.2V typical and 1.4V typical). When V_{EN} exceeds the lower threshold the internal bias regulators begin to function and supply current increases above the shutdown current level. Switching operation begins when V_{EN} exceeds the upper threshold. Unlike many competing devices, EN is a high voltage input that can be safely connected to VIN (up to 18V) for automatic start-up.

Input Under-Voltage Lock-Out

In addition to the enable function, the RT7275/76 feature an under-voltage lock-out (UVLO) function that monitors the internal linear regulator output (PVCC). To prevent operation without fully-enhanced internal MOSFET switches, this function inhibits switching when PVCC drops below the UVLO-falling threshold. The IC resumes switching when PVCC exceeds the UVLO-rising threshold.

Soft-Start (SS)

The RT7275/76 soft-start uses an external pin (SS) to clamp the output voltage and allow it to slowly rise. After V_{EN} is high and PVCC exceeds its UVLO threshold, the IC begins to source 2μA from the SS pin. An external capacitor at SS is used to adjust the soft-start timing. The available capacitance range is from 2.7nF to 220nF. Do not leave SS unconnected.

During start-up, while the SS capacitor charges, the RT7275/76 operate in discontinuous switching mode with very small pulses. This prevents negative inductor currents and keeps the circuit from sinking current. Therefore, the output voltage may be pre-biased to some positive level before start-up. Once the V_{SS} ramp charges enough to raise the internal reference above the feedback voltage, switching will begin and the output voltage will smoothly rise from the pre-biased level to its regulated level. After V_{SS} rises above about 2.2V output over-and under-voltage protections are enabled and the RT7275 begins continuous-switching operation.

Internal Regulator (PVCC)

An internal linear regulator (PVCC) produces a 5.1V supply from VIN that powers the internal gate drivers, PWM logic, reference, analog circuitry, and other blocks. If VIN is 6V or greater, PVCC is guaranteed to provide significant power for external loads.

PGOOD Comparator

PGOOD is an open drain output controlled by a comparator connected to the feedback signal. If FB exceeds 90% of the internal reference voltage, PGOOD will be high impedance. Otherwise, the PGOOD output is connected to PGND.

External Bootstrap Capacitor (C6)

Connect a 0.1μF low ESR ceramic capacitor between BOOT and SW. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel MOSFET switch.

Over-Temperature Protection

The RT7275/76 includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C the IC will resume normal operation with a complete soft-start. For continuous operation, provide adequate cooling so that the junction temperature does not exceed 150°C.

Typical Application Circuit

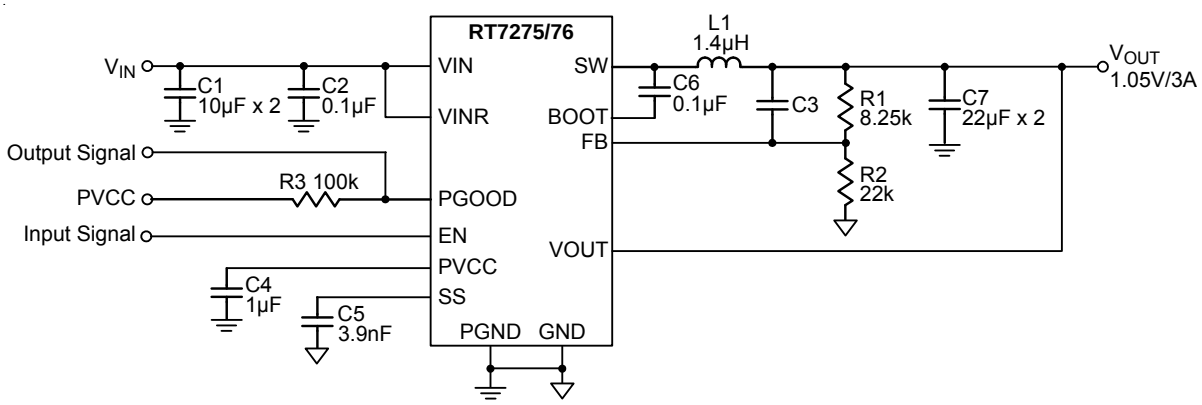


Table 1. Suggested Component Values (V_{IN} = 12V)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C3 (pF)	L1 (µH)	C7 (µF)
1	6.81	22.1	--	1.4	22 to 68
1.05	8.25	22.1	--	1.4	22 to 68
1.2	12.7	22.1	--	1.4	22 to 68
1.8	30.1	22.1	5 to 22	2	22 to 68
2.5	49.9	22.1	5 to 22	2	22 to 68
3.3	73.2	22.1	5 to 22	2	22 to 68
5	124	22.1	5 to 22	3.3	22 to 68
7	180	22.1	5 to 22	3.3	22 to 68

Design Procedure

Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response, but they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required and transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current (ΔI_L) about 20-50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency (f_{SW}), the maximum output current ($I_{OUT(MAX)}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current (ΔI_L) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and } I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output under-voltage shutdown feature make this unnecessary for most applications.

$I_{L(PEAK)}$ should not exceed the minimum value of IC's upper current limit level or the IC may not be able to meet the desired output current. If needed, reduce the inductor ripple current (ΔI_L) to increase the average inductor current (and the output current) while ensuring that $I_{L(PEAK)}$ does not exceed the upper current limit level.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses some type of ferrite core is usually best and a shielded core type, although possibly larger or more expensive, will probably give fewer EMI and other noise problems.

Considering the Typical Operating Circuit for 1.05V output at 3A and an input voltage of 12V, using an inductor ripple of 1A (33%), the calculated inductance value is :

$$L = \frac{1.05V \times (12V - 1.05V)}{12V \times 700kHz \times 1A} = 1.4\mu H$$

The ripple current was selected at 1A and, as long as we use the calculated 1.4µH inductance, that should be the actual ripple current amount. Typically the exact calculated inductance is not readily available and a nearby value is chosen. In this case 1.4µH was available and actually used in the typical circuit. To illustrate the next calculation, assume that for some reason is was necessary to select a 1.8µH inductor (for example). We would then calculate the ripple current and required peak current as below :

$$\Delta I_L = \frac{1.05V \times (12V - 1.05V)}{12V \times 700kHz \times 1.8\mu H} = 0.76A$$

$$\text{and } I_{L(PEAK)} = 3A + \frac{0.76}{2} = 3.38A$$

For the 1.8µH value, the inductor's saturation and thermal rating should exceed 3.38A. Since the actual value used was 1.4µH and the ripple current exactly 1A, the required peak current is 3.5A.

Input Capacitor Selection

The input filter capacitors are needed to smooth out the switched current drawn from the input power source and to reduce voltage ripple on the input. The actual capacitance value is less important than the RMS current rating (and voltage rating, of course). The RMS input ripple current (I_{RMS}) is a function of the input voltage, output voltage, and load current :

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{VIN} - V_{OUT})}}{V_{VIN}}$$

Ceramic capacitors are most often used because of their low cost, small size, high RMS current ratings, and robust surge current capabilities. However, take care when these

capacitors are used at the input of circuits supplied by a wall adapter or other supply connected through long, thin wires. Current surges through the inductive wires can induce ringing at the RT7275/76's input which could potentially cause large, damaging voltage spikes at VIN. If this phenomenon is observed, some bulk input capacitance may be required. Ceramic capacitors (to meet the RMS current requirement) can be placed in parallel with other types such as tantalum, electrolytic, or polymer (to reduce ringing and overshoot).

Choose capacitors rated at higher temperatures than required. Several ceramic capacitors may be paralleled to meet the RMS current, size, and height requirements of the application. The typical operating circuit uses two 10μF and one 0.1μF low ESR ceramic capacitors on the input.

Output Capacitor Selection

The RT7275/76 are optimized for ceramic output capacitors and best performance will be obtained using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

Output Ripple

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

For the Typical Operating Circuit for 1.05V output and an inductor ripple of 1A, with 2 x 22μF output capacitance each with about 5mΩ ESR including PCB trace resistance, the output voltage ripple components are :

$$V_{RIPPLE(ESR)} = 1A \times 2.5m\Omega = 2.5mV$$

$$V_{RIPPLE(C)} = \frac{1A}{8 \times 44\mu F \times 0.7MHz} = 4mV$$

$$V_{RIPPLE} = 2.5mV + 4mV = 6.5mV$$

Output Transient Undershoot and Overshoot

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's 700kHz switching frequency. But some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The output voltage transient undershoot and overshoot each have two components : the voltage steps caused by the output capacitor's ESR, and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formulas to check if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor:

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT™ control scheme will ramp the current using on-times spaced apart with minimum off-times, which is

as fast as allowed. Calculate the approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF(MIN)}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

For the Typical Operating Circuit for 1.05V output, the circuit has an inductor 1.4μH and 2 x 22μF output capacitance with 5mΩ ESR each. The ESR step is 3A x 2.5mΩ = 7.5mV which is small, as expected. The output voltage sag and soar in response to full 0A-3A-0A instantaneous transients are :

$$t_{ON} = \frac{1.05V}{12V \times 700kHz} = 125ns$$

$$\text{and } D_{MAX} = \frac{125ns}{125ns + 230ns} = 0.35$$

$$V_{SAG} = \frac{1.4\mu H \times (3A)^2}{2 \times 44\mu F \times (12V \times 0.35 - 1.05V)} = 45mV$$

$$V_{SOAR} = \frac{1.4\mu H \times (3A)^2}{2 \times 44\mu F \times 1.05V} = 136mV$$

The sag is about 4% of the output voltage and the soar is a full 13% of the output voltage. The ESR step is negligible here but it does partially add to the soar, so keep that in mind whenever using higher-ESR output capacitors.

The soar is typically much worse than the sag in high-input, low-output step-down converters because the high input voltage demands a large inductor value which stores lots of energy that is all transferred into the output if the load stops drawing current. Also, for a given inductor, the soar for a low output voltage is a greater voltage change and an even greater percentage of the output voltage. This is illustrated by comparing the previous to the next example.

The Typical Operating Circuit for 12V to 3.3V with a 2μH inductor and 2 x 22μF output capacitance can be used to illustrate the effect of a higher output voltage. The output voltage sag and soar in response to full 0A-3A-0A instantaneous transients are calculated as follows :

$$t_{ON} = \frac{3.3V}{12V \times 700kHz} = 392ns$$

$$\text{and } D_{MAX} = \frac{392ns}{392ns + 230ns} = 0.63$$

$$V_{SAG} = \frac{2\mu H \times (3A)^2}{2 \times 44\mu F \times (12V \times 0.63 - 3.3V)} = 48mV$$

$$V_{SOAR} = \frac{2\mu H \times (3A)^2}{2 \times 44\mu F \times 3.3V} = 62mV$$

In this case the sag is about 1.5% of the output voltage and the soar is only 2% of the output voltage.

Any sag is always short-lived, since the circuit quickly sources current to regain regulation in only a few switching cycles. With the RT7275, any overshoot transient is typically also short-lived since the converter will sink current, reversing the inductor current sharply until the output reaches regulation again. The RT7276's discontinuous operation at light loads prevents sinking current so, for that IC, the output voltage will soar until load current or leakage brings the voltage down to normal.

Most applications never experience instantaneous full load steps and the RT7275/76's high switching frequency and fast transient response can easily control voltage regulation at all times. Also, since the sag and soar both are proportional to the square of the load change, if load steps were reduced to 1A (from the 3A examples preceding) the voltage changes would be reduced by a factor of almost ten. For these reasons sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

In any application with large quick transients, always calculate soar to make sure that over-voltage protection will not be triggered. Under-voltage is not likely since the threshold is very low (70%), that function has a long delay (250μs), and the IC will quickly return the output to regulation. Over-voltage protection has a minimum threshold of 115% and short delay of 5μs and can actually be triggered by incorrect component choices, particularly for the RT7276 which does not sink current.

Output Capacitors Stability Criteria

The RT7275/76's ACOT™ control architecture uses an internal virtual inductor current ramp and other compensation that ensures stability with any reasonable output capacitor. The internal ramp allows the IC to operate with very low ESR capacitors and the IC is stable with very small capacitances. Therefore, output capacitor selection is nearly always a matter of meeting output voltage ripple and transient response requirements, as discussed in the previous sections. For the sake of the unusual application where ripple voltage is unimportant and there are few transients (perhaps battery charging or LED lighting) the stability criteria are discussed below.

The equations giving the minimum required capacitance for stable operation include a term that depends on the output capacitor's ESR. The higher the ESR, the lower the capacitance can be and still ensure stability. The equations can be greatly simplified if the ESR term is removed by setting ESR to zero. The resulting equation gives the worst-case minimum required capacitance and it is usually sufficiently small that there is usually no need for the more exact equation.

The required output capacitance (C_{OUT}) is a function of the inductor value (L) and the input voltage (V_{IN}) :

$$C_{OUT} \geq \frac{5.23 \times 10^{-11}}{V_{IN} \times L}$$

The worst-case high capacitance requirement is for low VIN and small inductance, so a 5V to 3.3V converter is used for an example. Using the inductance equation in a previous section to determine the required inductance :

$$L = \frac{3.3V \times (5V - 3.3V)}{5V \times 700kHz \times 1A} = 1.6\mu H$$

Therefore, the required minimum capacitance for the 5V to 3.3V converter is :

$$C_{OUT} \geq \frac{5.23 \times 10^{-11}}{5V \times 1.6\mu H} = 6.6\mu F$$

Using the 12V to 1.05V typical application as another example :

$$C_{OUT} \geq \frac{5.24 \times 10^{-11}}{12V \times 1.4\mu H} = 3.1\mu F$$

Any ESR in the output capacitor lowers the required minimum output capacitance, sometimes considerably. For the rare application where that is needed and useful, the equation including ESR is given here :

$$C_{OUT} \geq \frac{V_{OUT}}{2 \times f_{SW} \times V_{IN} \times (R_{ESR} + 13647 \times L \times V_{OUT})}$$

As can be seen, setting R_{ESR} to zero and simplifying the equation yields the previous simpler equation. To allow for the capacitor's temperature and bias voltage coefficients, use at least double the calculated capacitance and use a good quality dielectric such as X5R or X7R with an adequate voltage rating since ceramic capacitors exhibit considerable capacitance reduction as their bias voltage increases.

Feed-Forward Capacitor (C3)

The RT7275/76 are optimized for ceramic output capacitors and for low duty cycle applications. This optimization makes circuit stability easy to achieve with reasonable output capacitors. However, the optimization affects the quality factor (Q) of the circuit and therefore its transient response. To avoid an under-damped response (high Q) and its potential ringing, the internal compensation was chosen to achieve perfect damping for low output voltages, where the FB divider has low attenuation (V_{OUT} is close to V_{REF}). For high-output voltages, with high feedback attenuation, the circuit's response becomes over-damped and transient response can be slowed. In high-output voltage circuits (V_{OUT} > 1.5V) transient response is improved by adding a small "feed-forward" capacitor (C3) across the upper FB divider resistor, to increase the circuit's Q and reduce damping to speed up the transient response without affecting the steady-state stability of the circuit. Choose a capacitor value that gives, together with the divider impedance at FB, a time-constant between 100ns and 0.5μs. The divider impedance at FB is R1 in parallel with R2. C3 can be safely left out in low-output voltage circuits and if fast transient response is not required.

Applications Information

Current-Sinking Applications (RT7275)

The RT7275's is not recommended for current sinking applications even though its continuous switching operation allows the IC to sink some current. Sinking enables a fast recovery from output voltage overshoot caused by load transients and is normally useful for applications requiring negative currents, such as DDR V_{TT} bus termination applications and changing-output voltage applications where the output voltage needs to slew quickly from one voltage to another. However, the IC's negative current limit is set low (about 1.6A) and the current limit behavior latches the synchronous rectifier off until the high-side switch's next pulse, to prevent the possibility of IC damage from large negative currents. Therefore, sinking current is not necessarily available at all times.

If implementing applications where current-sinking may occur, take care to allow for the current that is delivered to the input supply. A step-down converter in sinking operation functions like a backwards step-up converter. The current that is sunk at its output terminals is delivered up to its input terminals. If this current has no outlet, the input voltage will rise.

A good arrangement for long-term sinking applications is for a sinking supply (supply A) that is sinking current sourced from supply B, to both be powered by the same input supply. That way, any current delivered back to the input by supply A is current that just left the input through supply B. In this way, the current simply makes a round trip and the input supply will not rise.

In cases where this is not possible, make sure that there are sufficient other loads on the input supply to prevent that supply's voltage from rising high enough to cause damage to itself or any of its loads. In cases where the sinking is not long-term, such as output-voltage slewing applications, make sure there is sufficient input capacitance to control any input voltage rise. The worst-case voltage rise is :

$$\Delta V_{IN} = \frac{C_{OUT} \times \Delta V_{OUT}}{C_{IN}}$$

Soft-Start

The RT7275/76 contains an external soft-start clamp that gradually raises the output voltage. The soft-start timing can be programmed by the external capacitor between SS pin and GND. The chip provides a 2μA charge current for the external capacitor. If a 3.9nF capacitor is used, the soft-start will be 2.6ms (typ.). The available capacitance range is from 2.7nF to 220nF.

$$t_{SS}\ (ms) = \frac{C5\ (nF) \times 1.365}{I_{SS}\ (\mu A)}$$

Enable Operation (EN)

For automatic start-up the high-voltage EN pin can be connected to V_{IN}, either directly or through a 100kΩ resistor. Its large hysteresis band makes EN useful for simple delay and timing circuits. EN can be externally pulled to V_{IN} by adding a resistor-capacitor delay (R_{EN} and C_{EN} in Figure 1). Calculate the delay time using EN's internal threshold where switching operation begins (1.4V, typical).

An external MOSFET can be added to implement digital control of EN when no system voltage above 2V is available (Figure 2). In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between VIN and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin. To prevent enabling circuit when VIN is smaller than the VOUT target value or some other desired voltage level, a resistive voltage divider can be placed between the input voltage and ground and connected to EN to create an additional input under-voltage lockout threshold (Figure 3).

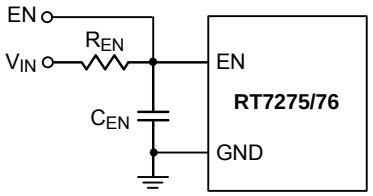


Figure 1. External Timing Control

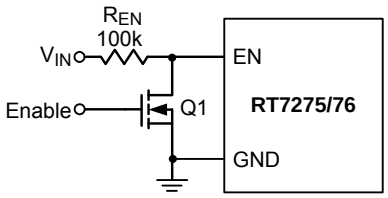


Figure 2. Digital Enable Control Circuit

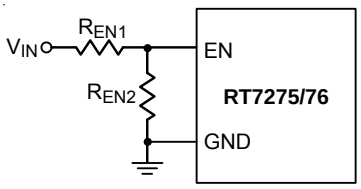


Figure 3. Resistor Divider for Lockout Threshold Setting

Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set according to the following equation :

$$V_{OUT} = 0.765 \times (1 + \frac{R1}{R2})$$

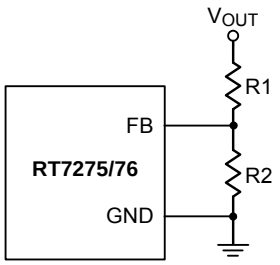


Figure 4. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R2 between 10kΩ and 100kΩ to minimize power consumption without excessive noise pick-up and calculate R1 as follows :

$$R1 = \frac{R2 \times (V_{OUT} - 0.765V)}{0.765V}$$

For output voltage accuracy, use divider resistors with 1% or better tolerance.

Under-Voltage Lockout Protection

The RT7275/76 feature an under-voltage lock-out (UVLO) function that monitors the internal linear regulator output (PVCC) and prevents operation if V_{PVCC} is too low. In some multiple input voltage applications, it may be desirable to use a power input that is too low to allow V_{PVCC} to exceed the UVLO threshold. In this case, if there is another low-power supply available that is high enough to operate the PVCC regulator, connecting that supply to VINR (TSSOP-14 (Exposed Pad) only) will allow the IC to operate, using the lower-voltage high-power supply for the DC-DC power path. Because of the internal linear regulator, any supply regulated or unregulated) between 4.5V and 18V will operate the IC.

External BOOT Bootstrap Diode

When the input voltage is lower than 5.5V it is recommended to add an external bootstrap diode between VIN (or VINR) and the BOOT pin to improve enhancement of the internal MOSFET switch and improve efficiency. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.

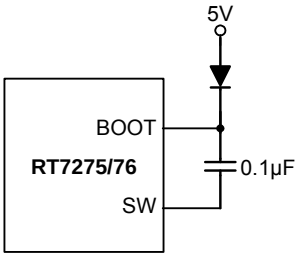


Figure 5. External Bootstrap Diode

External BOOT Capacitor Series Resistance

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. Switch turn-on is when most EMI occurs since V_{SW} rises rapidly. During switch turn-off, SW is discharged relatively slowly by the inductor current during the dead-time between high-side and low-side switch on-times.

In some cases it is desirable to reduce EMI further, at the expense of some additional power dissipation. The switch turn-on can be slowed by placing a small (<10Ω) resistance between BOOT and the external bootstrap capacitor. This will slow the high-side switch turn-on and V_{SW}'s rise. To remove the resistor from the capacitor charging path (avoiding poor enhancement due to under-charging the BOOT capacitor), use the external diode shown in figure 5 to charge the BOOT capacitor and place the resistance between BOOT and the capacitor/diode connection.

PVCC Capacitor Selection

Decouple PVCC to PGND with a 1µF ceramic capacitor. High grade dielectric (X7R, or X5R) ceramic capacitors are recommended for their stable temperature and bias voltage characteristics.

Thermal Considerations

The maximum power dissipation depends on the thermal resistance of the IC package and the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For the TSSOP-14 (Exposed Pad) package the thermal resistance, θ_{JA}, is 40°C/W on a standard JEDEC 51-7 four-layer thermal test board. For the WDFN-10L 3x3 package the thermal resistance, θ_{JA}, is 60°C/W on a standard JEDEC 51-7 four-layer thermal test board. These standard thermal test layouts have a very large area with long 2oz. copper traces connected to each IC pin and very large, unbroken 1oz. internal power and ground planes. Meeting the performance of the standard thermal test board in a typical tiny board area requires wide copper traces well-connected to the IC's backside pad leading to exposed copper areas on the component side of the board as well as good thermal vias from the backside pad connecting to a wide inner-layer ground plane and, perhaps, to an exposed copper area on the board's solder side. Using the backside tab in this way, 40°C/W is achievable in a small area with either package.

The maximum power dissipation at T_A = 25°C can be calculated by the following formulas:

$P_{D(MAX)}$ = (125°C – 25°C) / (40°C/W) = 2.50W for TSSOP-14 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (60°C/W) = 1.67W for WDFN-10L 3x3 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curves in Figure 6 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

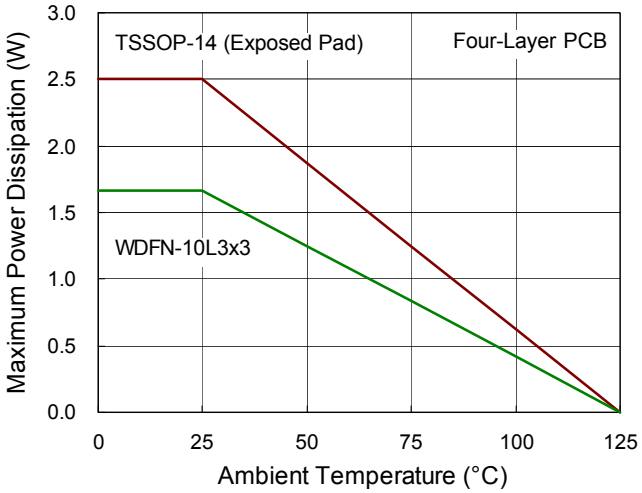
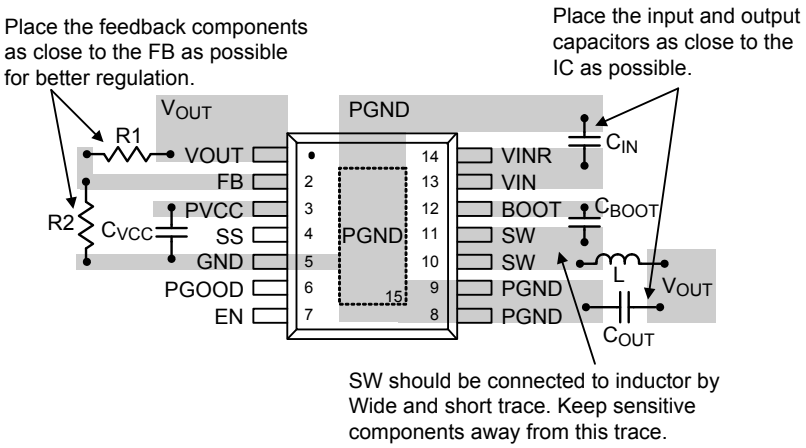


Figure 6. Derating Curve of Maximum Power Dissipation

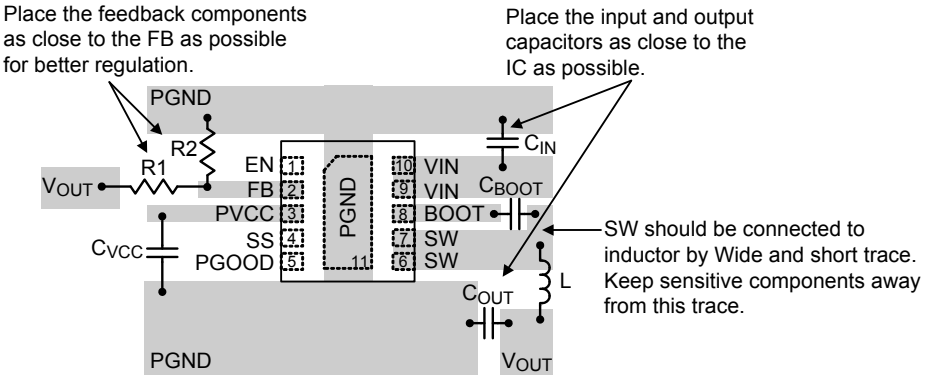
Layout Considerations

Follow the PCB layout guidelines for optimal performance of the RT7275/76.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and PGND).
- The high-frequency switching node (SW) has large voltage swings and fast edges and can easily radiate noise to adjacent components. Keep its area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Keep sensitive components away from the SW node or provide ground traces between for shielding, to prevent stray capacitive noise pickup.
- Connect the feedback network to the output capacitors rather than the inductor. Place the feedback components near the FB pin.
- The exposed pad, PGND, and GND should be connected to large copper areas for heat sinking and noise protection. Provide dedicated wide copper traces for the power path ground between the IC and the input and output capacitor grounds, rather than connecting each of these individually to an internal ground plane.
- Avoid using vias in the power path connections that have switched currents (from C_{IN} to PGND and C_{IN} to VIN) and the switching node (SW).



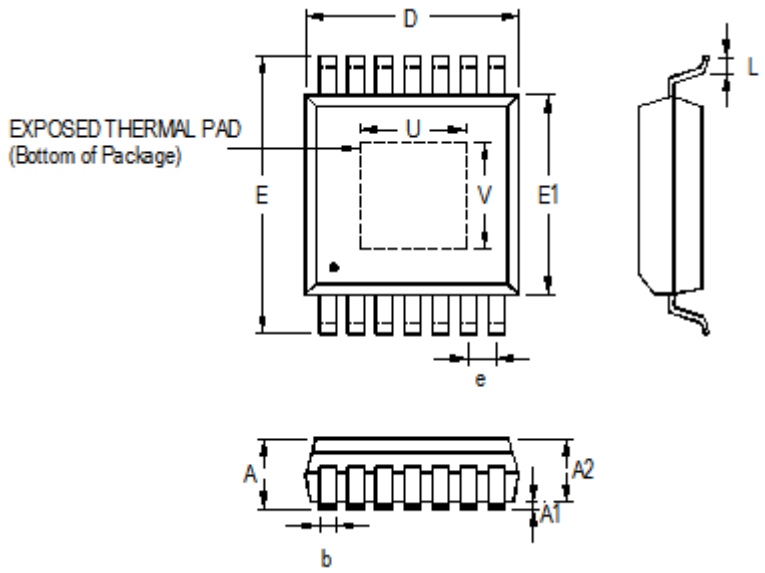
(a). For TSSOP-14 (Exposed Pad) Package



(b). For WDFN-10L 3x3 Package

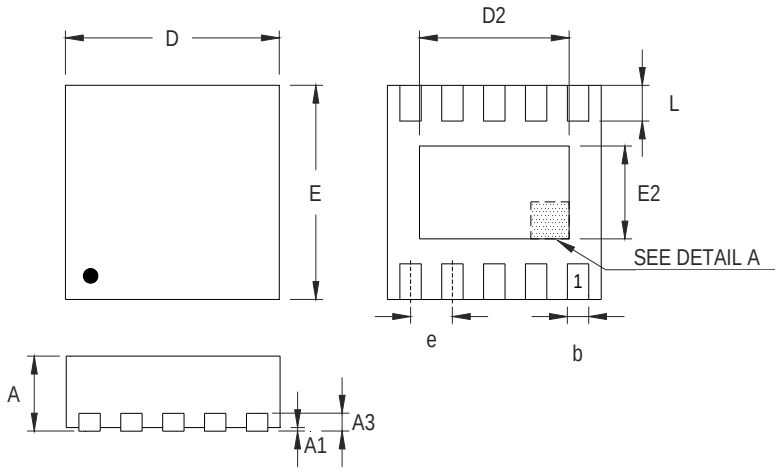
Figure 7. PCB Layout Guide

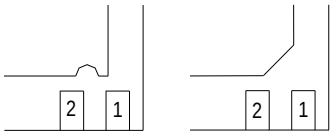
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.200	0.039	0.047
A1	0.000	0.150	0.000	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
D	4.900	5.100	0.193	0.201
e	0.650		0.026	
E	6.300	6.500	0.248	0.256
E1	4.300	4.500	0.169	0.177
L	0.450	0.750	0.018	0.030
U	1.900	2.900	0.075	0.114
V	1.600	2.600	0.063	0.102

14-Lead TSSOP (Exposed Pad) Plastic Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

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