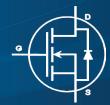
eGaN® FET DATASHEET EPC2033

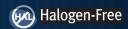
EPC2033 – Enhancement Mode Power Transistor

 V_{DSS} , 150 V $R_{DS(on)}$, 7 $m\Omega$ I_{D} , 48 A









Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 60 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings						
V _{DS}	Drain-to-Source Voltage (Continuous)	150	V			
I _D	Continuous ($T_A = 25^{\circ}C$, $R_{\theta JA} = 4^{\circ}C/W$)	48	۸			
	Pulsed (25°C, T _{PULSE} = 300 μs)	260	A			
V_{GS}	Gate-to-Source Voltage	6	V			
	Gate-to-Source Voltage	-4	V			
Tı	Operating Temperature	-40 to 150	°C			
T _{STG}	Storage Temperature	-40 to 150	C			



EPC2033 eGaN® FETs are supplied only in passivated die form with solder bumps. Die Size: 4.6 mm x 2.6 mm

- High Frequency DC-DC Conversion
- Motor Drive
- Industrial Automation
- · Class-D Audio

www.epc-co.com/epc/Products/eGaNFETs/EPC2033.aspx

	Static Characteristics (T _J = 25°C unless otherwise stated)							
	PARAMETER	TEST CONDITIONS MIN		ТҮР	MAX	UNIT		
BV _{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V, } I_D = 0.7 \text{ mA}$	150			V		
I _{DSS}	Drain Source Leakage	$V_{DS} = 120 \text{ V}, V_{GS} = 0 \text{ V}$		0.1	0.5	mA		
	Gate-to-Source Forward Leakage	$V_{GS} = 5 V$		1	8	mA		
I _{GSS}	Gate-to-Source Reverse Leakage	$V_{GS} = -4 V$		0.1	0.5	mA		
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 9 \text{ mA}$	0.8	1.4	2.5	V		
R _{DS(on)}	Drain-to-Source On Resistance	$V_{GS} = 5 \text{ V}, I_D = 25 \text{ A}$		5	7	mΩ		
V_{SD}	Source-to-Drain Forward Voltage	$I_S = 0.5 \text{ A}, V_{GS} = 0 \text{ V}$		1.9		V		

All measurements were done with substrate shorted to source.

Thermal Characteristics					
		ТҮР	UNIT		
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.45	°C/W		
$R_{ heta JB}$	Thermal Resistance, Junction to Board	3.9	°C/W		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	45	°C/W		

Note 1: R_{ijk} is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

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	Dynamic Characteristics (T _j = 25°C unless otherwise stated)							
	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT		
C _{ISS}	Input Capacitance			1160	1400			
C _{RSS}	Reverse Transfer Capacitance	$V_{DS} = 120 V, V_{GS} = 0 V$		6				
C _{oss}	Output Capacitance			480	720	pF		
C _{OSS(ER)}	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0$ to 120 V, $V_{CS} = 0$ V		670		ρr		
C _{OSS(TR)}	Effective Output Capacitance, Time Related (Note 3)	V _{DS} = 0 to 120 v, v _{GS} = 0 v		900				
R_{G}	Gate Resistance			0.5		Ω		
Q_{G}	Total Gate Charge	$V_{DS} = 120 \text{ V}, V_{GS} = 5 \text{ V}, I_{D} = 25 \text{ A}$		12	15			
Q _{GS}	Gate-to-Source Charge			3.8				
Q_{GD}	Gate-to-Drain Charge	$V_{DS} = 120 V, I_{D} = 25 A$		3.2		nC		
Q _{G(TH)}	Gate Charge at Threshold			2.8		IIC		
Qoss	Output Charge	$V_{DS} = 120 V, V_{GS} = 0 V$		90	135			
Q_{RR}	Source-to-Drain Recovery Charge			0				

Note 2: $C_{OSS(R)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS}. Note 3: $C_{OSS(R)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

Figure 2: Transfer Characteristics

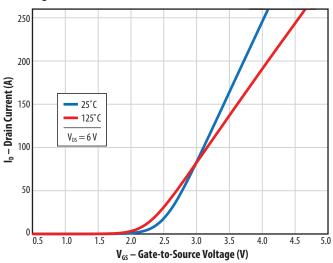


Figure 3: R_{DS(on)} vs. V_{GS} for Various Drain Currents

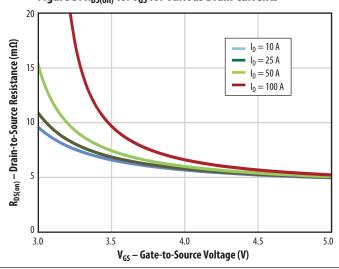
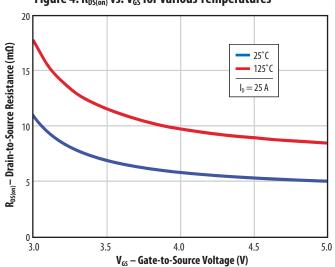


Figure 4: R_{DS(on)} vs. V_{GS} for Various Temperatures



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Figure 5a: Capacitance (Linear Scale)

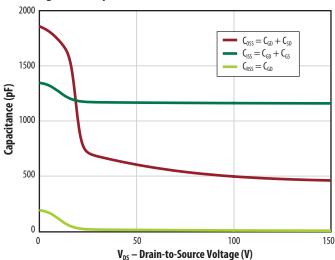


Figure 5b: Capacitance (Log Scale)

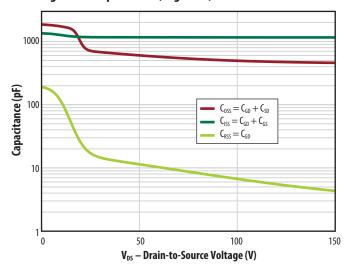


Figure 6: Gate Charge

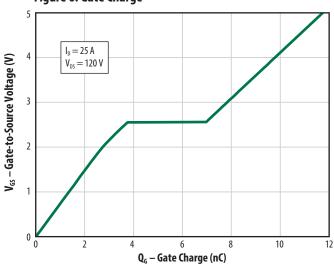


Figure 7: Reverse Drain-Source Characteristics

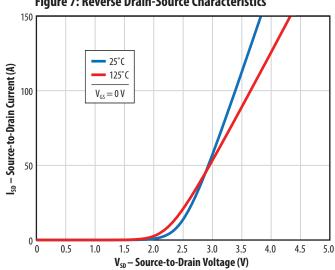


Figure 8: Normalized On-State Resistance vs. Temperature

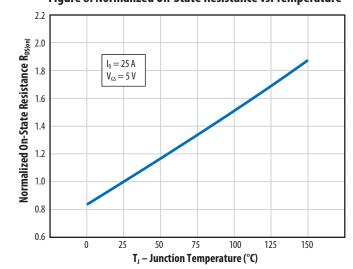
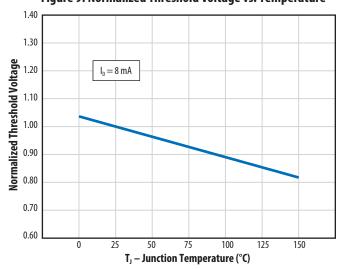


Figure 9: Normalized Threshold Voltage vs. Temperature



All measurements were done with substrate shortened to source. TJ= 25°C unless otherwise stated.

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Figure 10: Gate Leakage Current

40

25°C

125°C

125°C

10

10

10

10

V_{cs} – Gate-to-Source Voltage (V)

Figure 11: Safe Operating Area

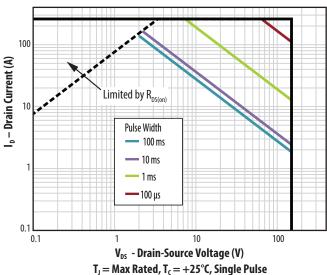
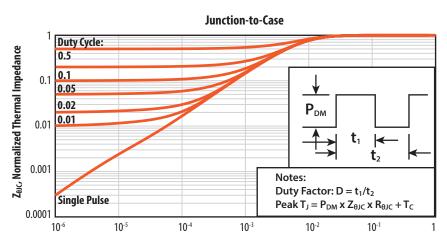
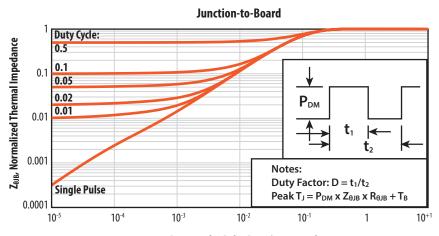


Figure 12: Transient Thermal Response Curves



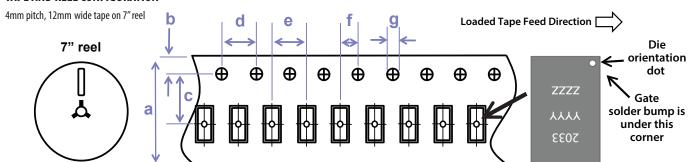
t_p, Rectangular Pulse Duration, seconds



t_p, Rectangular Pulse Duration, seconds

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TAPE AND REEL CONFIGURATION



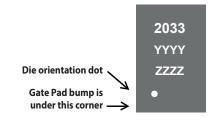
	EPC2033 (note 1)			
Dimension (mm)	target	min	max	
а	12.00	11.70	12.30	
b	1.75	1.65	1.85	
c (see note)	5.50	5.45	5.55	
d	4.00	3.90	4.10	
е	4.00	3.90	4.10	
f (see note)	2.00	1.95	2.05	
g	1.50	1.50	1.60	

Die is placed into pocket solder bump side down (face side down)

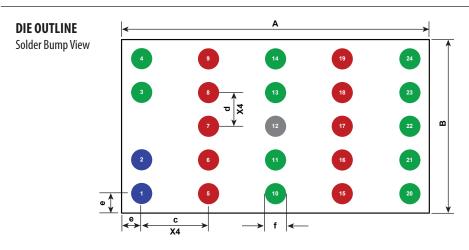
Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard. Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE MARKINGS

Side View



Part		Laser Marking	
Number	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2033	2033	YYYY	ZZZZ



	Micrometers				
DIM	MIN	Nominal	MAX		
Α	4570	4600	4630		
В	2570	2600	2630		
C	1000	1000	1000		
d	500	500	500		
е	285	300	315		
f	332	369	406		

Pads 1 and 2 are Gate;

Pads 5, 6, 7, 8, 9, 15, 16, 17, 18, 19 are Drain;

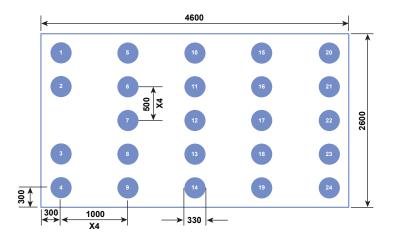
Pads 3, 4, 10, 11, 13, 14, 20, 21, 22, 23, 24 are Source;

Pad 12 is Substrate

		510 typ	790 typ
	SEATING PLANE	280+/-28	<u> </u>

RECOMMENDED LAND PATTERN

(units in μ m)



Land pattern is solder mask defined Solder mask opening is 330 µm It is recommended to have on-Cu trace PCB vias

Pads 1 and 2 are Gate;

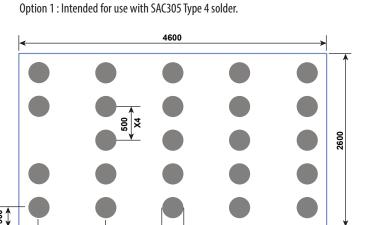
Pads 5, 6, 7, 8, 9, 15, 16, 17, 18, 19 are Drain;

Pads 3, 4, 10, 11, 13, 14, 20, 21, 22, 23, 24 are Source;

Pad 12 is Substrate

RECOMMENDED STENCIL DRAWING

(units in μ m)

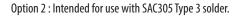


Recommended stencil should be 4mil (100 μ m) thick, must be laser cut, openings per drawing.

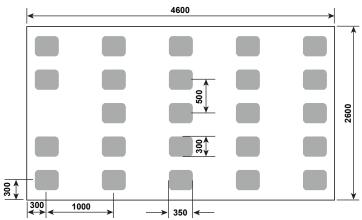
Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

RECOMMENDED STENCIL DRAWING

(units in µm)



1000



Recommended stencil should be 4mil (100 μ m) thick, must be laser cut, openings per drawing.

Additional assembly resources available at http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

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U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398; 8,785,974; 8,890,168; 8,969,918; 8,853,749; 8,823,012

Information subject to change without notice.
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