



# STD2NK70Z STD2NK70Z-1

N-channel 700V - 6Ω - 1.6 A - DPAK/IPAK  
Zener protected SuperMESH™ Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STD2NK70Z	700V	7Ω	1.6A	45W
STD2NK70Z-1	700V	7Ω	1.6A	45W

- Extremely high dv/dt capability
- ESD improved capability
- 100% avalanche tested
- New high voltage benchmark
- Gate charge minimized

## Description

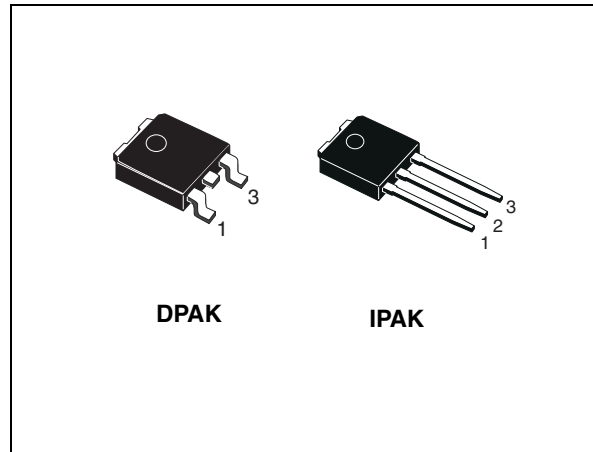
The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding application. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

## Applications

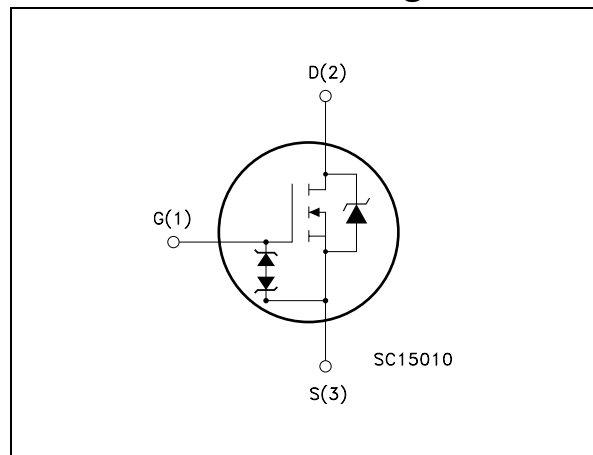
- Switching application

## Order codes

Part number	Marking	Package	Packaging
STD2NK70Z	D2NK70Z	D <sup>2</sup> PAK	Tape & reel
STD2NK70Z-1	D2NK70Z	IPAK	Tube



## Internal schematic diagram



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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	700	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20\text{ k}\Omega$ )	700	V
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	1.6	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	1	A
$I_{DM}^{(1)}$	Drain current (pulsed)	6.4	A
$P_{tot}$	Total dissipation at $T_C = 25^\circ\text{C}$	45	W
	Derating factor	0.36	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD (HBM-C = 100pF, R = 1.5 K $\Omega$ )	2000	V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$T_{stg}$	Storage temperature	55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature		

1. Pulse width limited by safe operating area.

2.  $I_{SD} \leq 1.6\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$

**Table 2. Thermal data**

$R_{thj-case}$	Thermal resistance junction-case max	2.78	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	100	$^\circ\text{C}/\text{W}$
$T_J$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ Max)	1.6	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$ , $I_d=I_{ar}$ , $V_{dd}=50\text{V}$ )	110	mJ

**Table 4. Gate-source zener diode**

Symbol	Parameter	Test Condition	Min.	Typ.	Max	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{mA}$ (open drain)	30			A

## 1.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}$ , $V_{GS} = 0$	700			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating} @ 125^{\circ}\text{C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{V}$			$\pm 10$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$ , $I_D = 0.8\text{A}$		6	7	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$ , $I_D = 0.8\text{A}$		1.4		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$ , $V_{GS} = 0$		280 35 6.5		pF pF pF
$C_{oss\ eq}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0\text{V to } 560\text{V}$		17		pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 350\text{V}$ , $I_D = 0.8\text{A}$ , $R_G = 4.7\Omega$ , $V_{GS} = 10\text{V}$ (see Figure 14)		7 17 20 35		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 560\text{V}$ , $I_D = 0.8\text{A}$ $V_{GS} = 10\text{V}$ (see Figure 15)		11.4 2 6.8		nC nC nC

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

2.  $C_{oss\ eq}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				1.6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				6.4	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=1.6A$ , $V_{GS}=0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=1.6A$ , $di/dt = 100A/\mu s$ , $V_{DD}=50V$ , $T_J=25^{\circ}C$ (see Figure 16)		334 918 5.5		ns $\mu C$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=1.6A$ , $di/dt = 100A/\mu s$ , $V_{DD}= 50V$ , $T_J=150^{\circ}C$ (see Figure 16)		350 1050 6		ns $\mu C$ A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

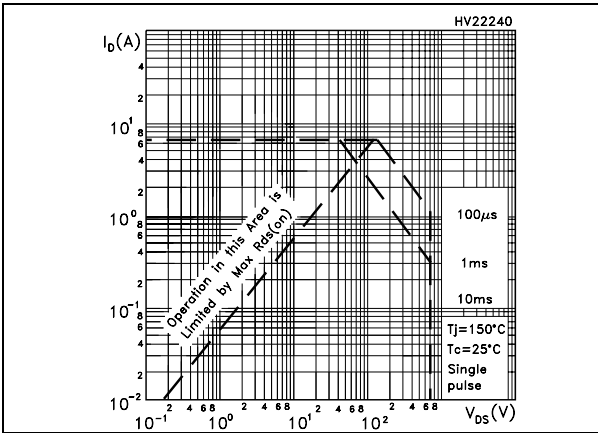


Figure 2. Thermal impedance

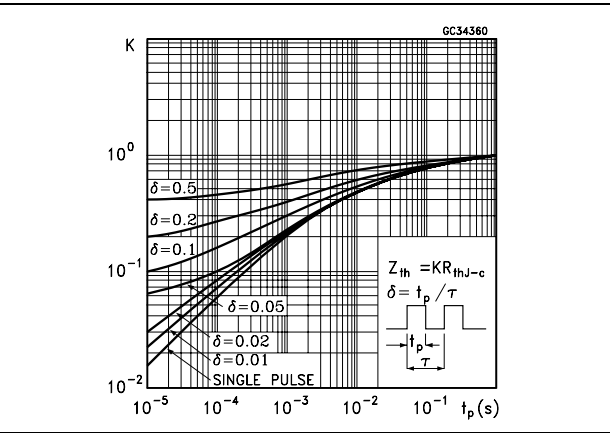


Figure 3. Output characteristics

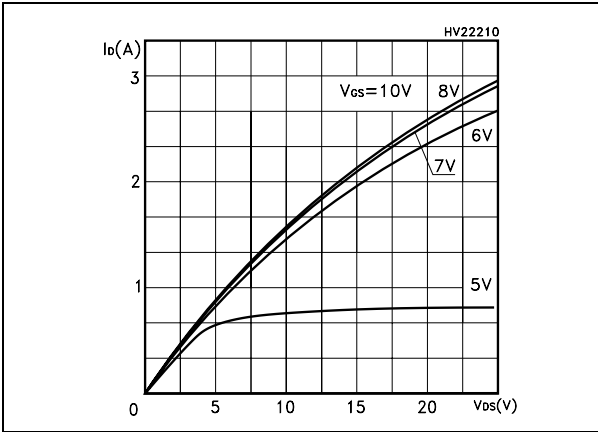


Figure 4. Transfer characteristics

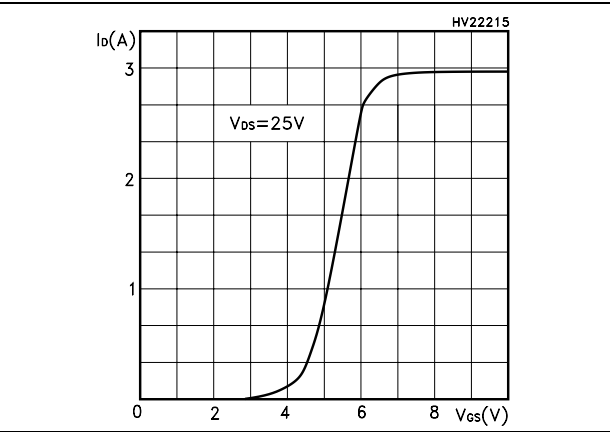


Figure 5. Transconductance

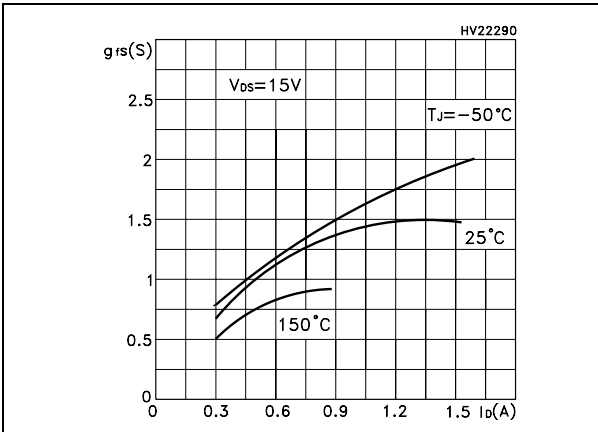


Figure 6. Static drain-source on resistance

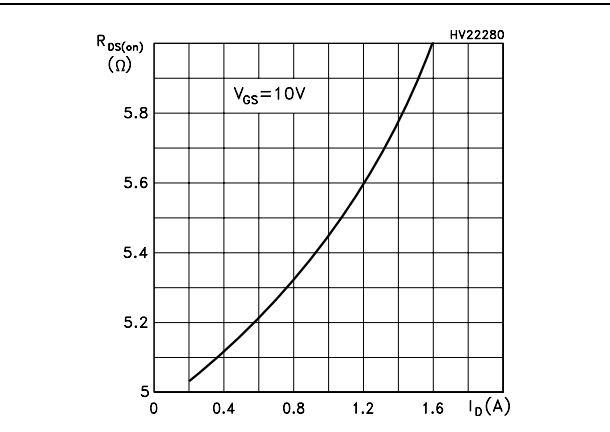


Figure 7. Gate charge vs gate-source voltage    Figure 8. Capacitance variations

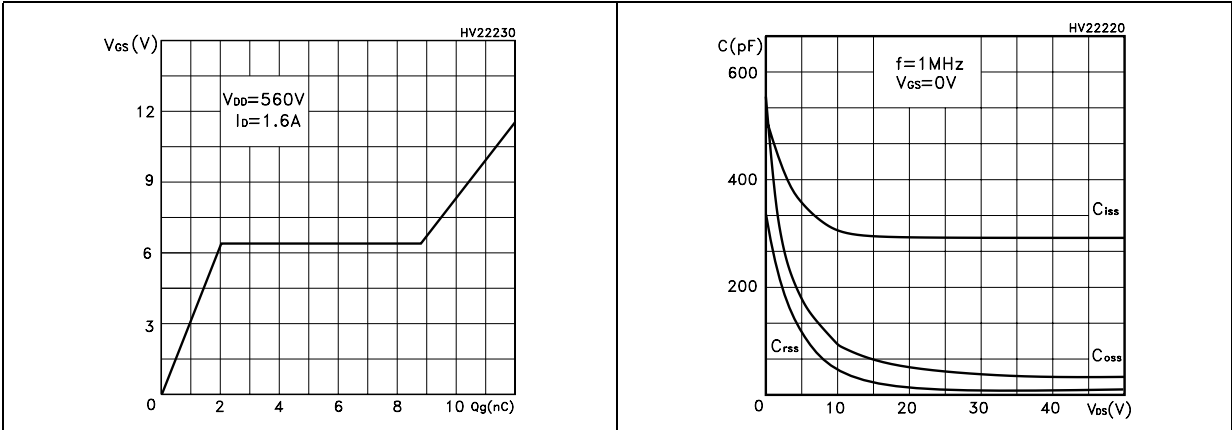


Figure 9. Normalized gate threshold voltage vs temperature    Figure 10. Normalized on resistance vs temperature

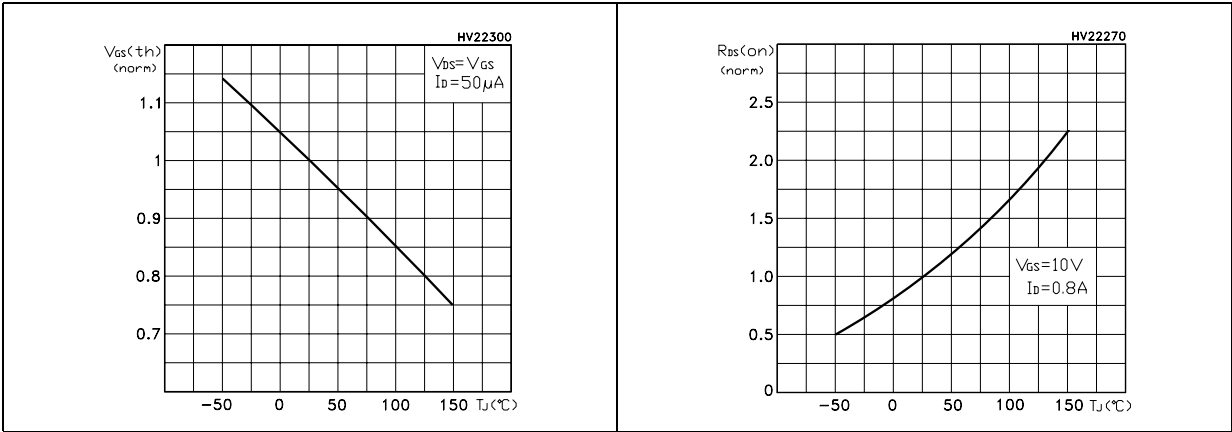


Figure 11. Source-drain diode forward characteristics    Figure 12. Normalized  $B_{V_{DS}}$  vs temperature

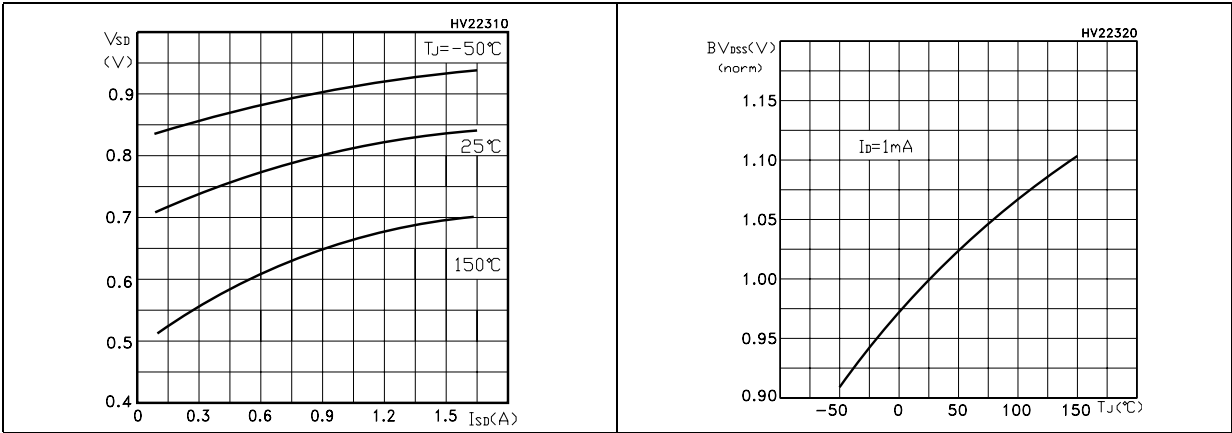
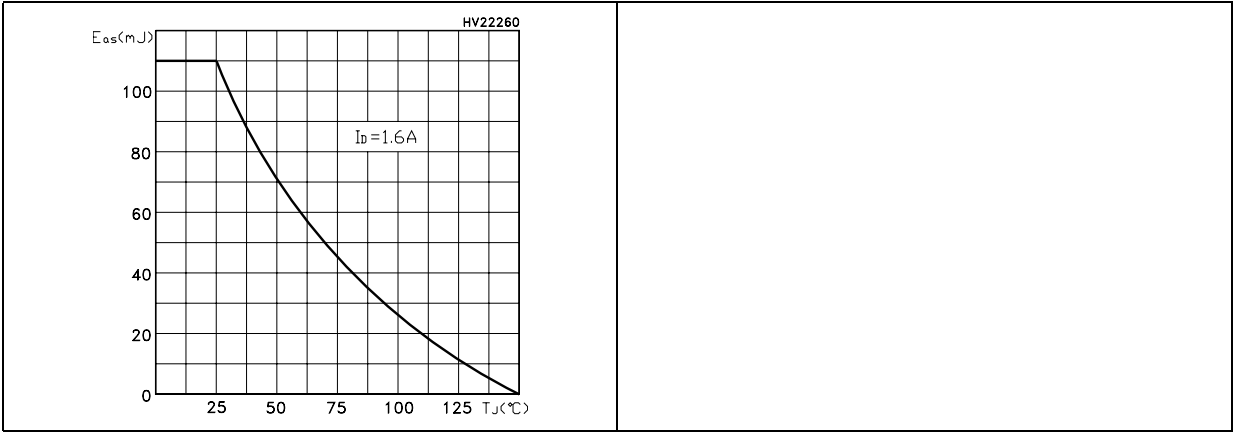




Figure 13. Maximum avalanche energy vs temperature



### 3 Test circuit

Figure 14. Switching times test circuit for resistive load

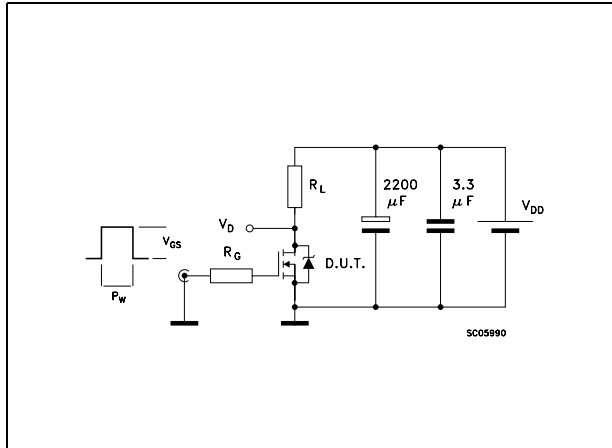


Figure 15. Gate charge test circuit

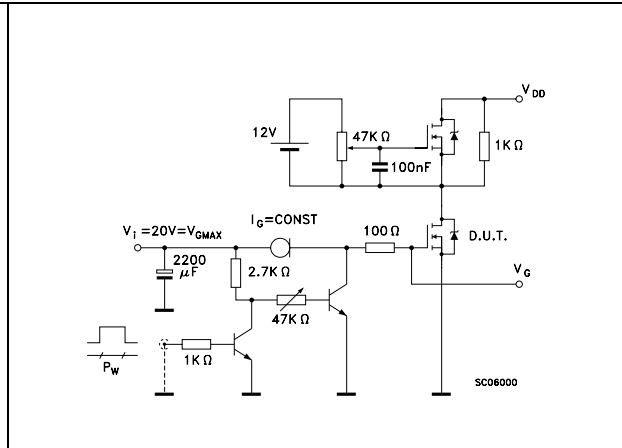


Figure 16. Test circuit for inductive load switching and diode recovery times

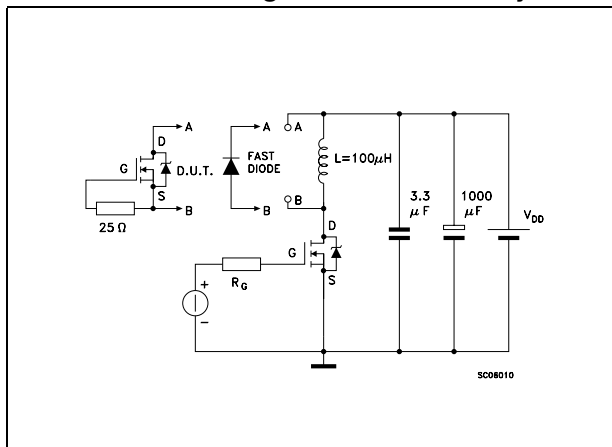


Figure 17. Unclamped Inductive load test circuit

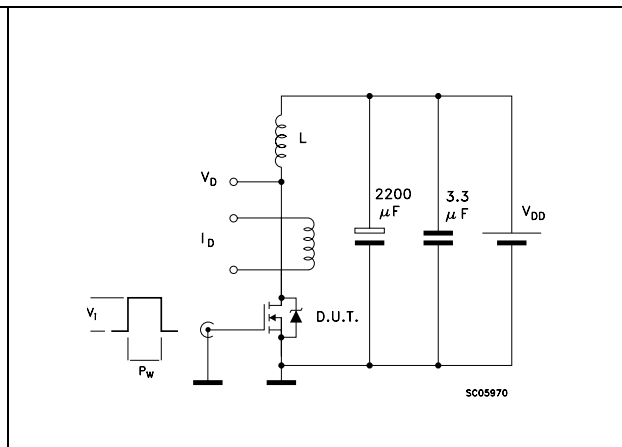


Figure 18. Unclamped inductive waveform

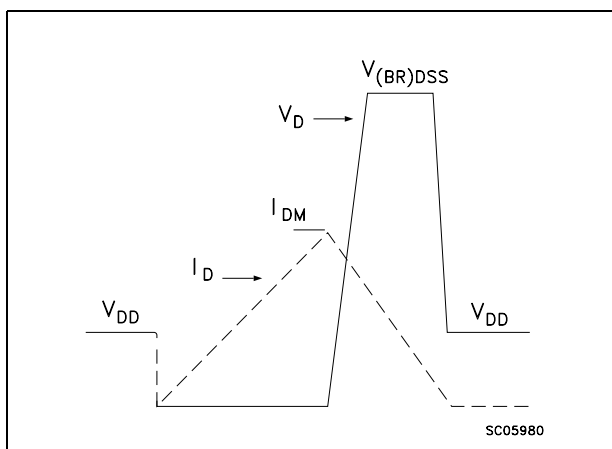
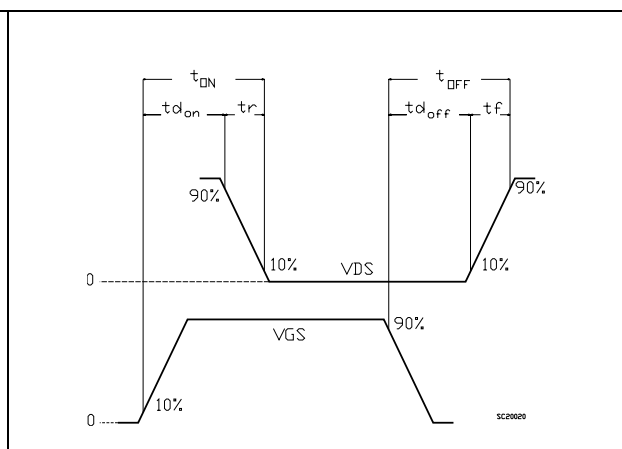


Figure 19. Switching time waveform

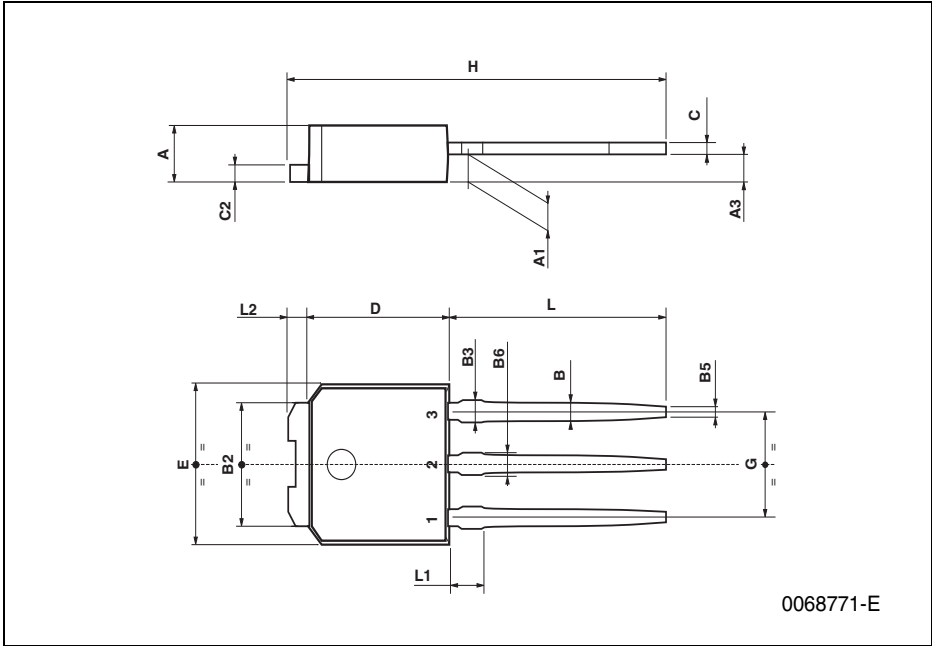


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

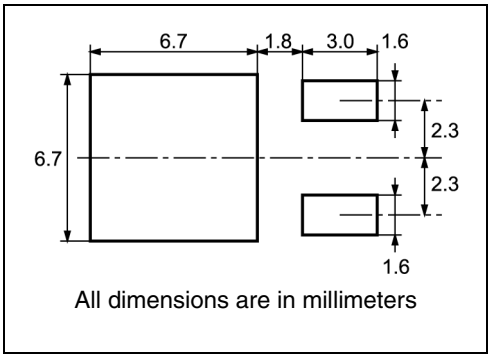
  

The mechanical drawing illustrates the DPAK package geometry. It includes a top view showing dimensions E, b4, and L2. A side view shows dimensions A, c2, D, and A1. A detail view of the thermal pad shows dimensions E1, D1, and a central pad. A cross-sectional view shows the seating plane, gauge plane, and dimensions A2, L, and V2. A note indicates a 0.25 mm dimension for the gauge plane.

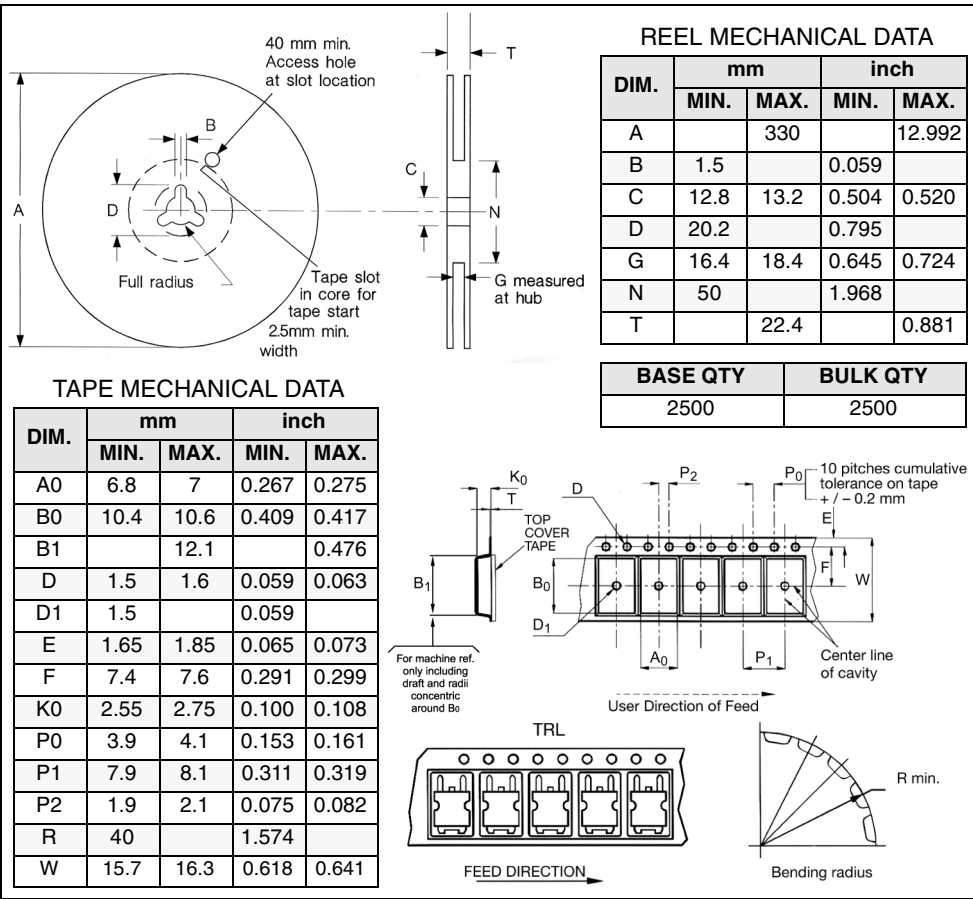
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# 5 Packaging mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT



## 6 Revision history

**Table 8. Revision history**

Date	Revision	Changes
21-Jan-2005	1	First Release
10-Jun-2005	2	Updated <i>Figure 1: Safe operating area</i>
13-Jul-2006	3	New template, no content change

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