National Semiconductor

54LS295A/DM74LS295A
4-Bit Shift Register with TRI-STATE® Outputs

General Description

The 'LS295A is a 4-bit shift register with serial and parallel synchronous operating modes, and independent TRI-STATE output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfers and shifting occur synchronous with the HIGH-to-LOW clock transition.

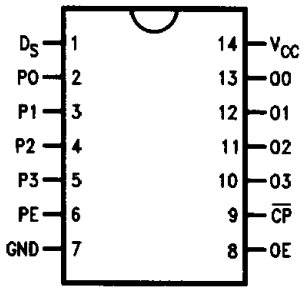
The TRI-STATE output buffers are controlled by an active HIGH Output Enable input (OE). Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion. The device is fabricated with the Schottky barrier diode process for high speed.

Features

- Fully synchronous serial or parallel data transfers
- Negative edge-triggered clock input
- Parallel enable mode control input
- TRI-STATE bussable output buffers

Connection Diagram

Dual-In-Line Package



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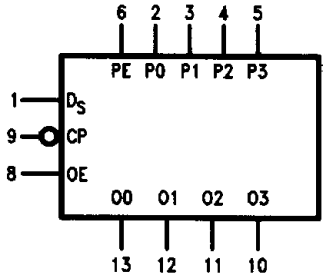
Order Number 54LS295ADMQB, 54LS295AFMQB, DM74LS295AM or DM74LS295AN
See NS Package Number J14A, M14A, N14A or W14B

Logic Symbol



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V_{CC} = Pin 14
GND = Pin 7

Pin Names	Description
PE	Parallel Enable Input (Active HIGH)
D_S	Serial Data Input
P0–P3	Parallel Data Inputs
OE	TRI-STATE Output Enable Input (Active HIGH)
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)
O0–O3	TRI-STATE Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS295A			DM74LS295A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Current			−1.0			−2.6	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_S, P_n to $\overline{CP}$	20 20			20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_S, P_n to $\overline{CP}$	10 10			10 10			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW PE to $\overline{CP}$	20 20			20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW PE to $\overline{CP}$	0 0			0 0			ns
t_w (L)	$\overline{CP}$ Pulse Width LOW	20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.4			V
			DM74	2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current Outputs ON	V_{CC} = Max, P_n = GND PE, DS, OE = 4.5V, $\overline{CP}$ = ⌝⌞				23	mA
	Outputs OFF	V_{CC} = Max, PE, DS = 4.5V P_n, OE, $\overline{CP}$ = GND				25	mA

Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max			20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−20	μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 3 for waveforms and load configurations)

Symbol	Parameter	54/74LS		Units
		R_L = 2 kΩ, C_L = 15 pF		
		Min	Max	
f_{max}	Maximum Shift Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n		30 26	ns
t_{PZH} t_{PZL}	Output Enable Time		18 20	ns
t_{PHZ} t_{PLZ}	Output Disable Time		24 20	ns

Functional Description

This device is a 4-bit shift register with serial and parallel synchronous operating modes. It has a Serial Data (D_S) and four Parallel Data (P0–P3) inputs and four parallel TRI-STATE output buffers (O0–O3). When the Parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data inputs (P0–P3) into the register synchronous with the HIGH-to-LOW transition of the Clock ($\overline{CP}$). When the PE is LOW, a HIGH-to-LOW transition on the clock transfers the serial data on the D_S input to the register Q0, and shifts data from Q0 to Q1, Q1 to Q2 and Q2 to Q3. The input data and parallel enable are fully edge-triggered and must be stable only one setup time before the HIGH-to-LOW clock transition.

The TRI-STATE output buffers are controlled by an active HIGH Output Enable input (OE). When the OE is HIGH, the four register outputs appear at the O0–O3 outputs. When OE is LOW, the outputs are forced to a high impedance OFF state. The TRI-STATE output buffers are completely independent of the register operation, i.e., the input transitions on the OE input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Mode Select Table

Operating Mode	Inputs				Outputs			
	PE	$\overline{CP}$	D_S	P_n	Q0	Q1	Q2	Q3
Shift Right	l	⌁	l	X	L	q_0	q_1	q_2
	l	⌁	h	X	H	q_0	q_1	q_2
Parallel Load	h	⌁	X	p_n	p0	p1	p2	p3

*The indicated data appears at the Q outputs when OE is HIGH. When OE is LOW, the indicated data is loaded into the register, but the outputs are all forced to the high impedance OFF state.

p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

l = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.

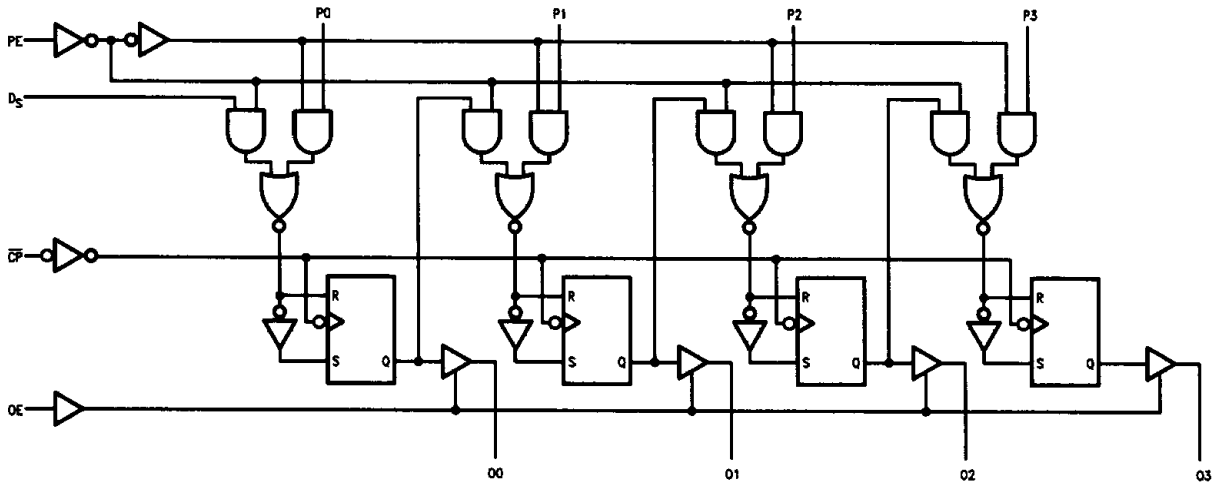
h = HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



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