

SN54ABT651, SN74ABT651 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS083E – JANUARY 1991 – REVISED APRIL 1998

- State-of-the-Art *EPIC-II*[™] BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Plastic (NT) and Ceramic (JT) DIPs

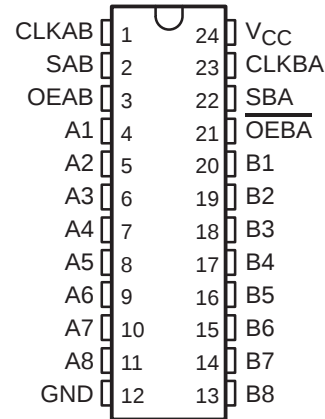
description

These devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output-enable (OEAB and $\overline{\text{OEBA}}$) inputs are provided to control the transceiver functions. The select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT651 devices.

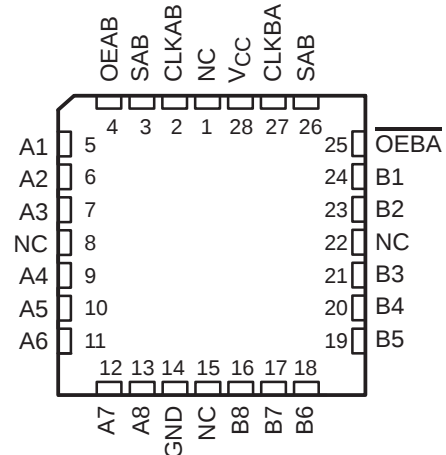
Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it also is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all the other data sources to the two sets of bus lines are at high impedance, each set remains at its last state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver (B to A). OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver (A to B).

SN54ABT651 . . . JT PACKAGE
SN74ABT651 . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



SN54ABT651 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC-II[®] is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1998, Texas Instruments Incorporated

SN54ABT651, SN74ABT651

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS083E – JANUARY 1991 – REVISED APRIL 1998

description (continued)

The SN54ABT651 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT651 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE

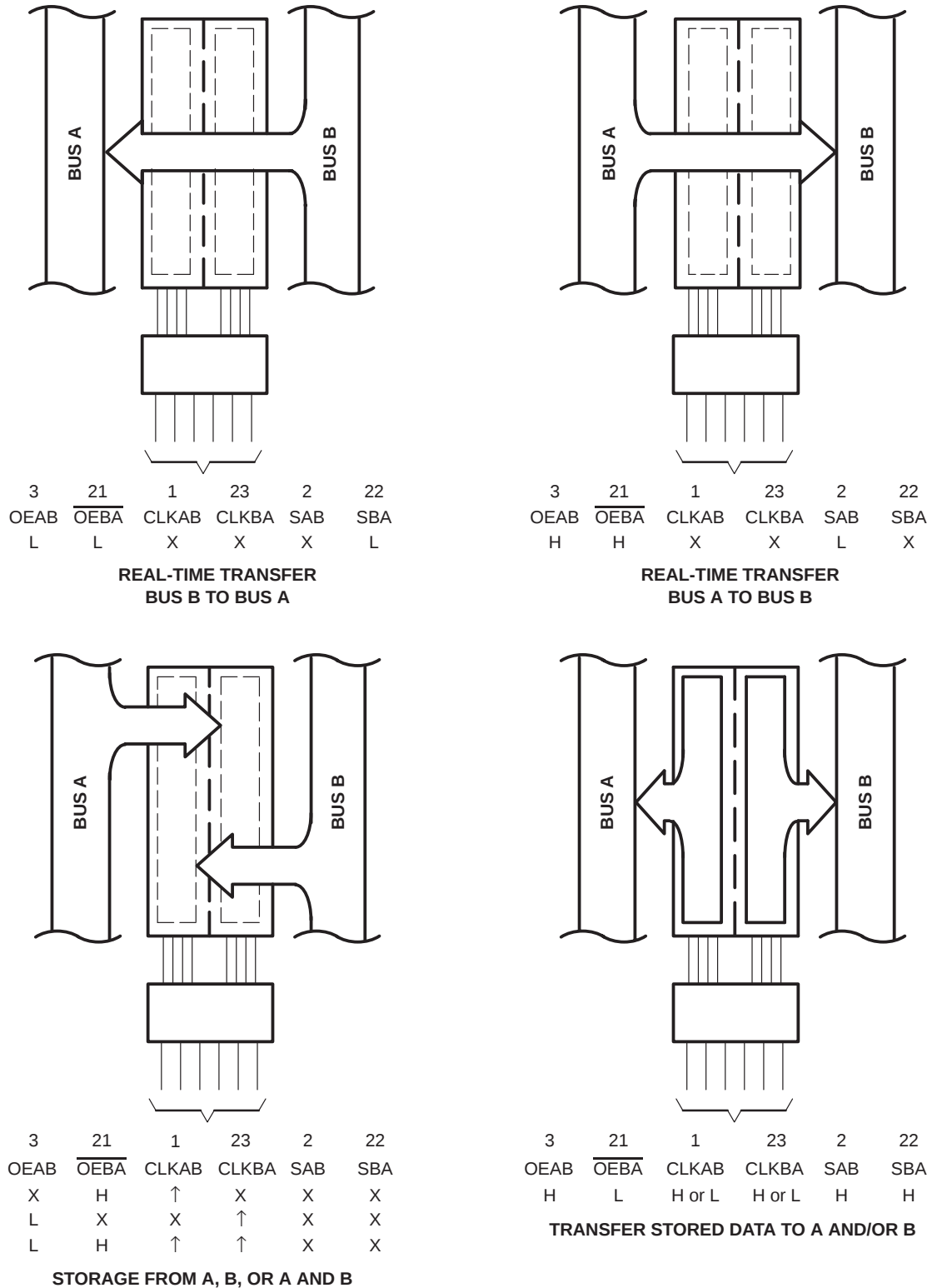
INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	$\uparrow$	$\uparrow$	X	X	Input	Input	Store A and B data
X	H	$\uparrow$	H or L	X	X	Input	Unspecified [†]	Store A, hold B
H	H	$\uparrow$	$\uparrow$	X [‡]	X	Input	Output	Store A in both registers
L	X	H or L	$\uparrow$	X	X	Unspecified [†]	Input	Hold A, store B
L	L	$\uparrow$	$\uparrow$	X	X [‡]	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time $\overline{\text{B}}$ data to A bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{\text{B}}$ data to A bus
H	H	X	X	L	X	Input	Output	Real-time $\overline{\text{A}}$ data to B bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{\text{A}}$ data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{\text{A}}$ data to B bus and stored $\overline{\text{B}}$ data to A bus

[†] The data output functions may be enabled or disabled by a variety of level combinations at OEAB or $\overline{\text{OEBA}}$. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

[‡] When select control is low, clocks can occur simultaneously if allowances are made for propagation delays from A to B (B to A) plus setup and hold times. When select control is high, clocks must be staggered to load both registers.

SN54ABT651, SN74ABT651 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS083E – JANUARY 1991 – REVISED APRIL 1998



Pin numbers are for the DB, DW, JT, NT, and PW packages.

Figure 1. Bus-Management Functions

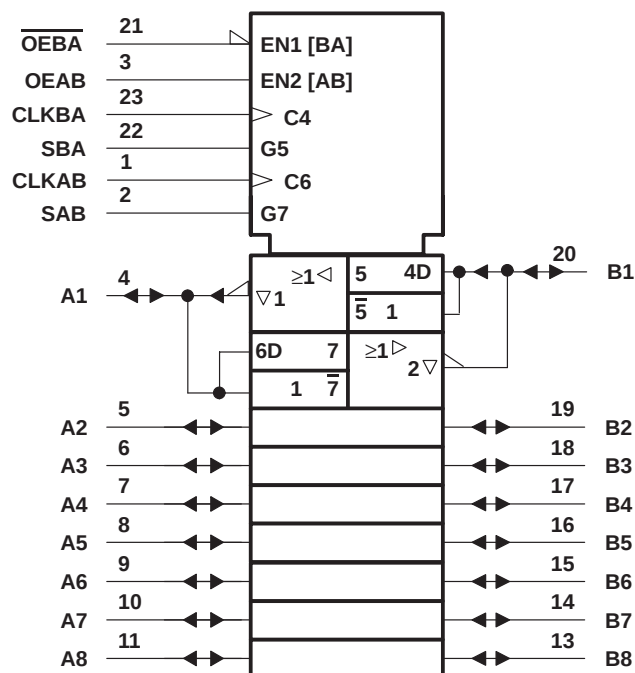
SN54ABT651, SN74ABT651

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS083E – JANUARY 1991 – REVISED APRIL 1998

logic symbol†

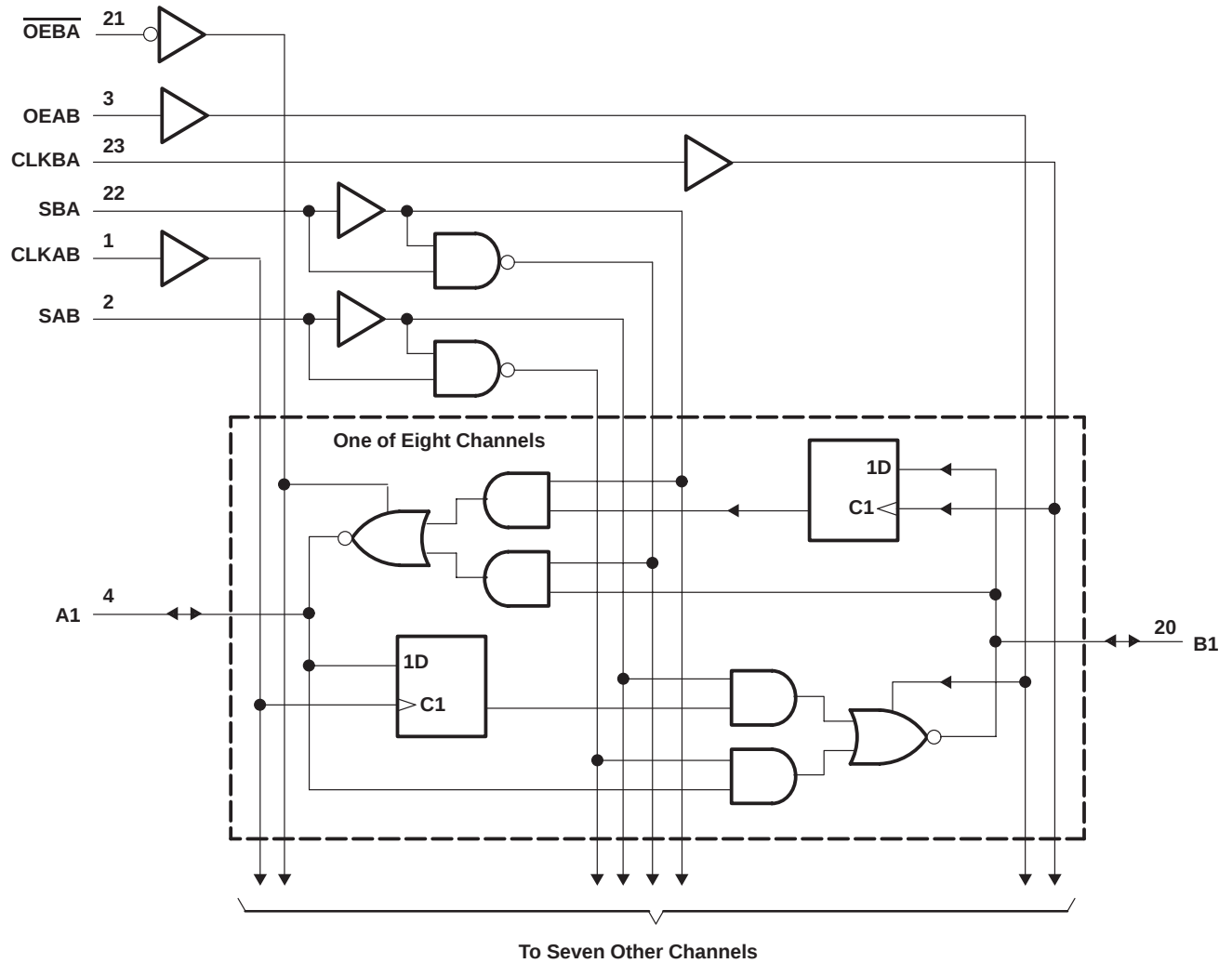


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

SN54ABT651, SN74ABT651 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS083E – JANUARY 1991 – REVISED APRIL 1998

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

SN54ABT651, SN74ABT651

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS083E – JANUARY 1991 – REVISED APRIL 1998

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT651	96 mA
SN74ABT651	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	104°C/W
DW package	81°C/W
NT package	67°C/W
PW package	120°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

	SN54ABT651		SN74ABT651		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		–24		–32	mA
I_{OL} Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		5		5	ns/V
T_A Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused pins (control or I/O) of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ABT651, SN74ABT651

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS083E – JANUARY 1991 – REVISED APRIL 1998

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT651		SN74ABT651		UNIT
		MIN	TYP [†]	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = –18 mA			–1.2		–1.2		–1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = –3 mA	2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = –3 mA	3			3		3		
	V _{CC} = 4.5 V			2					
				2*			2		
V _{OL}	V _{CC} = 4.5 V			0.55		0.55			V
				0.55*			0.55		
V _{hys}			100						mV
I _I	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND		±1		±1		±1	μA
	A or B ports			±100		±100		±100	
I _{OZH} [‡]	V _{CC} = 5.5 V, V _O = 2.7 V			50		50		50	μA
I _{OZL} [‡]	V _{CC} = 5.5 V, V _O = 0.5 V			–50		–50		–50	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V			50		50		50	μA
I _O [§]	V _{CC} = 5.5 V, V _O = 2.5 V	–50	–100	–180	–50	–180	–50	–180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND			250		250		250	μA
				30		30		30	mA
				250		250		250	μA
ΔI _{CC} [¶]	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V		6					pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V		7.5					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

		V _{CC} = 5 V, T _A = 25°C		SN54ABT651		SN74ABT651		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		125		125		125	MHz
t _w	Pulse duration, CLK high or low	4		4		4		ns
t _{su}	Setup time, A or B before CLKAB [↑] or CLKBA [↑]	3		3		3		ns
t _h	Hold time, A or B after CLKAB [↑] or CLKBA [↑]	0		0		0		ns

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ABT651, SN74ABT651

OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

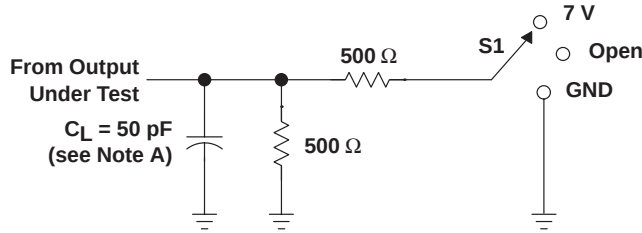
SCBS083E – JANUARY 1991 – REVISED APRIL 1998

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			SN54ABT651		SN74ABT651		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{\max}$			125			125		125		MHz
t_{PLH}	CLKBA or CLKAB	A or B	2.2	4	5.1	2.2	5.9	2.2	5.6	ns
t_{PHL}			1.7	4	5.1	1.7	5.9	1.7	5.6	
t_{PLH}	A or B	B or A	1.5	4	5.1	1.5	6.4	1.5	6.2	ns
t_{PHL}			1.5	3.3	4.6	1.5	5.6	1.5	5.4	
t_{PLH}	SAB or SBA [†]	A or B	1.5	4	5.1	1.5	6.8	1.5	6.5	ns
t_{PHL}			1.5	3.6	4.9	1.5	6.2	1.5	5.9	
t_{PZH}	$\overline{OEBA}$	A	1.3	3.6	4.6	1.3	5.9	1.3	5.8	ns
t_{PZL}			2.5	5.7	6.8	2.5	8.9	2.5	8.5	
t_{PHZ}	$\overline{OEBA}$	A	1.5	3.2	4.5	1.5	6.2	1.5	5	ns
t_{PLZ}			1.5	3	3.8	1.5	4.3	1.5	4.1	
t_{PZH}	OEAB	B	1.8	4.3	6.1	1.8	6.7	1.8	6.5	ns
t_{PZL}			2.9	5.5	6.5	2.9	7.6	2.9	7.4	
t_{PHZ}	OEAB	B	1.5	3.3	4.5	1.5	6.5	1.5	5.5	ns
t_{PLZ}			1.5	3.4	4.4	1.5	5.2	1.5	5.1	

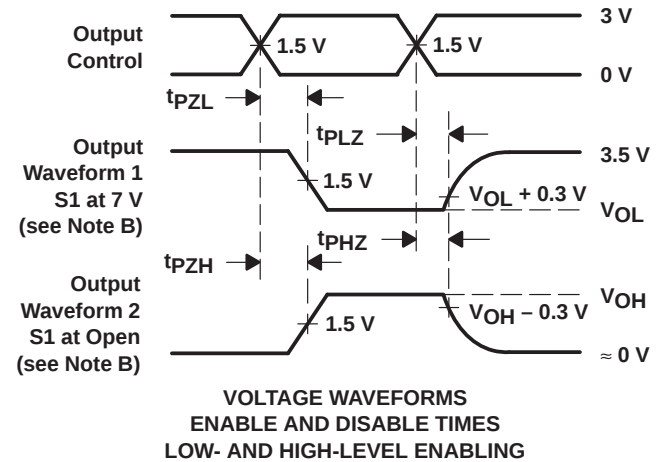
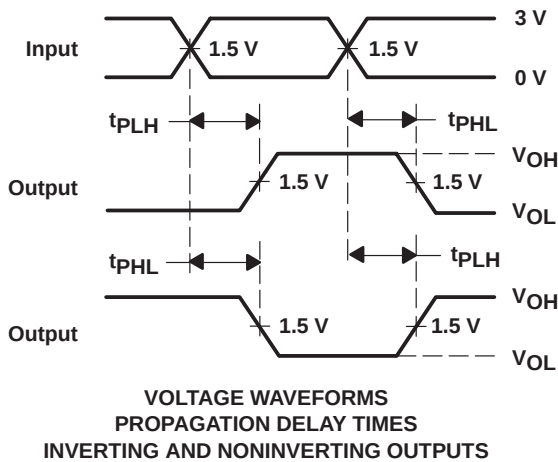
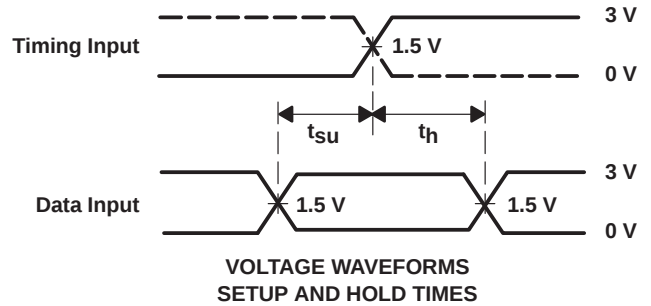
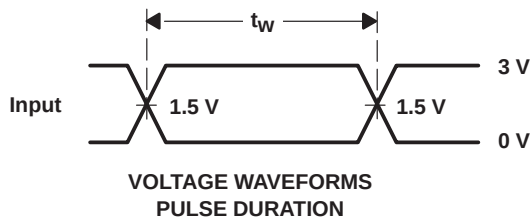
[†] These parameters are measured with the internal output state of the storage register opposite that of the bus input.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ABT651DBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
SN74ABT651DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT651DBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT651DBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT651DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT651DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT651DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT651DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT651DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT651DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT651NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ABT651NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

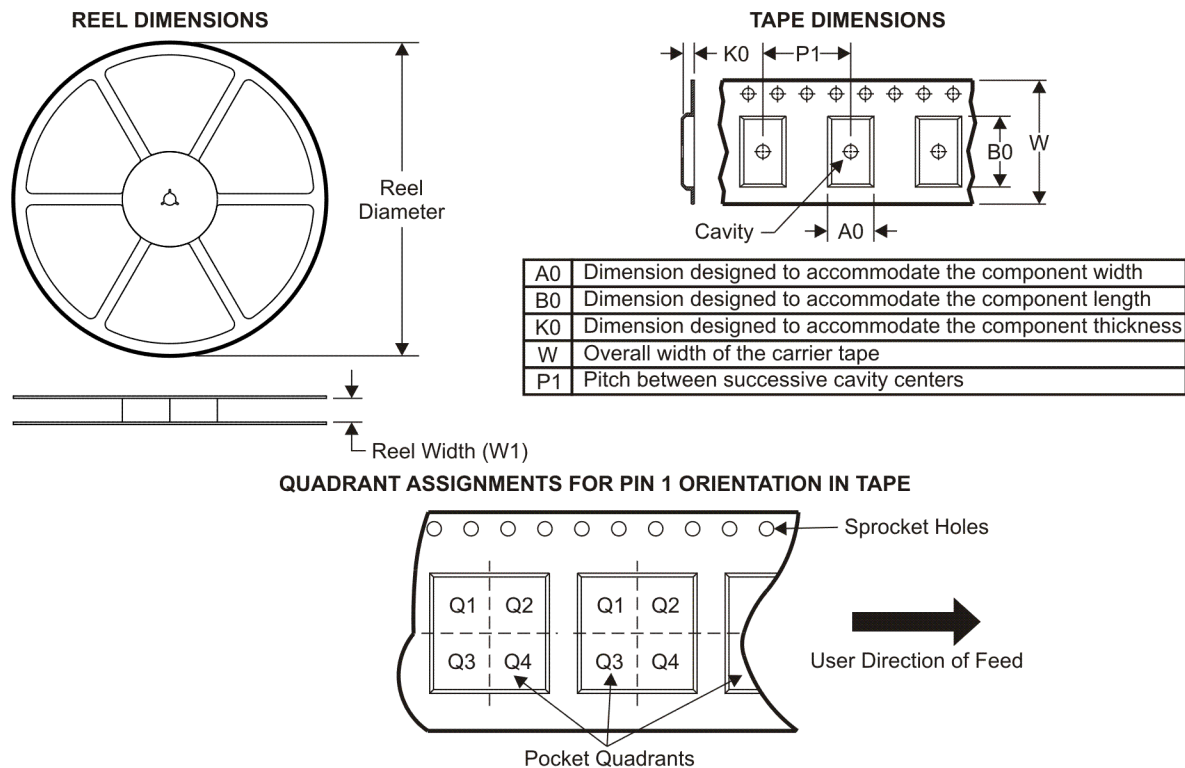
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

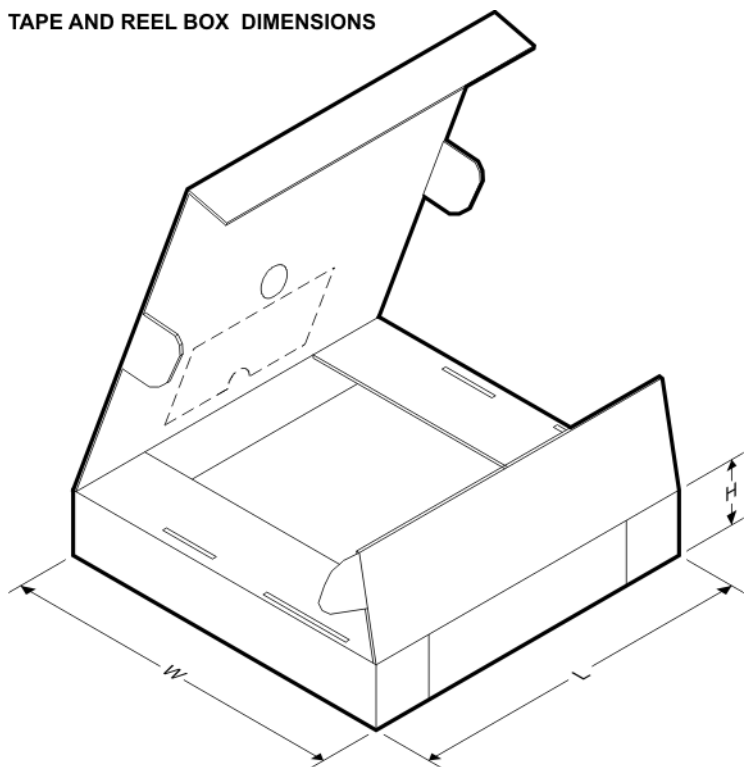
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT651DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74ABT651DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT651DBR	SSOP	DB	24	2000	346.0	346.0	33.0
SN74ABT651DWR	SOIC	DW	24	2000	346.0	346.0	41.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated