

To all our customers

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**Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.**

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The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.)

Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

# PRELIMINARY

Notice: This is not a final specification.  
Some parametric limits are subject to change.

## M65667FP

### PICTURE-IN-PICTURE SIGNAL PROCESSING

#### DESCRIPTION

The M65667FP is a NTSC PIP (Picture in Picture) signal processing LSI, whose sub and main-picture inputs are composite and Y/C separated signals, respectively. The built-in field memory (96k-bit RAM), V-chip data slicer and analog circuitries lead the PIP system low cost and small size.

#### FEATURES

- Built-in 96k-bit field memory (sub-picture data storage)
- Internal V-chip data slicer (for sub-picture)
- Vertical filter for sub-picture (Y signal)
- Single sub-picture (selectable picture size : 1/9 , 1/16)
- Sub-picture processing specification (1/9 size / 1/16 size) :
  - Quantization bits Y, B-Y, R-Y : 6bits
  - Horizontal sampling 171 pixels (Y) , 28.5 pixels (B-Y, R-Y)
  - Vertical lines 69/ 52 lines
- Frame (sub-picture) on/off
- Built-in analog circuits :
  - Two 8-bit A/D converters (main and sub-picture signals)
  - Two 8-bit D/A converters (Y and C sub-picture signals)
  - Sync-tip-clump, VCXO, Analog switch ... etc.
- I<sup>2</sup>C BUS control (parallel/serial control) :
  - PIP on/off , Sub-picture size(1/9 or 1/16), Frame on/off (programmable luma level), PIP position (4 corners fixed position), Picture freeze , Y delay adjustment, Chroma level, Tint, Black level, Contrast ... etc.

#### APPLICATION

NTSC color TV

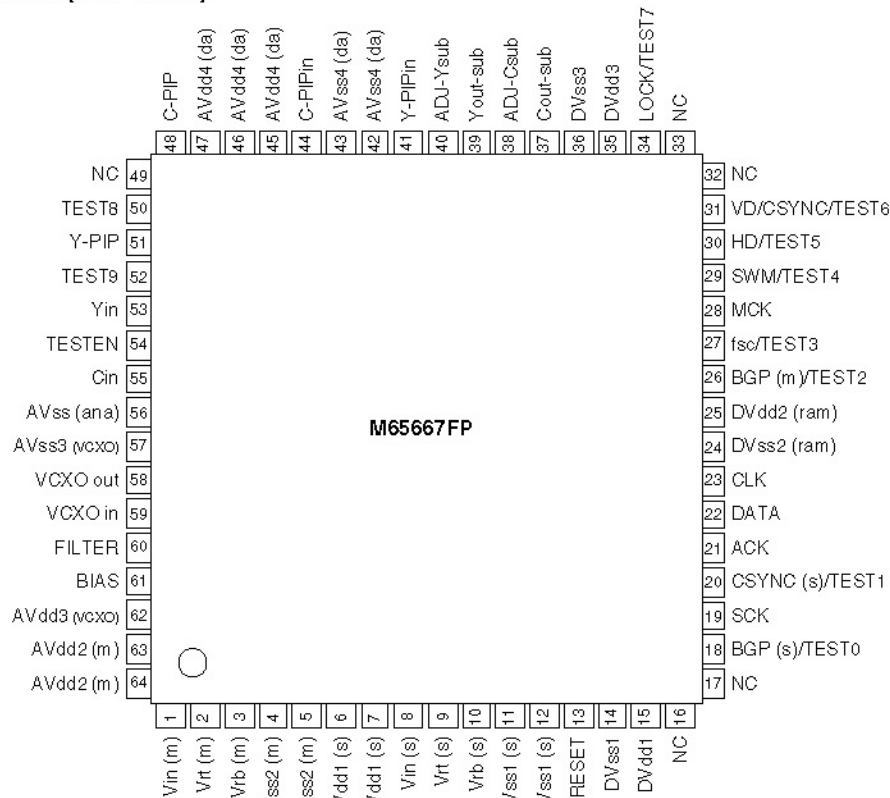
#### RECOMMENDED OPERATING CONDITION

|                                         |                                          |
|-----------------------------------------|------------------------------------------|
| Supply voltage range.....               | 3.1 to 3.5V                              |
| Operating frequency.....                | 14.32 MHz                                |
| Operating temperature.....              | -20 to 75 °C                             |
| Input voltage (CMOS interface) "H"..... | V <sub>DD</sub> 0.7 to V <sub>DD</sub> V |
| "L".....                                | 0 to V <sub>DD</sub> 0.3V                |
| Output current (output buffer).....     | 4mA (MAX)                                |
| Output load capacitance.....            | 20pF (MAX) <sup>1</sup>                  |
| Circuit current.....                    | 160mA                                    |

NOTICE: Connect a 0.1 μF or larger capacitor between V<sub>DD</sub> and V<sub>SS</sub> pins.

<sup>1</sup> : Include pin capacitance (7pF)

#### PIN CONFIGURATION (TOP VIEW)



Outline 64P6N-A

NC : NO CONNECTION

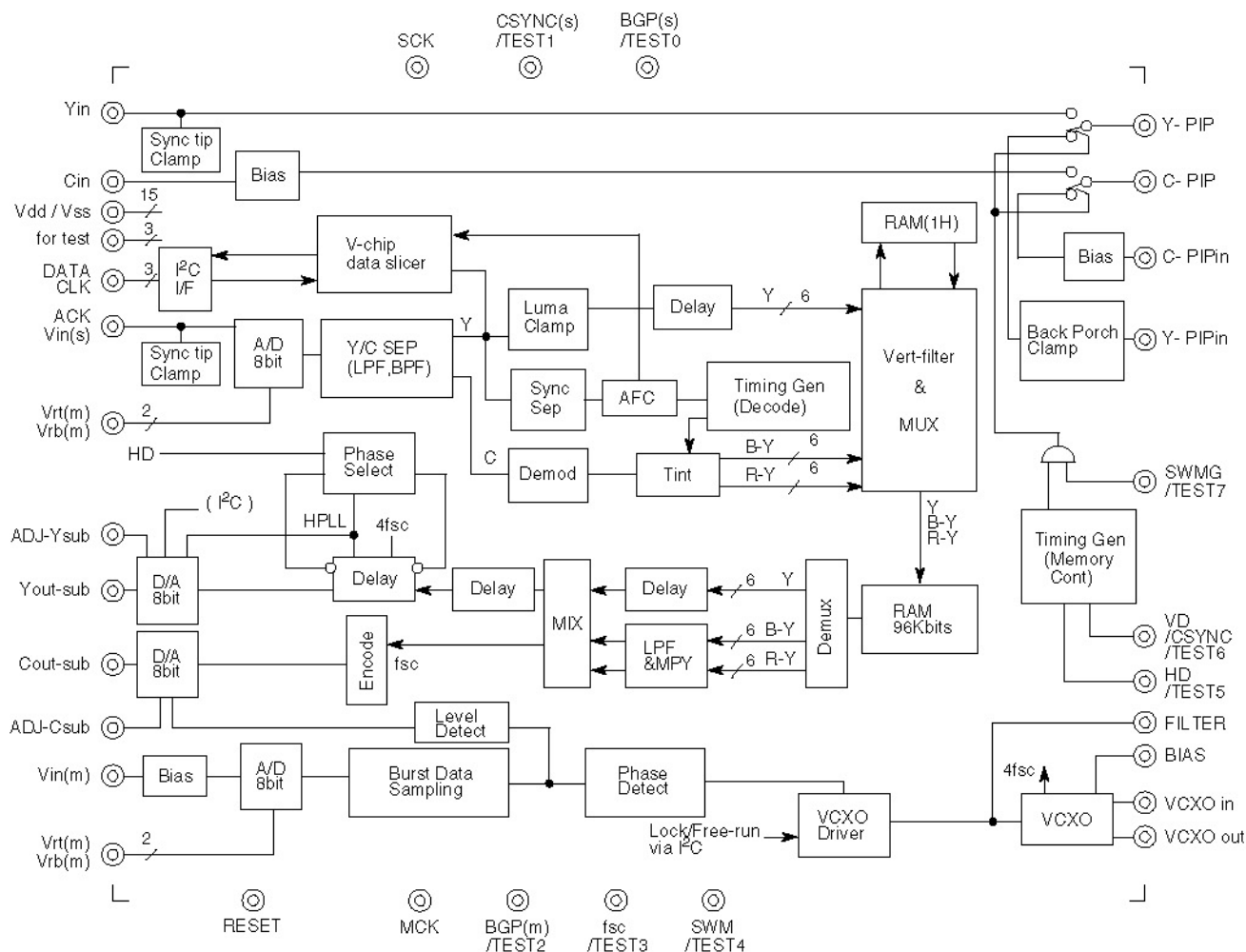
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## M65667FP

## PICTURE-IN-PICTURE SIGNAL PROCESSING

## BLOCK DIAGRAM



# PRELIMINARY

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## M65667FP

### PICTURE-IN-PICTURE SIGNAL PROCESSING

#### DESCRIPTION OF PIN

| Pin No. | Name           | I/O   | Function                                                   | Remarks                  |
|---------|----------------|-------|------------------------------------------------------------|--------------------------|
| 1       | Vin (m)        | I     | Chroma signal input (main-picture)                         |                          |
| 2       | Vrt (m)        | O     | A/D Vref+ (main-picture)                                   |                          |
| 3       | Vrb (m)        | O     | A/D Vref- (main-picture)                                   |                          |
| 4       | AVss2 (m)      | GND   | Connect to analog GND                                      |                          |
| 5       | AVss2 (m)      | GND   | Connect to analog GND                                      |                          |
| 6       | AVdd1 (s)      | Vdd   | Connect to analog power supply                             |                          |
| 7       | AVdd1 (s)      | Vdd   | Connect to analog power supply                             |                          |
| 8       | Vin (s)        | I     | Composite video signal input (sub-picture)                 |                          |
| 9       | Vrt (s)        | O     | A/D Vref+ (sub-picture)                                    |                          |
| 10      | Vrb (s)        | O     | A/D Vref- (sub-picture)                                    |                          |
| 11      | AVss1 (s)      | GND   | Connect to analog GND                                      |                          |
| 12      | AVss1 (s)      | GND   | Connect to analog GND                                      |                          |
| 13      | RESET          | I     | Power on reset input signal ("L" reset)                    | 100k to VDD, 10 F to GND |
| 14      | DVss1          | GND   | Connect to digital GND                                     |                          |
| 15      | DVdd1          | Vdd   | Connect to digital power supply                            |                          |
| 16      | NC             |       |                                                            |                          |
| 17      | NC             |       |                                                            |                          |
| 18      | BGP(s)/TEST0   | (I/O) | For test                                                   | non connect              |
| 19      | SCK            | I     | For test (connect to digital GND)                          | connect to GND           |
| 20      | CSYNC(s)/TEST1 | I(O)  | For test (connect to digital GND)                          | pull down 15k            |
| 21      | ACK            | O     | I <sup>2</sup> C bus-data/Acknowledge output signal        |                          |
| 22      | DATA           | I     | I <sup>2</sup> C bus-data input signal                     |                          |
| 23      | CLK            | I     | I <sup>2</sup> C bus-clock input signal                    |                          |
| 24      | DVss2(ram)     | GND   | Connect to digital GND                                     |                          |
| 25      | DVdd2(ram)     | Vdd   | Connect to digital power supply                            |                          |
| 26      | BGP(m)/TEST2   | (I/O) | For test                                                   | non connect              |
| 27      | fsc/TEST3      | I(O)  | For test (pull down to digital GND by resistor 15k )       | pull down 15k            |
| 28      | MCK            | I     | For test (connect to digital GND)                          | connect to GND           |
| 29      | SWM/TEST4      | (I/O) | For test                                                   | non connect              |
| 30      | HD/TEST5       | I(O)  | Horizontal sync input signal (Positive going edge is used) |                          |
| 31      | VD/CSYNC/TEST6 | I(O)  | Vertical sync input signal (active "H")                    |                          |
| 32      | NC             |       |                                                            |                          |
| 33      | NC             |       |                                                            |                          |
| 34      | SWMG/TEST7     | I(O)  | Enable input signal to display sub picture ("H" enable)    | pull up 15k              |
| 35      | DVdd3          | Vdd   | Connect to digital power supply                            |                          |
| 36      | DVss3          | GND   | Connect to digital GND                                     |                          |
| 37      | Cout-sub       | O     | D/A output signal (Chroma signal of sub-picture)           |                          |
| 38      | ADJ-Csub       | I     | D/A adjust for chroma signal (sub-picture)                 |                          |
| 39      | Yout-sub       | O     | D/A output signal (Luma signal of sub-picture)             |                          |
| 40      | ADJ-Ysub       | I     | D/A adjust for luma signal (sub-picture)                   |                          |
| 41      | Y-PIPin        | I     | PIP luma signal re-input                                   |                          |
| 42      | AVss4 (da)     | GND   | Connects to analog GND                                     |                          |
| 43      | AVss4 (da)     | GND   | Connects to analog GND                                     |                          |
| 44      | C-PIPin        | I     | PIP chroma signal re-input                                 |                          |
| 45      | AVdd4 (da)     | Vdd   | Connect to analog power supply                             |                          |
| 46      | AVdd4 (da)     | Vdd   | Connect to analog power supply                             |                          |
| 47      | AVdd4 (da)     | Vdd   | Connect to analog power supply                             |                          |
| 48      | C-PIP          | O     | PIP chroma signal output                                   |                          |
| 49      | NC             |       |                                                            |                          |
| 50      | TEST8          | I     | For test (connect to analog GND)                           | pull up 15k              |
| 51      | Y-PIP          | O     | PIP luma signal output                                     |                          |
| 52      | TEST9          | I     | For test (connect to analog GND)                           | connect to GND           |

# PRELIMINARY

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## M65667FP

### PICTURE-IN-PICTURE SIGNAL PROCESSING

#### DESCRIPTION OF PIN (cont.)

| Pin No. | Name         | I/O | Function                           | Remarks        |
|---------|--------------|-----|------------------------------------|----------------|
| 53      | Yin          | I   | Luma input signal (main-picture)   |                |
| 54      | TESTEN       | I   | For test (connect to analog GND)   | connect to GND |
| 55      | Cin          | I   | Chroma input signal (main-picture) |                |
| 56      | AVss (ana)   | GND | Connect to analog GND              |                |
| 57      | AVss3 (vcxo) | GND | Connects to analog GND             |                |
| 58      | VCXO out     | O   | VCXO output signal                 |                |
| 59      | VCXO in      | I   | VCXO input signal                  |                |
| 60      | FILTER       | I   | Filter                             |                |
| 61      | BIAS         | O   | Bias                               |                |
| 62      | AVdd3 (vcxo) | Vdd | Connect to analog power supply     |                |
| 63      | AVdd2 (m)    | Vdd | Connect to analog power supply     |                |
| 64      | AVdd2 (m)    | Vdd | Connect to analog power supply     |                |

#### ABSOLUTE MAXIMUM RATINGS (Vss=0V)

| Symbol | Parameter             | Limits |                   | Unit |
|--------|-----------------------|--------|-------------------|------|
|        |                       | Min.   | Max.              |      |
| VDD3   | Supply voltage (3.3V) | -0.3   | 4.6               | V    |
| Vi     | Input voltage         | -0.3   | VDD3+0.3          | V    |
| Vo     | Output voltage        | -0.3   | VDD3+0.3          | V    |
| Io     | Output current (1)    |        | IOL=20<br>IOH=-26 | mA   |
| Pa     | Power dissipation     |        | 1400              | mW   |
| Topr   | Operating temperature | -20    | 75                | °C   |
| Tstg   | Storage temperature   | -50    | 125               | °C   |

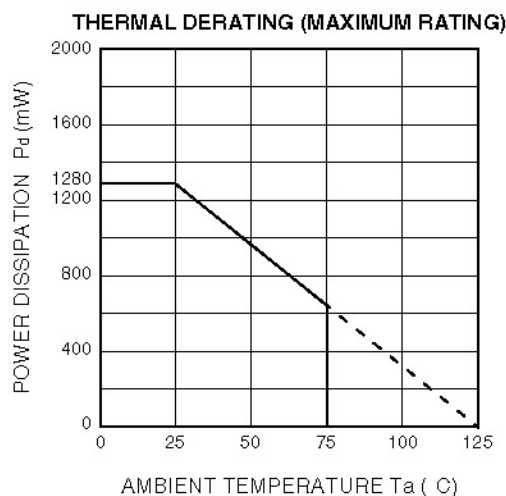
1: Output current per output terminal. But Pa limits all current.

**PRELIMINARY**

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**M65667FP****PICTURE-IN-PICTURE SIGNAL PROCESSING****DC CHARACTERISTICS** ( $T_a=25^\circ\text{C}$ , unless otherwise noted,  $V_{SS}=0\text{V}$ )

| Symbol           | Parameter                                         |             | Test conditions                               | Limits |      |      | Unit |
|------------------|---------------------------------------------------|-------------|-----------------------------------------------|--------|------|------|------|
|                  |                                                   |             |                                               | Min.   | Typ. | Max. |      |
| V <sub>IL</sub>  | Input voltage<br>(CMOS interface)                 | L           | V <sub>DD</sub> =2.7V                         | 0      |      | 0.81 | V    |
| V <sub>IH</sub>  |                                                   | H           | V <sub>DD</sub> =3.6V                         | 2.52   |      | 3.6  | V    |
| V <sub>T-</sub>  | Input voltage schmitt trigger<br>(CMOS interface) | —           | V <sub>DD</sub> =3.3V                         | 0.5    |      | 1.65 | V    |
| V <sub>T+</sub>  |                                                   | +           |                                               | 1.4    |      | 2.4  | V    |
| V <sub>H</sub>   |                                                   | Hysteresis  |                                               | 0.3    |      | 1.2  | V    |
| V <sub>OL</sub>  | Output voltage                                    | L           | V <sub>DD</sub> =3.3V,  I <sub>o</sub>   <1 A |        |      | 0.05 | V    |
| V <sub>OH</sub>  |                                                   | H           |                                               | 3.25   |      |      | V    |
| I <sub>OL</sub>  | Output current                                    | L           | V <sub>DD</sub> =3.0V, V <sub>OL</sub> =0.4V  | 4      |      |      | mA   |
| I <sub>OH</sub>  |                                                   | H           | V <sub>DD</sub> =3.0V, V <sub>OH</sub> =2.6V  |        |      | -4   | mA   |
| I <sub>IH</sub>  | Input current                                     | L           | V <sub>DD</sub> =3.6V, V <sub>I</sub> =0V     | -1     |      | 1    | A    |
| I <sub>IL</sub>  |                                                   | H           | V <sub>DD</sub> =3.6V, V <sub>I</sub> =3.6V   | -1     |      | 1    | A    |
| I <sub>oZL</sub> | Output leakage current                            | L           | V <sub>DD</sub> =3.6V, V <sub>o</sub> =0V     | -1     |      | 1    | A    |
| I <sub>oZH</sub> |                                                   | H           | V <sub>DD</sub> =3.6V, V <sub>o</sub> =3.6V   | -1     |      | 1    | A    |
| C <sub>i</sub>   | Input pin capacitance                             |             | f=1MHz, V <sub>DD</sub> =0V                   |        | 7    | 15   | pF   |
| C <sub>o</sub>   | Output pin capacitance                            |             |                                               |        | 7    | 15   | pF   |
| C <sub>io</sub>  | Bidirectional pin capacitance                     |             |                                               |        | 7    | 15   | pF   |
| I <sub>DD</sub>  | Operating current                                 | 3.3V supply |                                               |        |      | 140  | mA   |

**TYPICAL CHARACTERISTICS**

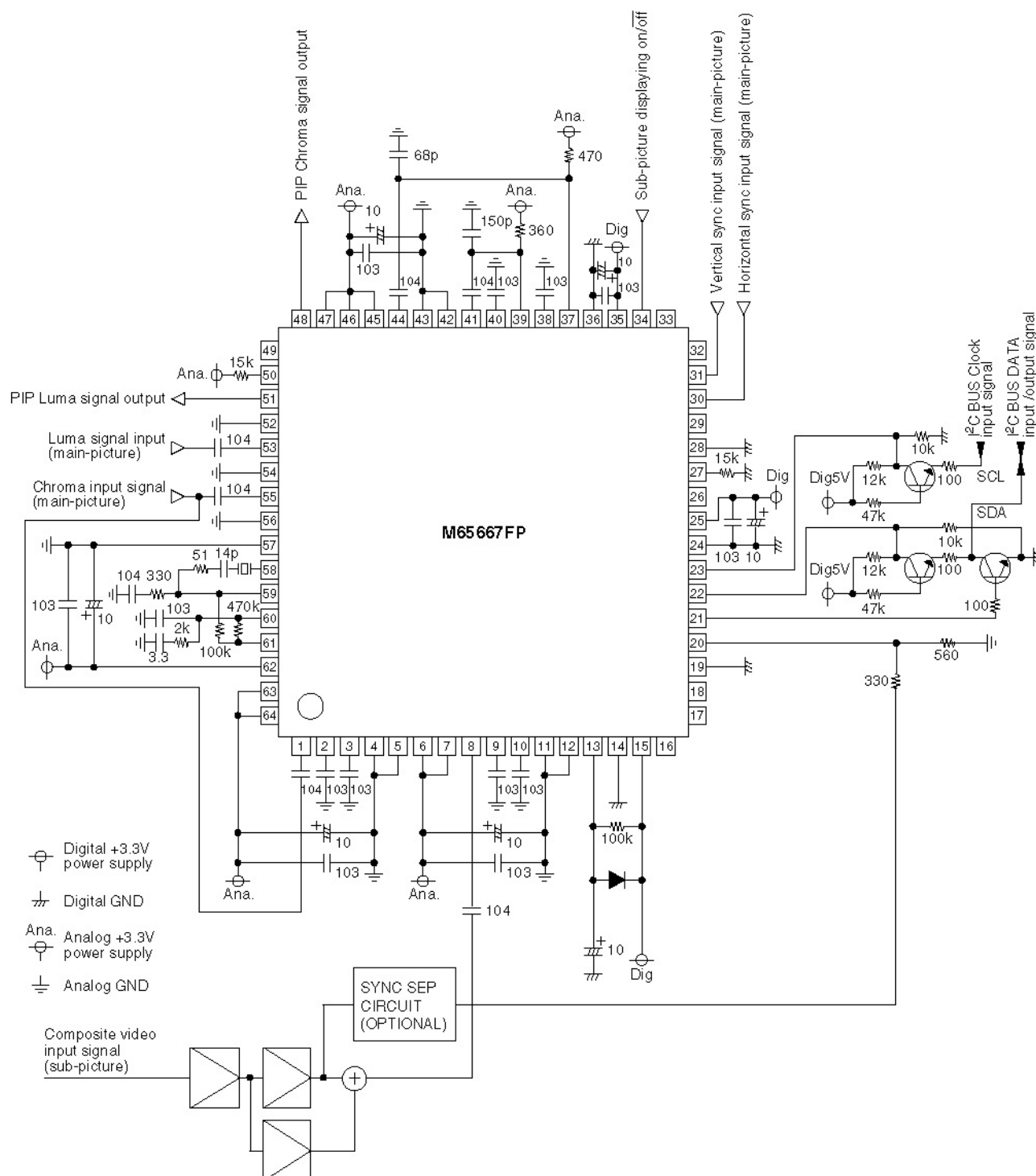
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## M65667FP

## PICTURE-IN-PICTURE SIGNAL PROCESSING

## APPLICATION EXAMPLE



Separate Y/C signals by using LC-tank circuit or LPF, BPF for Y/C signals level adjust.  
And then mix both signals for sub-picture input video signal.

Units Resistance :  
Capacitance : F

# PRELIMINARY

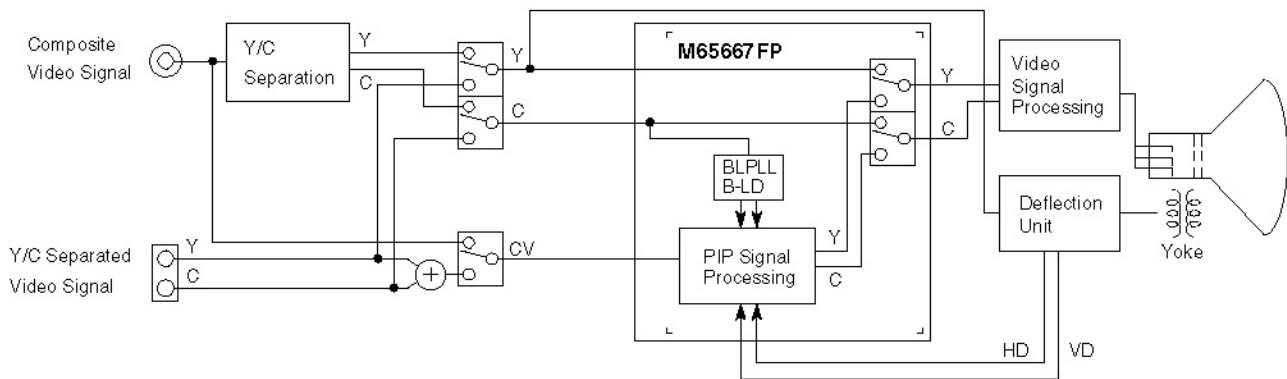
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## M65667FP

### PICTURE-IN-PICTURE SIGNAL PROCESSING

#### PIP TV SYSTEM BLOCK DIAGRAM

(BASIC)



#### (Driving Method and Operating Specification for Serial Interface Data)

##### (1) Serial data transmission completion and start

A low-to-high transition of the DATA (serial data) line while the CLK (serial clock) is high, that completes the serial transmission and makes the bus free.

A high-to-low transition of the DATA line while the CLK is high, that starts the serial transmission and waits for the following CLK and DATA inputs.

##### (2) Serial data transmission

The data are transmitted in the most significant bit (MSB) first by one-byte unit on the DATA line successively. One-byte data transmission is completed by 9 clock cycles, the former 8 cycles are for address/data and the latter one is for acknowledge detection. (In reading state, ACK is 'H' under these two conditions ; 1) the coincidence of two address data for the address data transmission, 2) the completion of 8-bit setting data transfer. In writing state, ACK is 'H' with the address coincidence and ACK is 'L' for detecting acknowledge input from the master (micro processor) after sending 8-bit setting data.)

For address/data transmission, DATA must change while CLK is 'L'. (The data change while CLK is 'H' or the simultaneous change of CLK and DATA, that will be a false operation because of undistinguished condition from the completion/start of serial data transfer).

After the beginning of serial data transmission, the total number of data bytes that can be transferred are not limited.

##### (3) The byte format of data transmission (The sequence of data transmission)

1. The byte format during data setting to M65667FP are shown as follows.

In right after the forming of serial data transmitting state, the slave address 24h (00100100b) is transferred. Afterwards, the internal register address (1 byte) and setting data (by 1 byte unit) are transferred successively. Several bytes of setting data can be handled in the one transmission. In this operation, the setting data are written into the address register whose address is increased one in initially transferred internal register address. (The next address of 7Fh, it returns to 00h).

2. The byte format during data reading from M65667FP are shown as follows.

Before data reading from M65667FP, whose internal address need to be set by the data reading/transmitting. After the data reading/transmitting, the operation of "serial data transmission completion and start" (described in (1)) is necessary. Continuously, the slave address 25h (00100101b) is sent, and then the inverted read out data are available on ACK. Several bytes of writing data can be handled in the one transmission, too. In this operation, the setting data also are written into the address register whose address is increased one in initially transferred internal register address. (The next address of 7Fh, it returns to 00h).

# PRELIMINARY

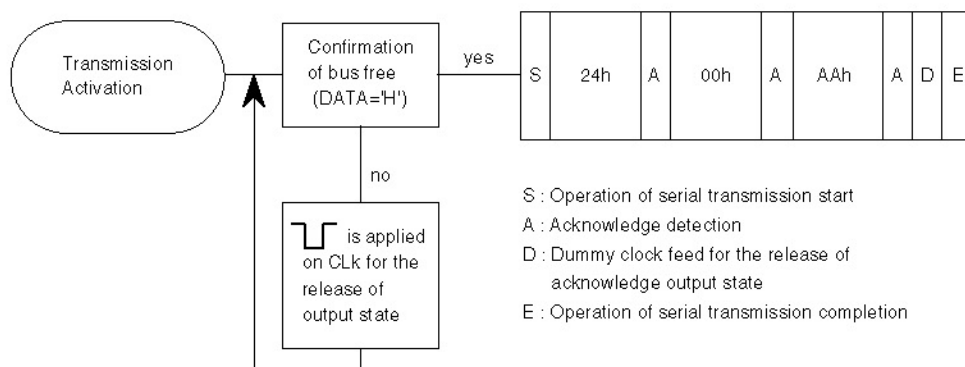
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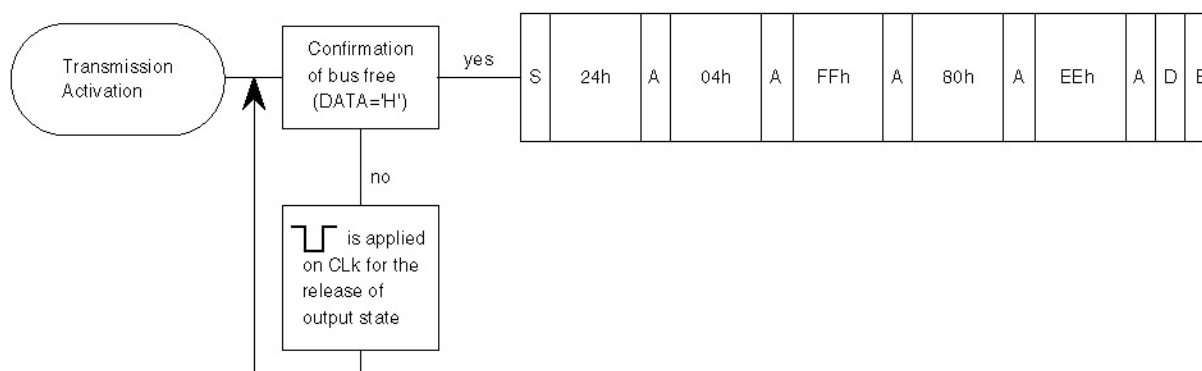
### PICTURE-IN-PICTURE SIGNAL PROCESSING

#### (The examples of serial byte transmission format)

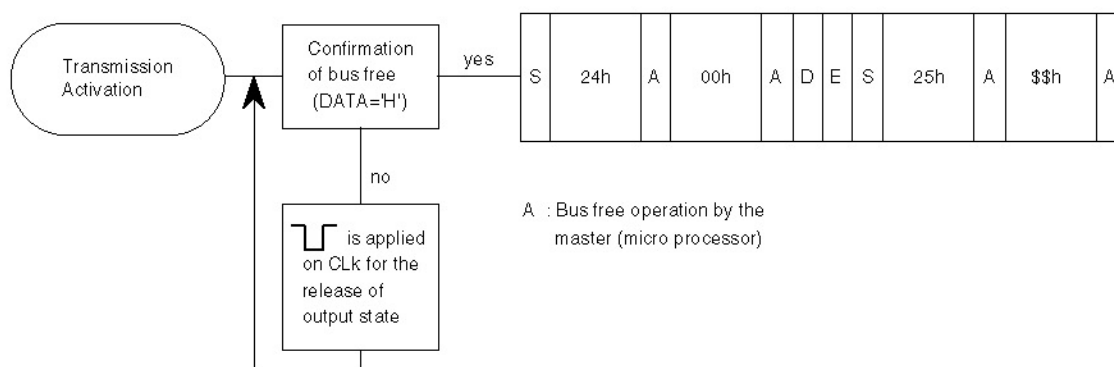
(1) The writing operation of the setting data (AAh) into M65667FP internal address of 00h



(2) The writing operation of the setting data (FFh, 80h, EEh) into M65667FP internal address of 04h to 06h



(3) The reading operation of the setting data from M65667FP internal address of 00h



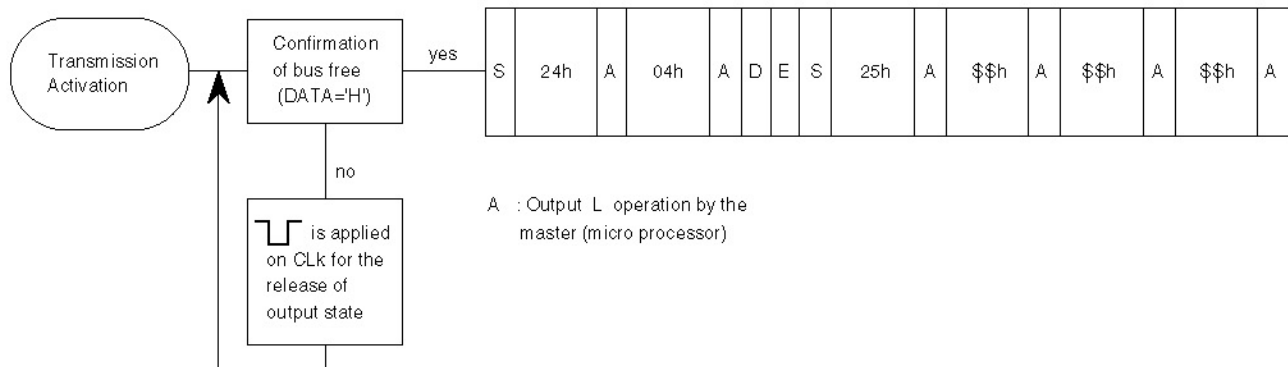
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## M65667FP

### PICTURE-IN-PICTURE SIGNAL PROCESSING

(4) The reading operation of the setting data from M65667FP internal address of 04h to 06h



### TIMING DIAGRAM

