STM690, STM704, STM795
STM802, STM804, STM805, STM806

3V Supervisor with Battery Switchover

FEATURES SUMMARY

- RST OR $\overline{\text{RST}}$ OUTPUTS
- NVRAM SUPERVISOR FOR EXTERNAL LPSRAM
- CHIP-ENABLE GATING (STM795 only) FOR EXTERNAL LPSRAM (7ns max PROP DELAY)
- MANUAL (PUSH-BUTTON) RESET INPUT
- 200ms (TYP) t_{rec}
- WATCHDOG TIMER - 1.6sec (TYP)
- AUTOMATIC BATTERY SWITCHOVER
- LOW BATTERY SUPPLY CURRENT - 0.4µA (TYP)
- POWER-FAIL COMPARATOR (PFI/$\overline{\text{PFO}}$)
- LOW SUPPLY CURRENT - 40µA (TYP)
- GUARANTEED $\overline{\text{RST}}$ (RST) ASSERTION DOWN TO V_{CC} = 1.0V
- OPERATING TEMPERATURE:
  –40°C to 85°C (Industrial Grade)

Figure 1. Packages

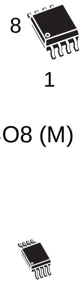

Table 1. Device Options

	Watchdog Input	Active-Low $\overline{\text{RST}}$(1)	Active-High RST	Manual Reset Input	Battery Switch-over	Power-fail Compar-ator	Chip-Enable Gating
STM690	✔	✔			✔	✔	
STM704		✔		✔	✔	✔	
STM795		✔(2)			✔		✔
STM802	✔	✔			✔	✔	
STM804	✔		✔(2)		✔	✔	
STM805	✔		✔(2)		✔	✔	
STM806		✔		✔	✔	✔	

Note: 1. All $\overline{\text{RST}}$ outputs push-pull (unless otherwise noted)
2. Open drain output.

* Contact local ST sales office for availability.

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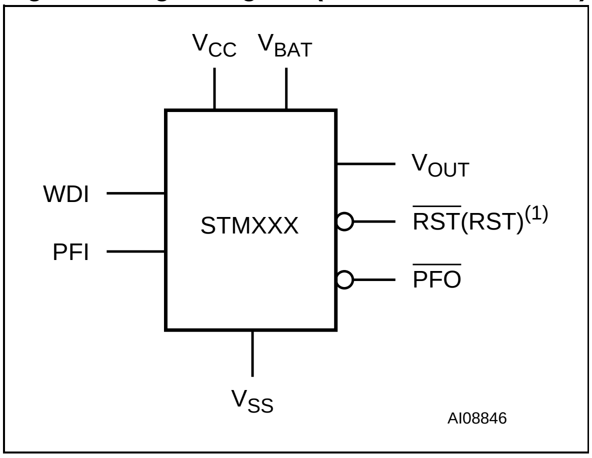
SUMMARY DESCRIPTION

The STMXXX Supervisors are self-contained devices which provide microprocessor supervisory functions with the ability to non-volatize and write-protect external LPSRAM. A precision voltage reference and comparator monitors the V_{CC} input for an out-of-tolerance condition. When an invalid V_{CC} condition occurs, the reset output ($\overline{RST}$) is forced low (or high in the case of RST). These devices also offer a watchdog timer (except for STM704/795/806) as well as a power-fail comparator (except for STM795) to provide the system with an early warning of impending power failure.

These devices are available in a standard 8-pin SOIC package or a space-saving 8-pin TSSOP package.

Figure 2. Logic Diagram (STM690/802/804/805)



Note: 1. For STM804/805, reset output is active-high and open drain.

Figure 3. Logic Diagram (STM704/806)

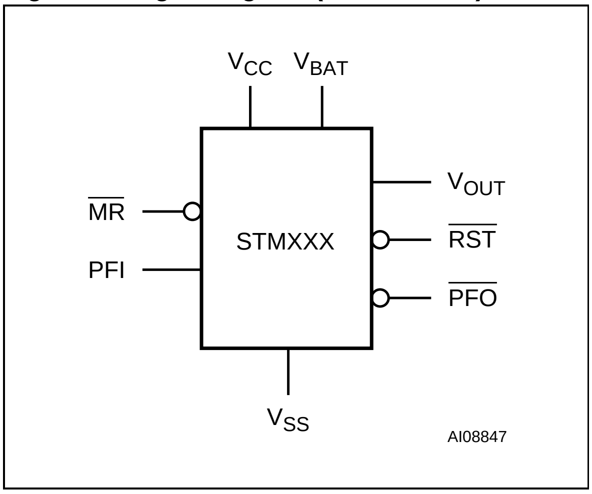


Figure 4. Logic Diagram (STM795)

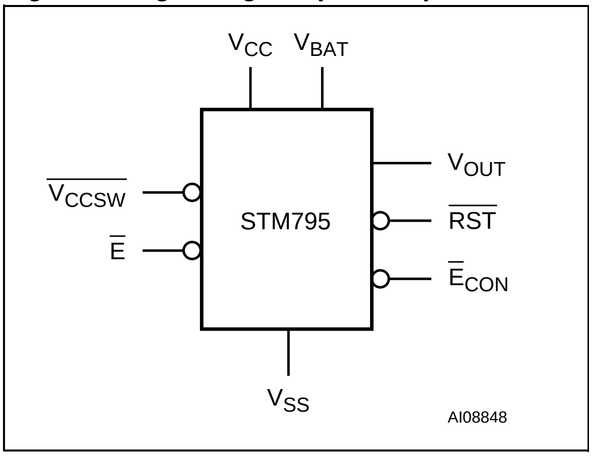
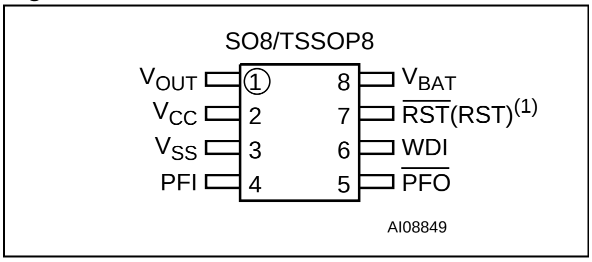


Table 2. Signal Names

$\overline{MR}$	Push-button Reset Input
WDI	Watchdog Input
$\overline{RST}$	Active-Low Reset Output
RST(1)	Active-High Reset Output
$\overline{E}$(2)	Chip Enable Input
$\overline{E}_{CON}$(2)	Conditioned Chip Enable Output
$\overline{V_{CCSW}}$(2)	V_{CC} Switch Output
V_{OUT}	Supply Voltage Output
V_{CC}	Supply Voltage
V_{BAT}	Back-up Supply Voltage
PFI	Power-fail Input
$\overline{PFO}$	Power-fail Output
V_{SS}	Ground

Note: 1. Open drain for STM804/805 only.
2. STM795

Figure 5. STM690/802/804/805 Connections



Note: 1. For STM804/805, reset output is active-high and open drain.

Figure 6. STM704/806 Connections

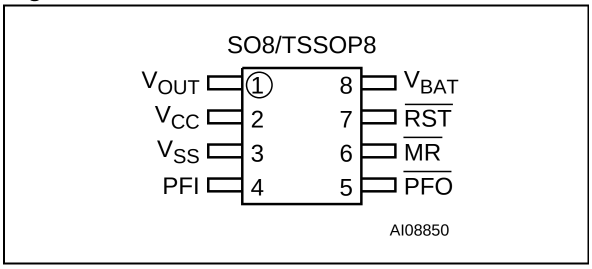


Figure 7. STM795 Connections

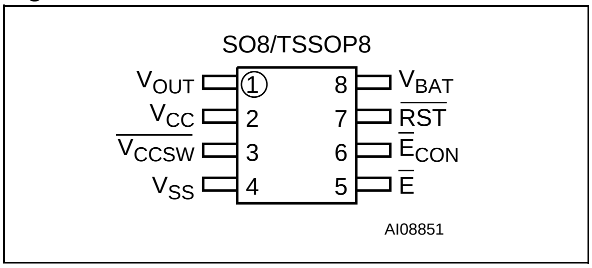
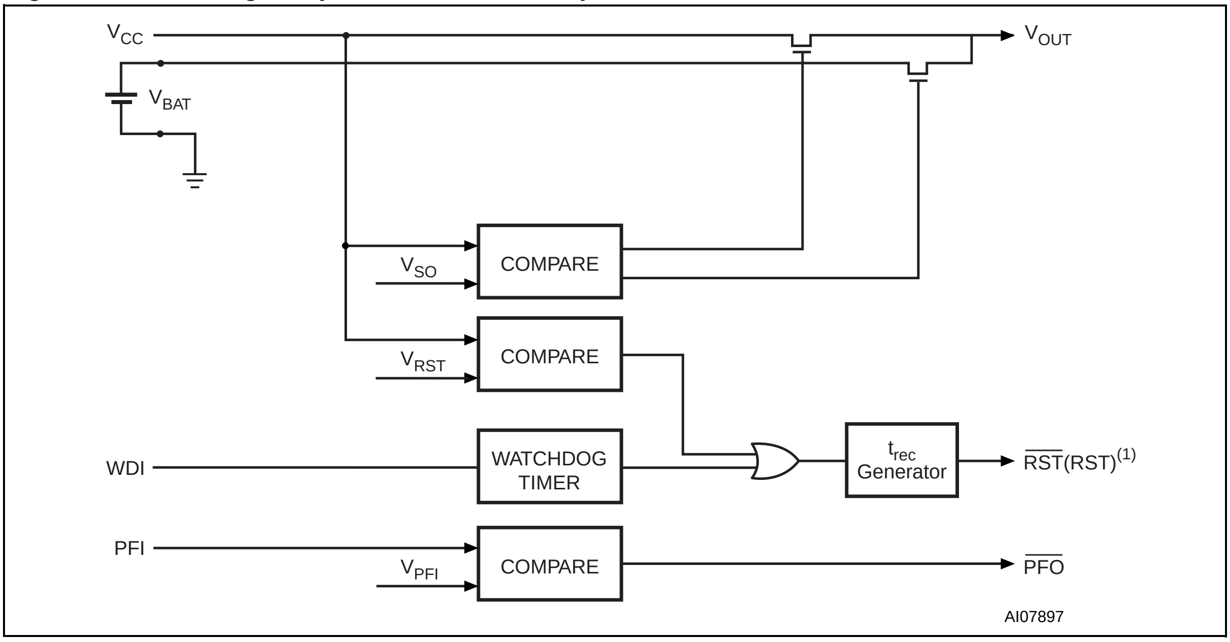


Table 3. Pin Description

Pin				Name	Function
STM795	**STM690 STM802**	**STM704 STM806**	**STM804 STM805**		
–	–	6	–	$\overline{MR}$	**Push-button Reset Input.** A logic low on /MR asserts the reset output. Reset remains asserted as long as $\overline{MR}$ is low and for t_{rec} after $\overline{MR}$ returns high. This active-low input has an internal pull-up. It can be driven from a TTL or CMOS logic line, or shorted to ground with a switch. Leave open if unused.
–	6	–	6	WDI	**Watchdog Input.** If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and reset is triggered. The internal watchdog timer clears while reset is asserted or when WDI sees a rising or falling edge. The watchdog function cannot be disabled by allowing the WDI pin to float.
–	–	–	7	RST	**Active-High Reset Output.** Inverse of $\overline{RST}$. (Open drain)
–	4	4	4	PFI	**PFI Power-fail Input.** When PFI is less than V_{PFI} or when V_{CC} falls below V_{SW} (2.4V), $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high. Connect to ground if unused.
–	5	5	5	$\overline{PFO}$	**$\overline{PFO}$ Power-fail Output.** When PFI is less than V_{PFI}, or V_{CC} falls below V_{SW}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high. Leave open if unused.
1	1	1	1	V_{OUT}	**Supply Output for External LPSRAM.** When V_{CC} is above the switchover voltage (V_{SO}), V_{OUT} is connected to V_{CC} through a P-channel MOSFET switch. When V_{CC} falls below V_{SO}, V_{BAT} connects to V_{OUT}. Connect to V_{CC} if no battery is used.

Pin				Name	Function
STM795	STM690 STM802	STM704 STM806	STM804 STM805		
2	2	2	2	V_{CC}	**Supply Voltage.**
3	–	–	–	$\overline{Vccsw}$	**V_{CC} Switch Output.** When V_{OUT} switches to battery, $\overline{Vccsw}$ is high. When V_{OUT} switches back to V_{CC}, $\overline{Vccsw}$ is low. It can be used to drive gate of external PMOS transistor for I_{OUT} requirements exceeding 75mA.
4	3	3	3	V_{SS}	**Ground.**
5	–	–	–	$\overline{E}$	**Chip Enable Input.** The input to the chip-enable gating circuit. Connect to ground if unused.
6	–	–	–	$\overline{E}_{CON}$	**Conditioned Chip Enable Output.** $\overline{E}_{CON}$ goes low only when $\overline{E}$ is low and reset is not asserted. If $\overline{E}_{CON}$ is low when reset is asserted, $\overline{E}_{CON}$ will remain low for 15µs or until $\overline{E}$ goes high, whichever occurs first. In the disabled mode, $\overline{E}_{CON}$ is pulled up to V_{OUT}.
7	7	7	–	$\overline{RST}$	**Active-Low Reset Output.** Pulses low for t_{rec} when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is a logic low. It remains low for t_{rec} after either V_{CC} rises above the reset threshold, the watchdog triggers a reset, or $\overline{MR}$ goes from low to high.
8	8	8	8	V_{BAT}	**Backup-Battery Input.** When V_{CC} falls below V_{SO}, V_{OUT} switches from V_{CC} to V_{BAT}. When V_{CC} rises above V_{SO} + hysteresis, V_{OUT} reconnects to V_{CC}. V_{BAT} may exceed V_{CC}. Connect to V_{CC} if no battery is used.

Figure 8. Block Diagram (STM690/802/804/805)



Note: 1. For STM804/805, reset output is active-high and open drain.

Figure 9. Block Diagram (STM704/806)

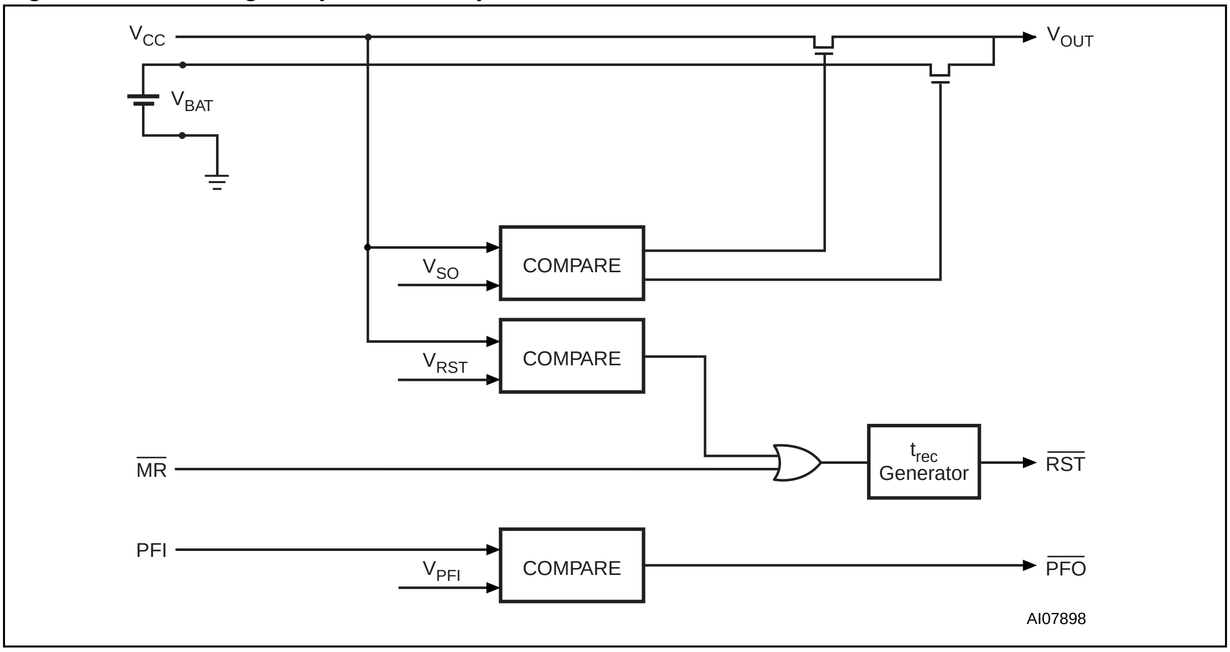


Figure 10. Block Diagram (STM795)

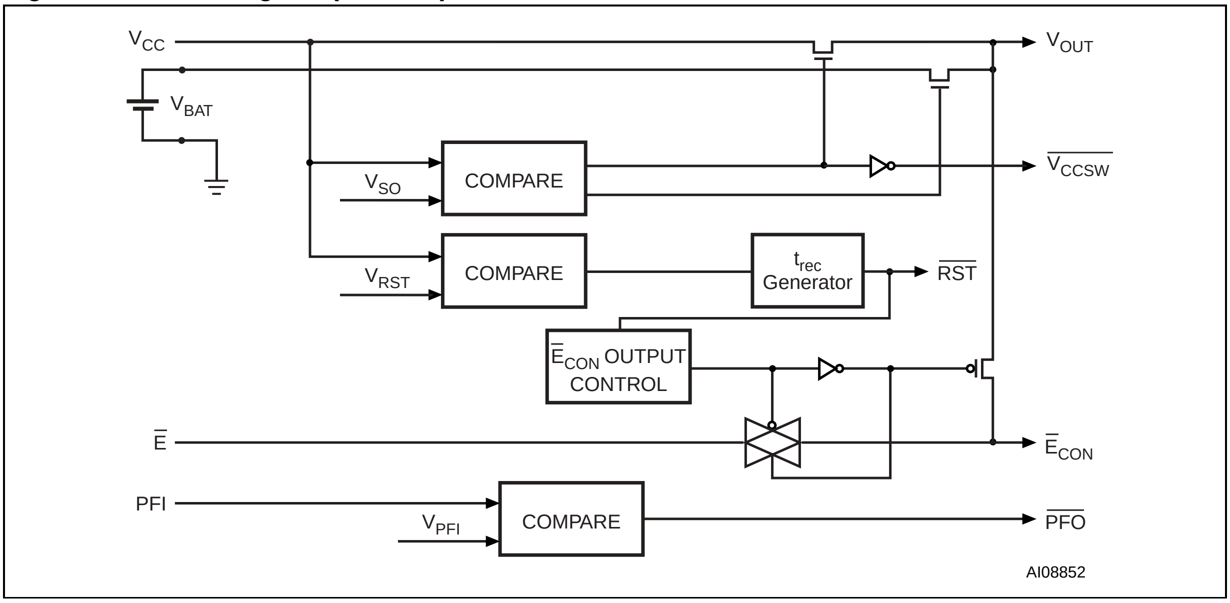
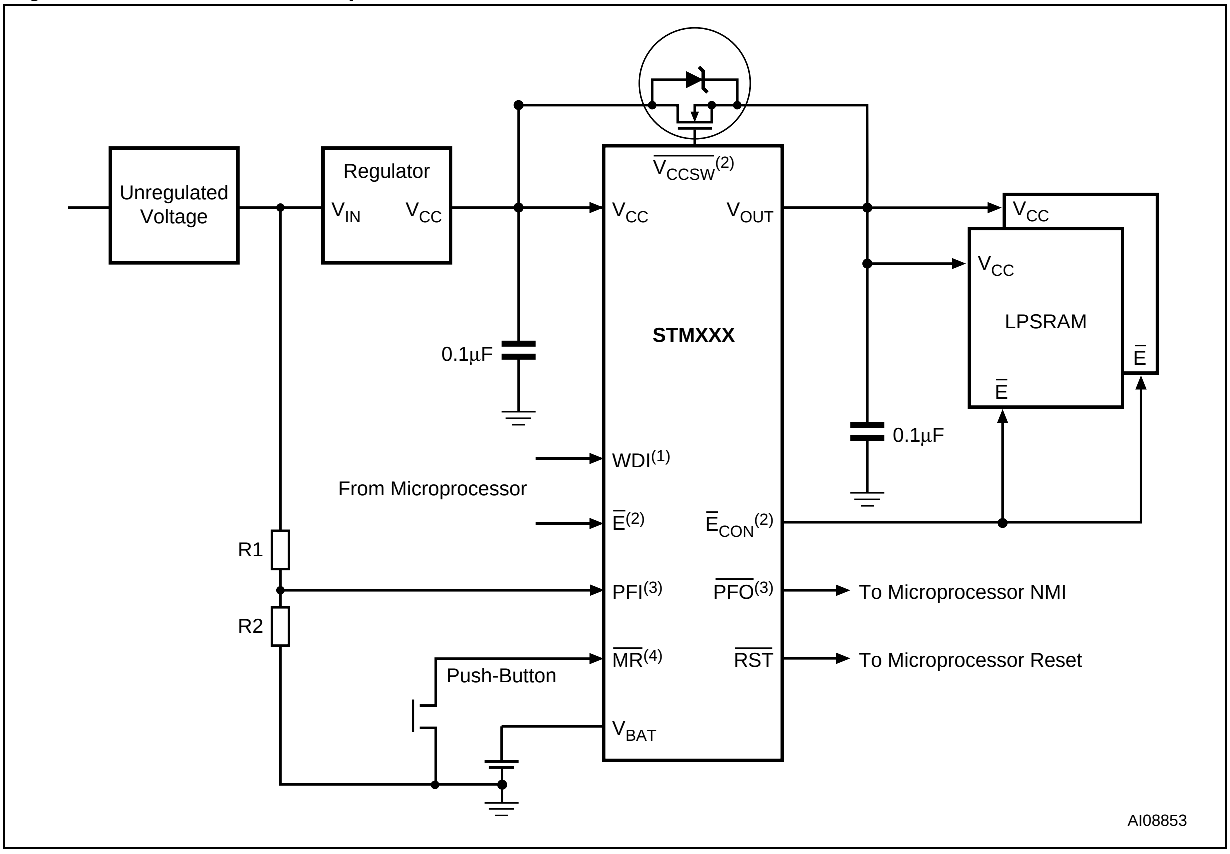


Figure 11. Hardware Hookup



Note: 1. For STM690/802/804/805.
2. For STM795 only.
3. Not available on STM795.
4. For STM704/806.

OPERATION

Reset Output

The STMXXX SUPERVISOR asserts a reset signal to the MCU whenever V_{CC} goes below the reset threshold (V_{RST}), a watchdog time-out occurs, or when the Push-button Reset Input ($\overline{MR}$) is taken low. $\overline{RST}$ is guaranteed to be a logic low (logic high for STM804/805) for 0V < V_{CC} < V_{RST} if V_{BAT} is greater than 1V. Without a back-up battery, $\overline{RST}$ is guaranteed valid down to V_{CC} =1V.

During power-up, once V_{CC} exceeds the reset threshold an internal timer keeps $\overline{RST}$ low for the reset time-out period, t_{rec}. After this interval $\overline{RST}$ returns high.

If V_{CC} drops below the reset threshold, $\overline{RST}$ goes low. Each time $\overline{RST}$ is asserted, it stays low for at least the reset time-out period (t_{rec}). Any time V_{CC} goes below the reset threshold the internal timer clears. The reset timer starts when V_{CC} returns above the reset threshold.

Push-button Reset Input (STM704/806)

A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for t_{rec} (see Figure 36., page 22) after it returns high. The $\overline{MR}$ input has an internal 40kΩ pull-up resistor, allowing it to be left open if not used. This input can be driven with TTL/CMOS-logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity. $\overline{MR}$ may float, or be tied to V_{CC} when not used.

Watchdog Input (NOT available on STM704/795/806)

The watchdog timer can be used to detect an out-of-control MCU. If the MCU does not toggle the Watchdog Input (WDI) within t_{WD} (1.6sec typ), the reset is asserted. The internal watchdog timer is cleared by either:

1. a reset pulse, or
2. by toggling WDI (high-to-low or low-to-high), which can detect pulses as short as 50ns. If WDI is tied high or low, a reset pulse is triggered every 1.8sec (t_{WD} + t_{rec}).

The timer remains cleared and does not count for as long as reset is asserted. As soon as reset is released, the timer starts counting (see Figure 37., page 23).

Note: Input frequency greater than 20ns (50MHz) will be filtered.

Back-up Battery Switchover

In the event of a power failure, it may be necessary to preserve the contents of external SRAM through V_{OUT}. With a backup battery installed with voltage V_{BAT}, the devices automatically switch the SRAM to the back-up supply when V_{CC} falls.

Note: If back-up battery is not used, connect both V_{BAT} and V_{OUT} to V_{CC}.

This family of Supervisors does not always connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{CC}. V_{BAT} connects to V_{OUT} (through a 100Ω switch) when V_{CC} is below V_{SW} (2.4V) or V_{BAT} (whichever is lower). This is done to allow the back-up battery (e.g., a 3.6V lithium cell) to have a higher voltage than V_{CC}.

Assuming that V_{BAT} > 2.0V, switchover at V_{SO} ensures that battery back-up mode is entered before V_{OUT} gets too close to the 2.0V minimum required to reliably retain data in most external SRAMs. When V_{CC} recovers, hysteresis is used to avoid oscillation around the V_{SO} point. V_{OUT} is connected to V_{CC} through a 3Ω PMOS power switch.

Note: The back-up battery may be removed while V_{CC} is valid, assuming V_{BAT} is adequately decoupled (0.1µF typ), without danger of triggering a reset.

Table 4. I/O Status in Battery Back-up

Pin	Status
V_{OUT}	Connected to V_{BAT} through internal switch
V_{CC}	Disconnected from V_{OUT}
PFI	Disabled
$\overline{PFO}$	Logic low
$\overline{E}$	High impedance
$\overline{E}_{CON}$	Logic high
WDI	Watchdog timer is disabled
$\overline{MR}$	Disabled
$\overline{RST}$	Logic low
RST	Logic high
V_{BAT}	Connected to V_{OUT}
$\overline{V_{CCSW}}$	Logic high (STM795)

Chip-Enable Gating (STM795 only)

Internal gating of the chip enable ($\overline{E}$) signal prevents erroneous data from corrupting the external CMOS RAM in the event of an undervoltage condition. The STM795 uses a series transmission gate from $\overline{E}$ to $\overline{E}_{CON}$ (see Figure 12). During normal operation (reset not asserted), the $\overline{E}$ transmission gate is enabled and passes all $\overline{E}$ transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short $\overline{E}$ propagation delay from $\overline{E}$ to $\overline{E}_{CON}$ enables the STM795 to be used with most µPs. If $\overline{E}$ is low when reset asserts, $\overline{E}_{CON}$ remains low for typically 10µs to permit the current WRITE cycle to complete.

Chip Enable Input (STM795 only)

The chip-enable transmission gate is disabled and $\overline{E}$ is high impedance (disabled mode) while reset is asserted. During a power-down sequence when V_{CC} passes the reset threshold, the chip-enable transmission gate disables and $\overline{E}$ immediately becomes high impedance if the voltage at $\overline{E}$ is high. If $\overline{E}$ is low when reset asserts, the chip-enable transmission gate will disable 10µs after reset asserts (see Figure 13). This permits the current WRITE cycle to complete during power-down.

Any time a reset is generated, the chip-enable transmission gate remains disabled and $\overline{E}$ remains high impedance (regardless of $\overline{E}$ activity) for the reset time-out period. When the chip enable transmission gate is enabled, the impedance of $\overline{E}$ appears as a 40Ω resistor in series with the load at $\overline{E}_{CON}$. The propagation delay through the chip-enable transmission gate depends on V_{CC}, the source impedance of the drive connected to $\overline{E}$, and the loading on $\overline{E}_{CON}$ (see "Typical Operating Characteristics"). The chip enable propagation delay is production tested from the 50% point on $\overline{E}$ to the 50% point on $\overline{E}_{CON}$ using a 50Ω driver and a 50pF load capacitance (see Figure 35., page 22). For minimum propagation delay, minimize the capacitive load at $\overline{E}_{CON}$ and use a low-output impedance driver.

Chip Enable Output (STM795 only)

When the chip-enable transmission gate is enabled, the impedance of $\overline{E}_{CON}$ is equivalent to a 40Ω resistor in series with the source driving $\overline{E}$. In the disabled mode, the transmission gate is off and an active pull-up connects $\overline{E}_{CON}$ to V_{OUT} (see Figure 12). This pull-up turns off when the transmission gate is enabled.

Figure 12. Chip-Enable Gating

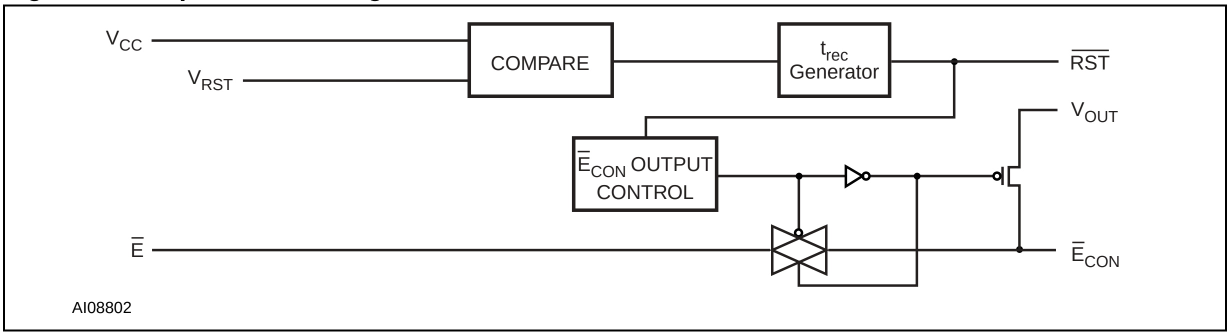
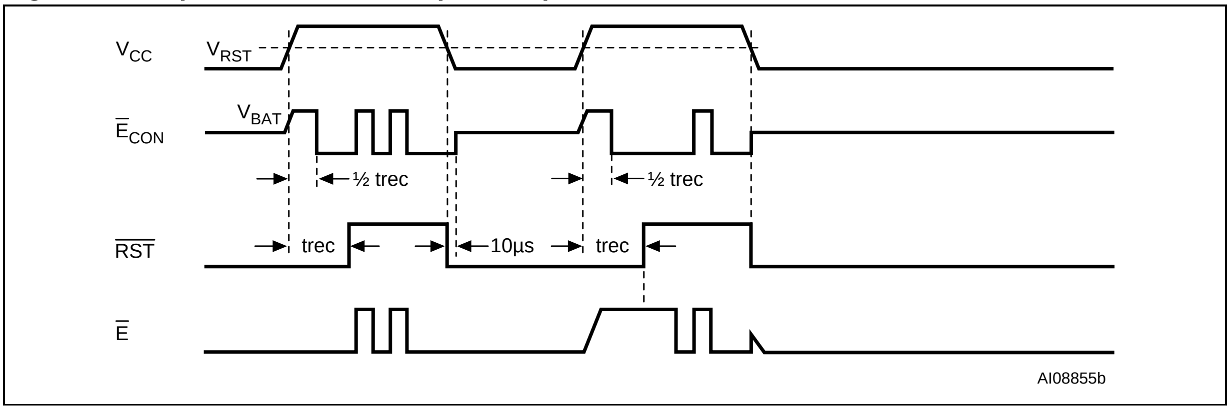


Figure 13. Chip Enable Waveform (STM795)



Power-fail Input/Output (NOT available on STM795)

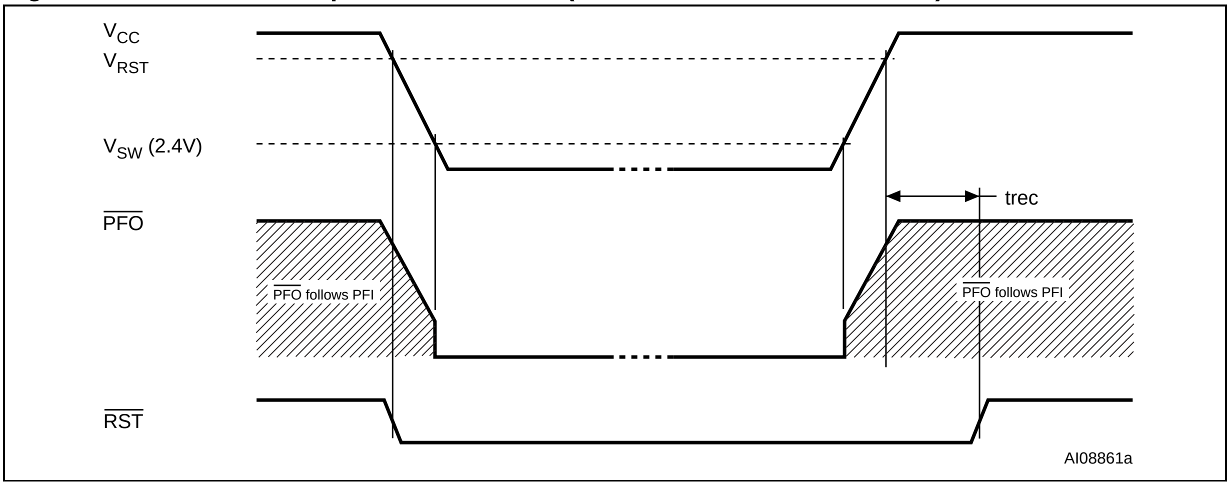
The Power-fail Input (PFI) is compared to an internal reference voltage (independent from the V_{RST} comparator). If PFI is less than the power-fail threshold (V_{PFI}), the Power-Fail Output ($\overline{PFO}$) will go low. This function is intended for use as an undervoltage detector to signal a failing power supply. Typically PFI is connected through an external voltage divider (see Figure 11., page 8) to either the unregulated DC input (if it is available) or the regulated output of the V_{CC} regulator. The voltage divider can be set up such that the voltage at PFI falls below V_{PFI} several milliseconds before the regulated V_{CC} input to the STMXXX or the microprocessor drops below the minimum operating voltage.

During battery back-up, the power-fail comparator is turned off and $\overline{PFO}$ goes (or remains) low (see Figure 14., page 11). This occurs after V_{CC} drops below V_{SW} (2.4V). When power returns, the power-fail comparator is enabled and $\overline{PFO}$ follows PFI. If the comparator is unused, PFI should be connected to V_{SS} and $\overline{PFO}$ left unconnected. $\overline{PFO}$ may be connected to $\overline{MR}$ on the STM704/806 so that a low voltage on PFI will generate a reset output.

Applications Information

These Supervisor circuits are not short-circuit protected. Shorting V_{OUT} to ground - excluding power-up transients such as charging a decoupling capacitor - destroys the device. Decouple both V_{CC} and V_{BAT} pins to ground by placing 0.1µF capacitors as close to the device as possible.

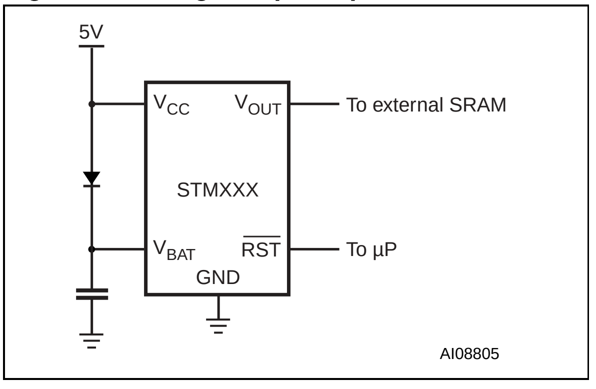
Figure 14. Power-fail Comparator Waveform (STM690/704/802/804/805/806)



Using a SuperCap™ as a Backup Power Source

SuperCaps™ are capacitors with extremely high capacitance values (e.g., order of 0.47F) for their size. Figure 15 shows how to use a SuperCap as a back-up power source. The SuperCap may be connected through a diode to the V_{CC} supply. Since V_{BAT} can exceed V_{CC} while V_{CC} is above the reset threshold, there are no special precautions when using these supervisors with a SuperCap.

Figure 15. Using a SuperCap™



Negative-Going V_{CC} Transients

The STMXXXs are relatively immune to negative-going V_{CC} transients (glitches). The graph was generated using a negative pulse applied to V_{CC}, starting at V_{RST} + 0.3V and ending below the reset threshold by the magnitude indicated (comparator overdrive). The graph indicates the maximum pulse width a negative V_{CC} transient can have without causing a reset pulse. As the magnitude of the transient increases (further below the threshold), the maximum allowable pulse width decreases. Any combination of duration and overdrive which lies under the curve will NOT generate a reset signal. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 40µs or less will not cause a reset pulse. A 0.1µF bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

TYPICAL OPERATING CHARACTERISTICS

Note: Typical values are at T_A = 25°C.

Figure 16. V_{BAT}-to-V_{OUT} On-Resistance vs. Temperature

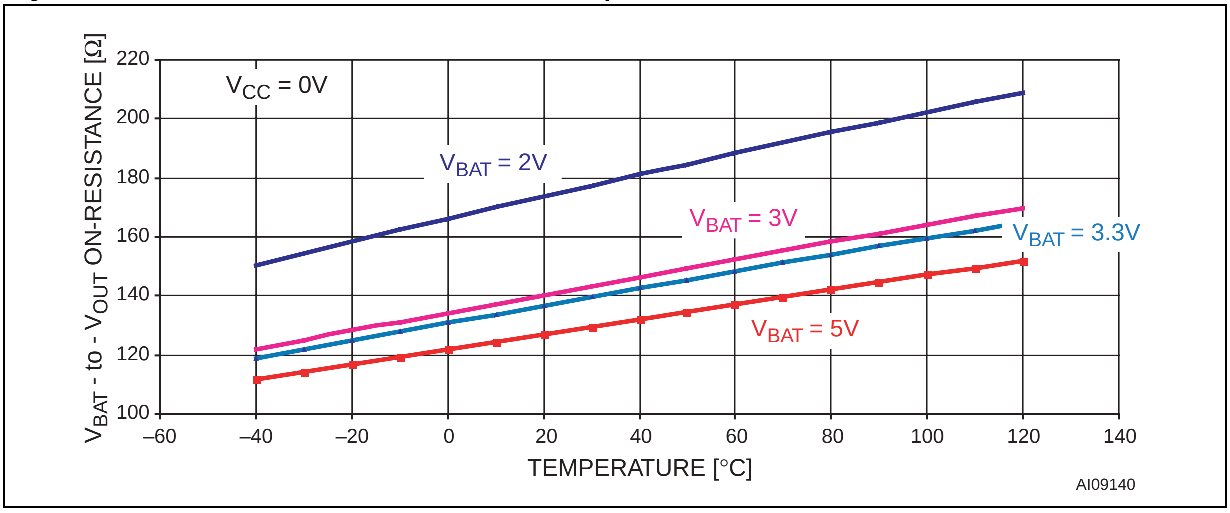


Figure 17. Supply Current vs. Temperature (no load)

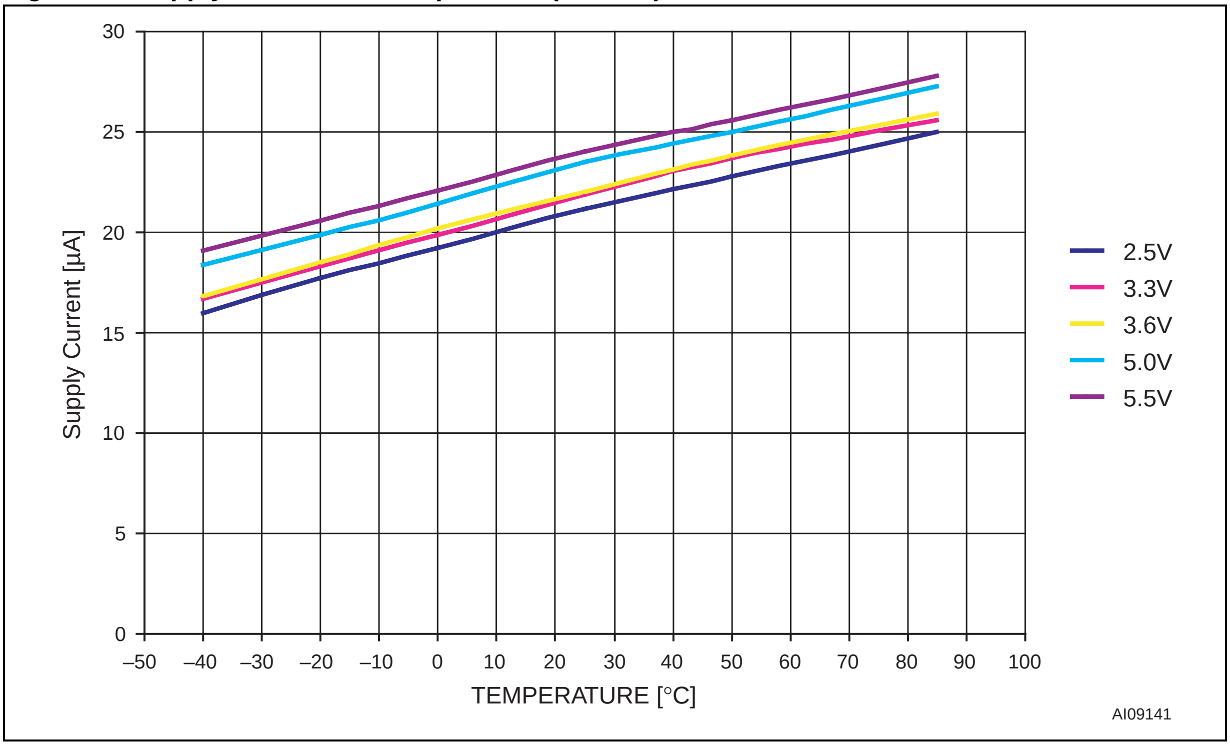


Figure 18. V_{PFI} Threshold vs. Temperature

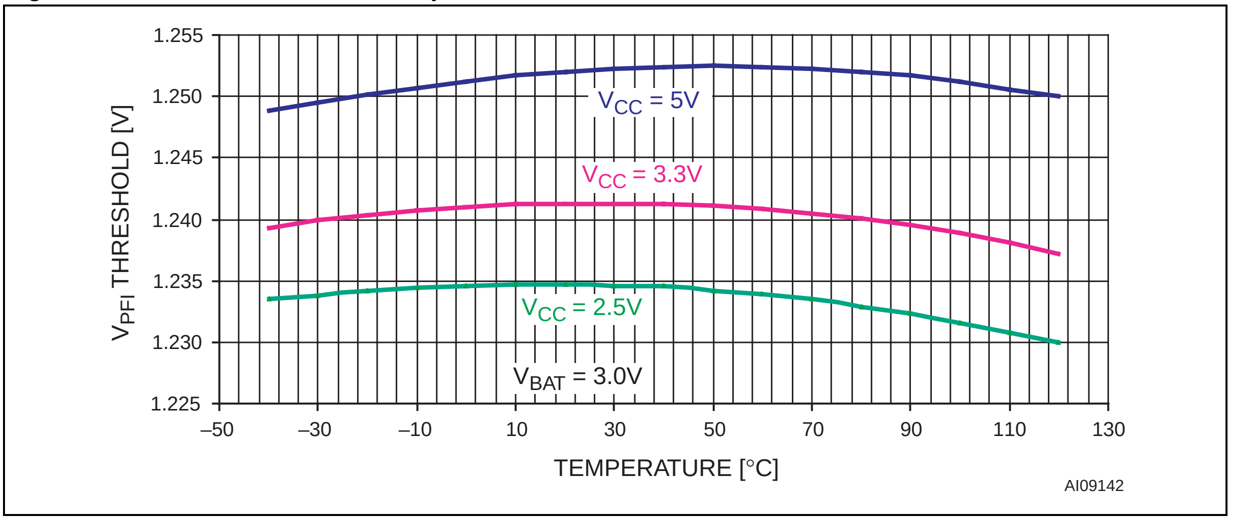


Figure 19. Reset Comparator Propagation Delay vs. Temperature

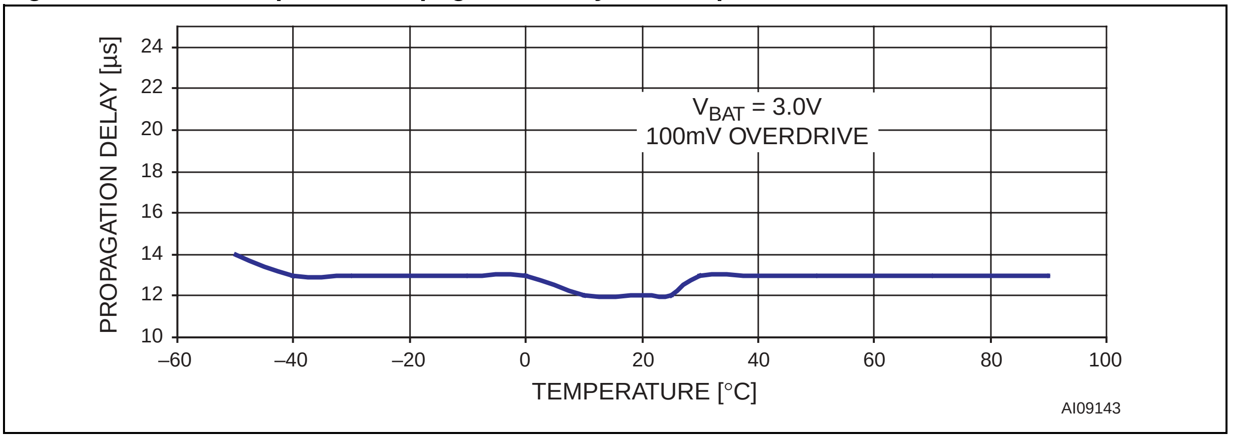


Figure 20. Power-up t_{rec} vs. Temperature

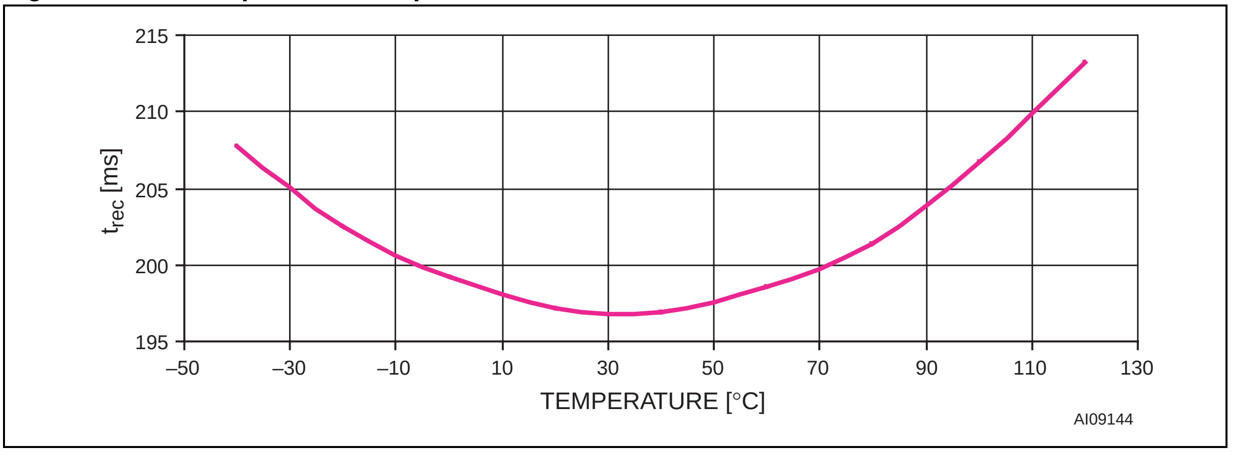


Figure 21. Normalized Reset Threshold vs. Temperature

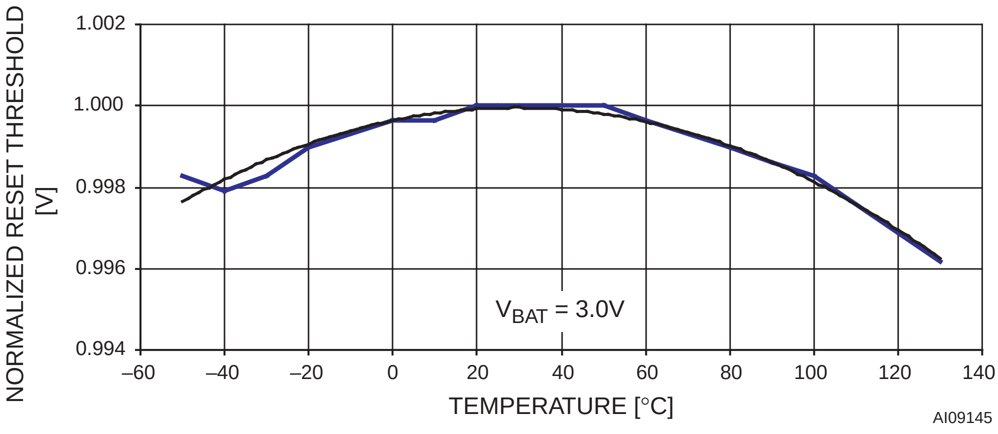


Figure 22. Watchdog Time-out Period vs. Temperature

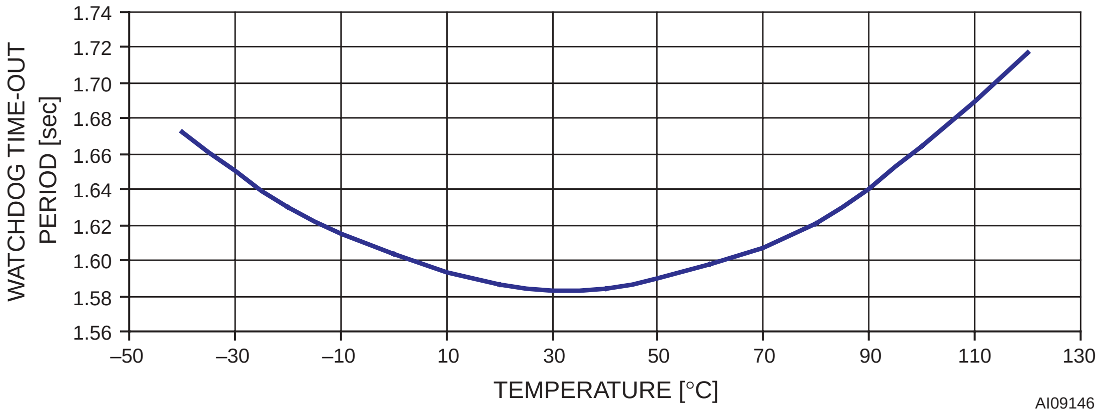


Figure 23. $\overline{E}$ to $\overline{E}_{CON}$ On-Resistance vs. Temperature

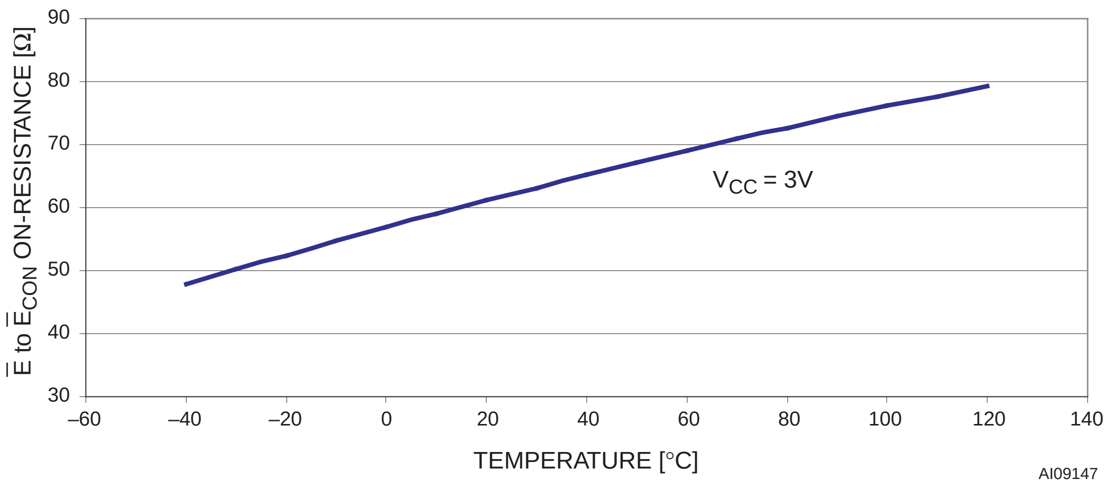


Figure 24. PFI to $\overline{\text{PFO}}$ Propagation Delay vs. Temperature

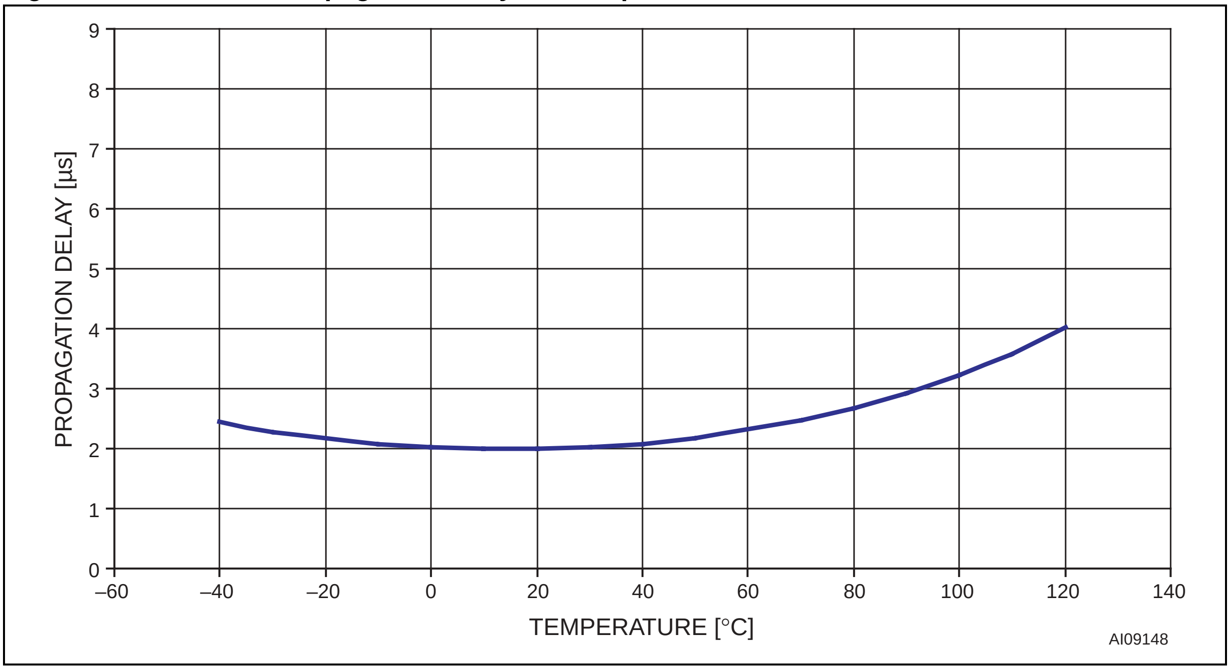


Figure 25. $\overline{\text{RST}}$ Output Voltage vs. Supply Voltage

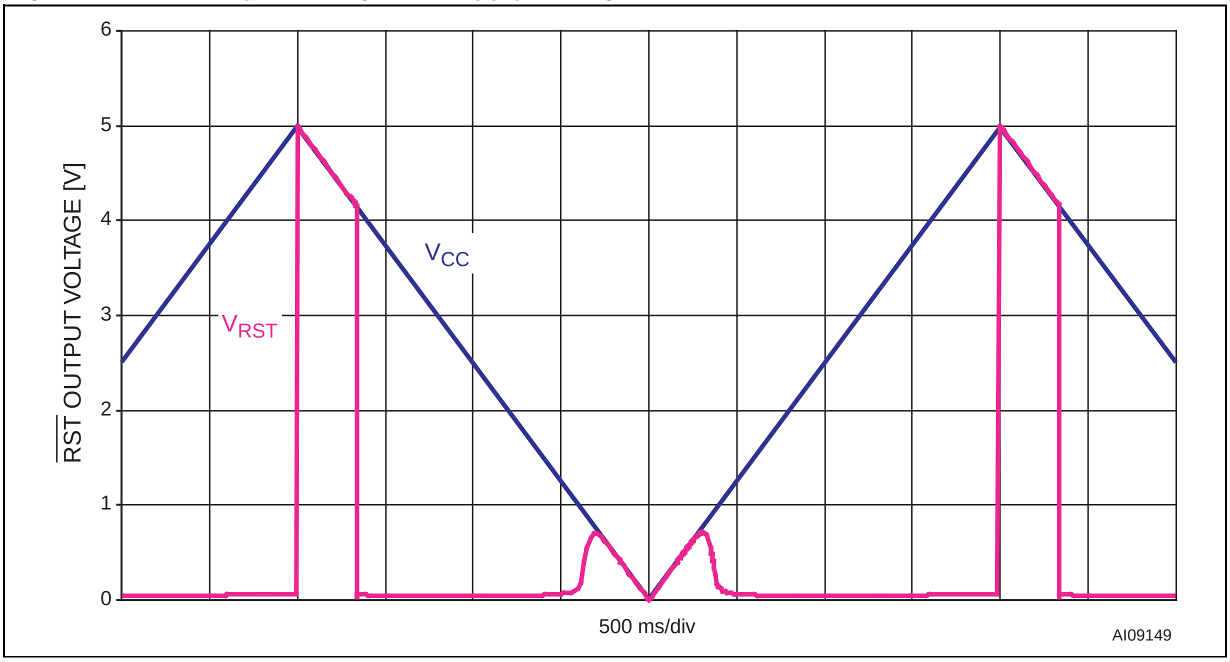


Figure 26. RST Output Voltage vs. Supply Voltage

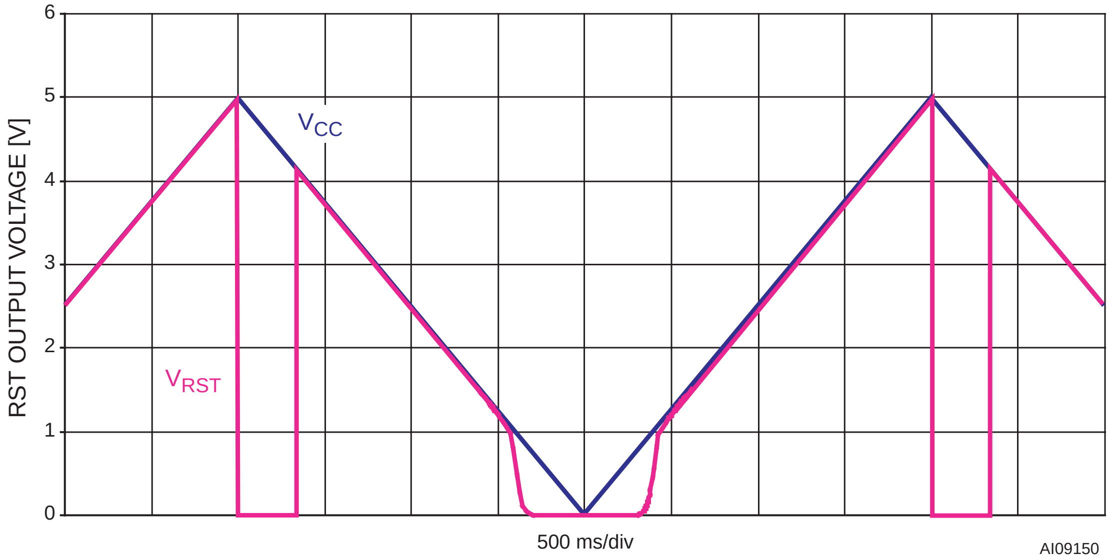


Figure 27. $\overline{\text{RST}}$ Response Time (Assertion)

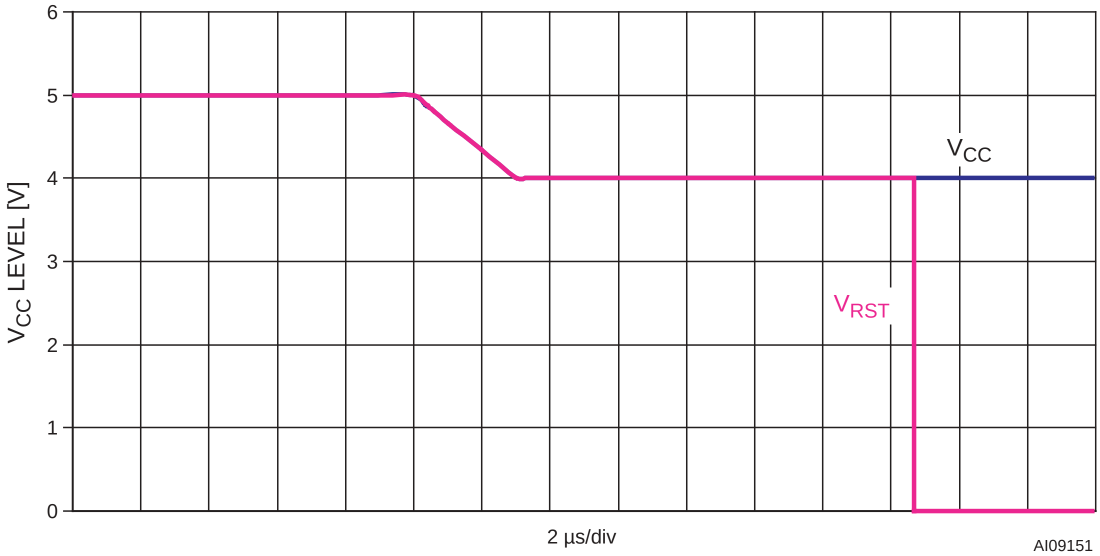


Figure 28. RESET Response Time (Assertion)

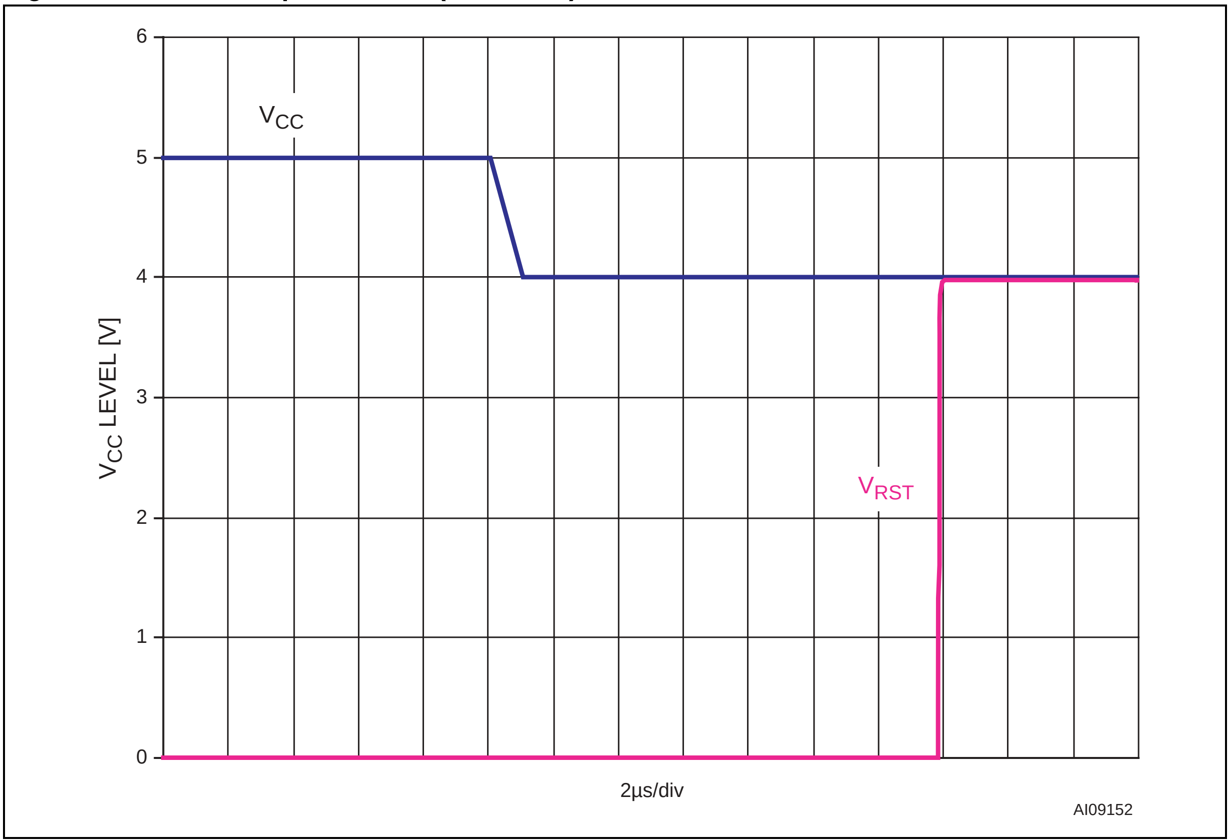


Figure 29. Power-fail Comparator Response Time (Assertion)

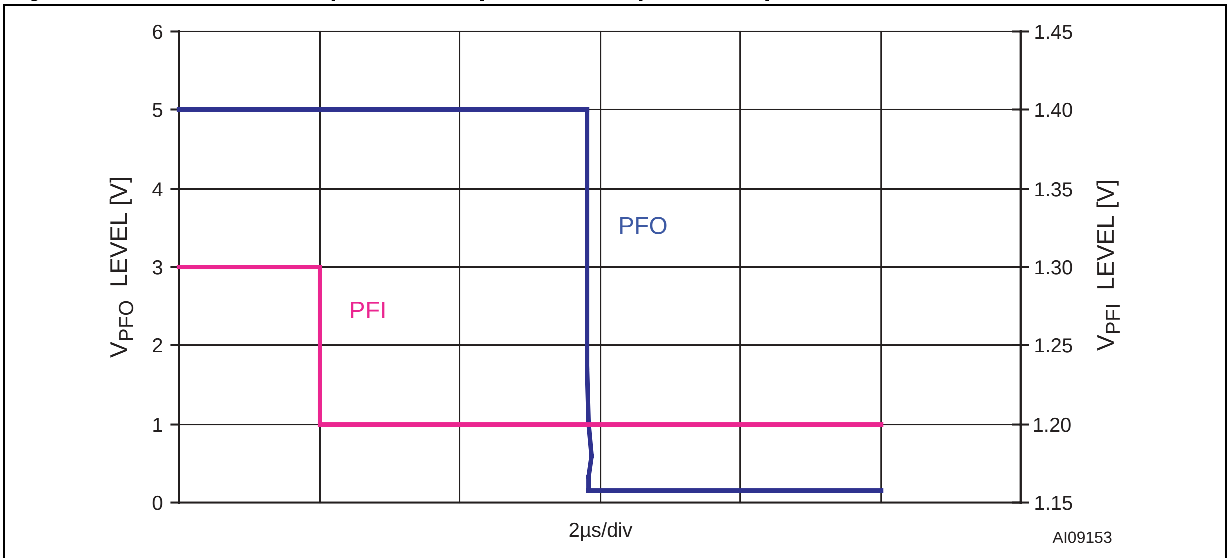


Figure 30. Power-fail Comparator Response Time (De-Assertion)

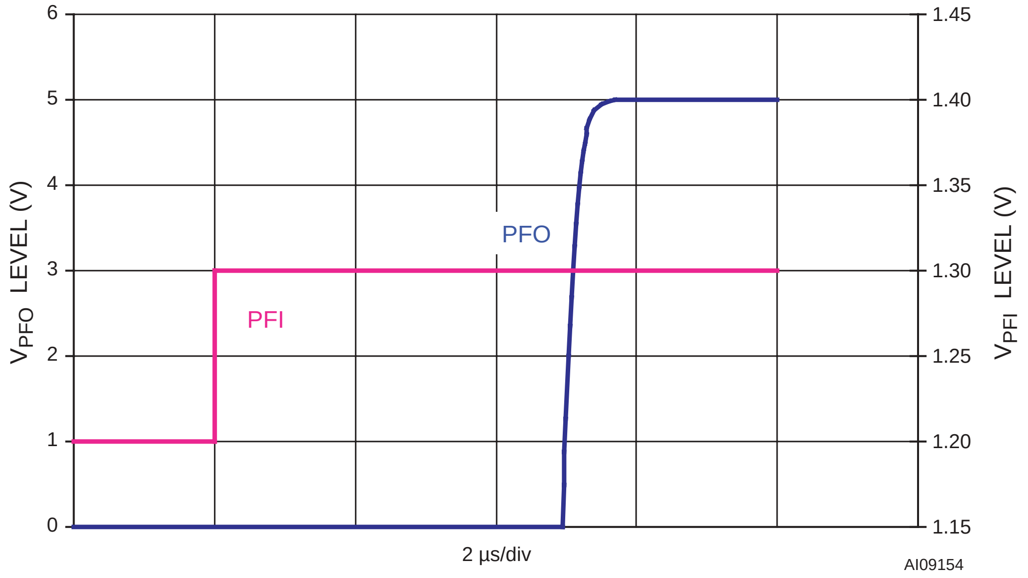


Figure 31. V_{CC} to Reset Propagation Delay vs. Temperature

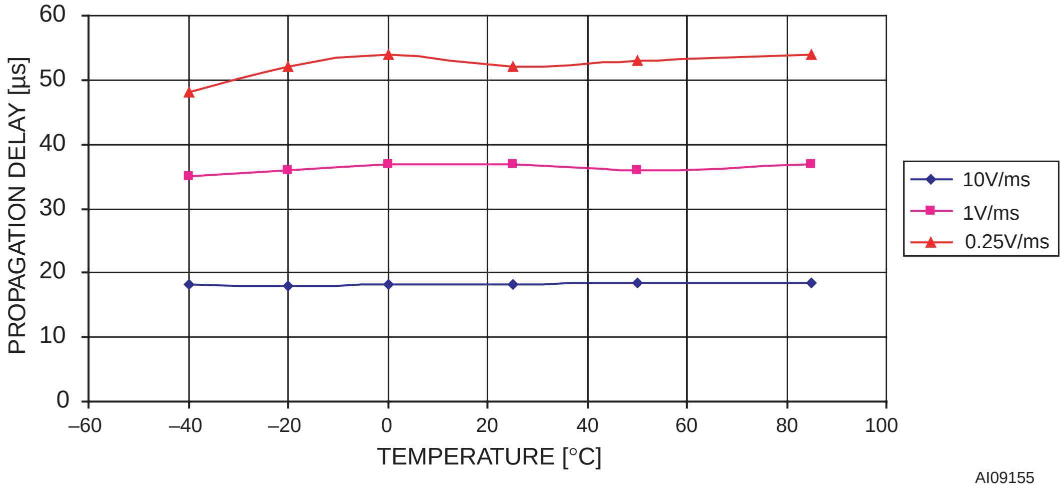


Figure 32. Maximum Transient Duration vs. Reset Threshold Overdrive

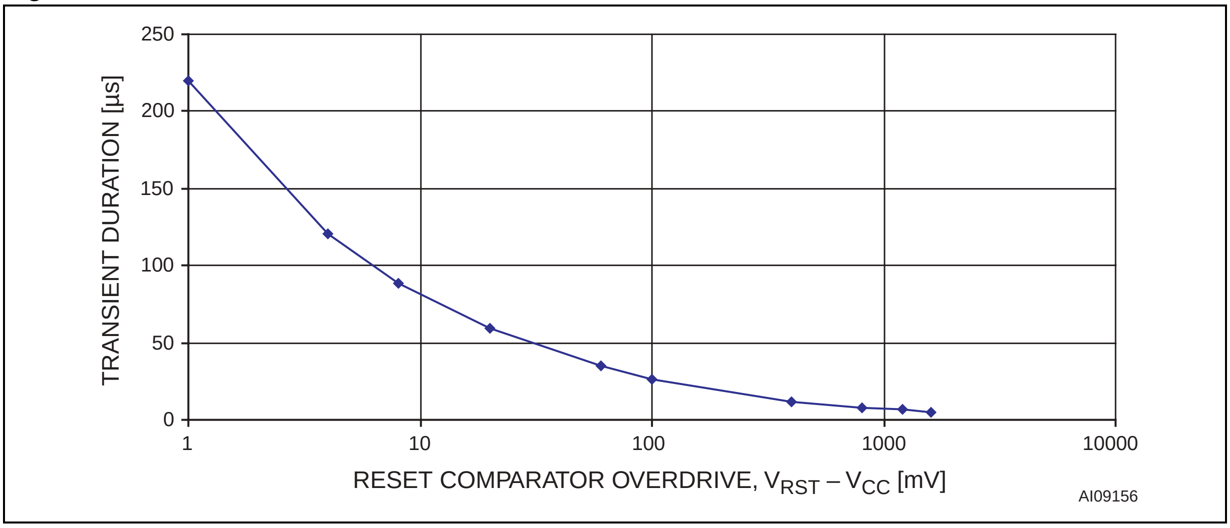
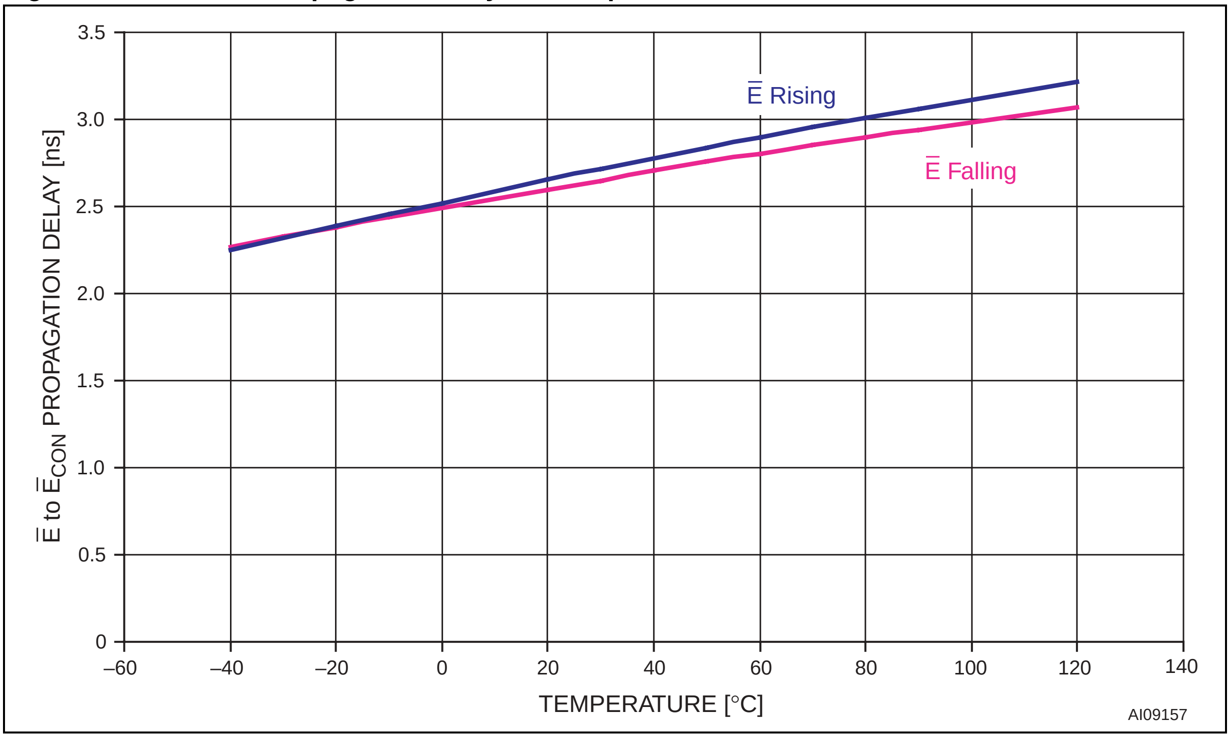


Figure 33. $\overline{E}$ to $\overline{E}_{CON}$ Propagation Delay vs. Temperature



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature (V_{CC} Off)	–55 to 150	°C
T_{SLD}(1)	Lead Solder Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltage	–0.3 to V_{CC} +0.3	V
V_{CC}/V_{BAT}	Supply Voltage	–0.3 to 6.0	V
I_O	Output Current	20	mA
P_D	Power Dissipation	320	mW

Note: 1. Reflow at peak temperature of 255°C to 260°C for < 30 seconds (total thermal budget not to exceed 180°C for between 90 to 150 seconds).

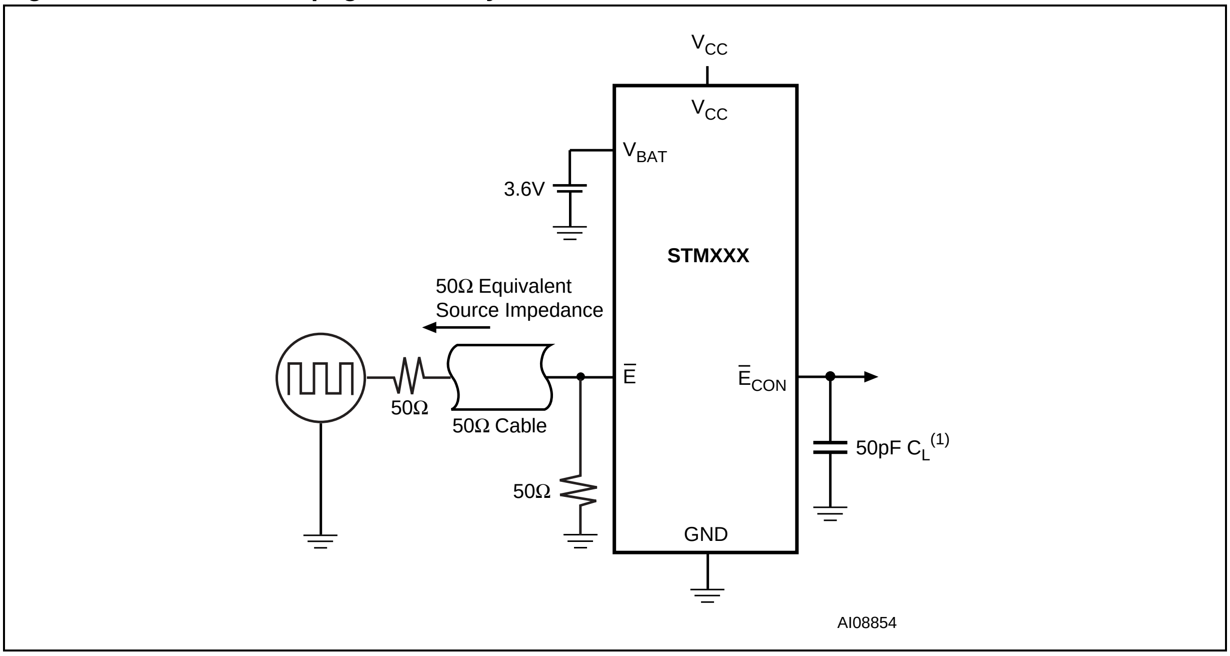
DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 6, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 6. Operating and AC Measurement Conditions

Parameter	STM690/704/795/ 802/804/805/806	Unit
V_{CC}/V_{BAT} Supply Voltage	1.0 to 5.5	V
Ambient Operating Temperature (T_A)	–40 to 85	°C
Input Rise and Fall Times	≤ 5	ns
Input Pulse Voltages	0.2 to 0.8V_{CC}	V
Input and Output Timing Ref. Voltages	0.3 to 0.7V_{CC}	V

Figure 34. $\overline{E}$ to $\overline{E}_{CON}$ Propagation Delay Test Circuit



Note: 1. C_L includes load capacitance and scope probe capacitance.

Figure 35. AC Testing Input/Output Waveforms

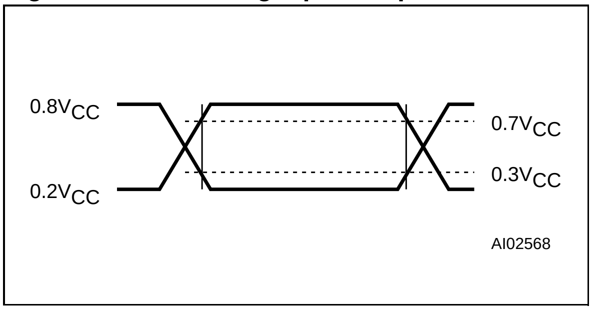
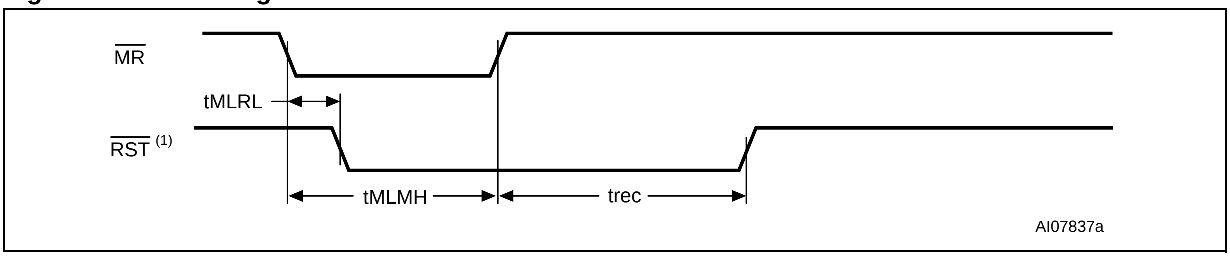


Figure 36. $\overline{MR}$ Timing Waveform



Note: 1. RST for STM805.

Figure 37. Watchdog Timing

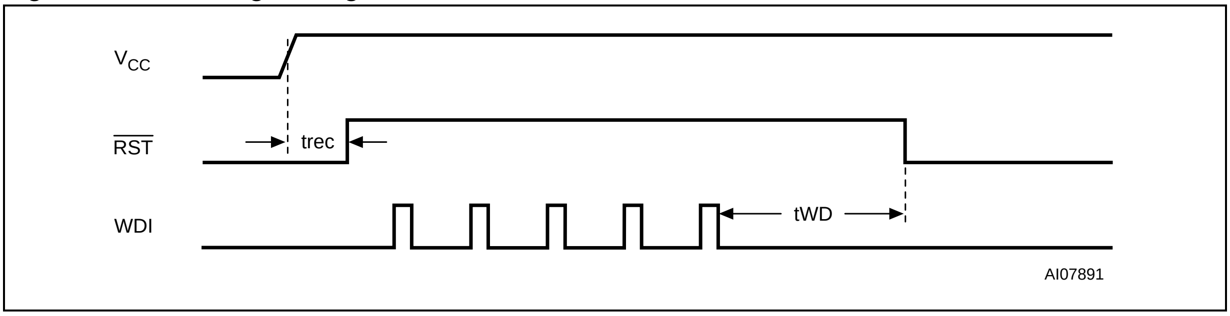


Table 7. DC and AC Characteristics

Sym	Alter-native	Description	Test Condition[1]	Min	Typ	Max	Unit
V_{CC}, V_{BAT}[2]		Operating Voltage	T_A = –40 to +85°C	1.1[3]		5.5	V
I_{CC}		V_{CC} Supply Current	Excluding I_{OUT} (V_{CC} < 5.5V)		40	60	µA
			Excluding I_{OUT} (V_{CC} < 3.6V)		35	50	µA
		V_{CC} Supply Current in Battery Back-up Mode	Excluding I_{OUT} (V_{BAT} = 2.3V, V_{CC} = 2.0V, $\overline{MR}$ = V_{CC})		25	35	µA
I_{BAT}[4]		V_{BAT} Supply Current in Battery Back-up Mode	Excluding I_{OUT} (V_{BAT} = 3.6V)		0.4	1.0	µA
V_{OUT1}		V_{OUT} Voltage (Active)	I_{OUT1} = 5mA[5]	V_{CC} – 0.03	V_{CC} – 0.015		V
			I_{OUT1} = 75mA	V_{CC} – 0.3	V_{CC} – 0.15		V
			I_{OUT1} = 250µA, V_{CC} > 2.5V[5]	V_{CC} – 0.0015	V_{CC} – 0.0006		V
V_{OUT2}		V_{OUT} Voltage (Battery Back-up)	I_{OUT2} = 250µA, V_{BAT} = 2.3V	V_{BAT} – 0.1	V_{BAT} – 0.034		V
			I_{OUT2} = 1mA, V_{BAT} = 2.3V		V_{BAT} – 0.14		V
V_{CC} to V_{OUT} On-resistance					3	4	Ω
V_{BAT} to V_{OUT} On-resistance					100		Ω
I_{LI}		Input Leakage Current ($\overline{MR}$)	STM704/806 only; $\overline{MR}$ = 0V; V_{CC} = 3V	20	75	350	µA
		Input Leakage Current (PFI)	0V = V_{IN} = V_{CC}	–25	2	+25	nA
		Input Leakage Current (WDI)	0V = V_{IN} = V_{CC}	–1		+1	µA
I_{LO}		Output Leakage Current	STM804/805/795; 0V = V_{IN} = V_{CC}[6]	–1		+1	µA
V_{IH}		Input High Voltage ($\overline{MR}$, WDI)	V_{RST} (max) < V_{CC} < 5.5V	0.7V_{CC}			V
V_{IL}		Input Low Voltage ($\overline{MR}$, WDI)	V_{RST} (max) < V_{CC} < 5.5V			0.3V_{CC}	V

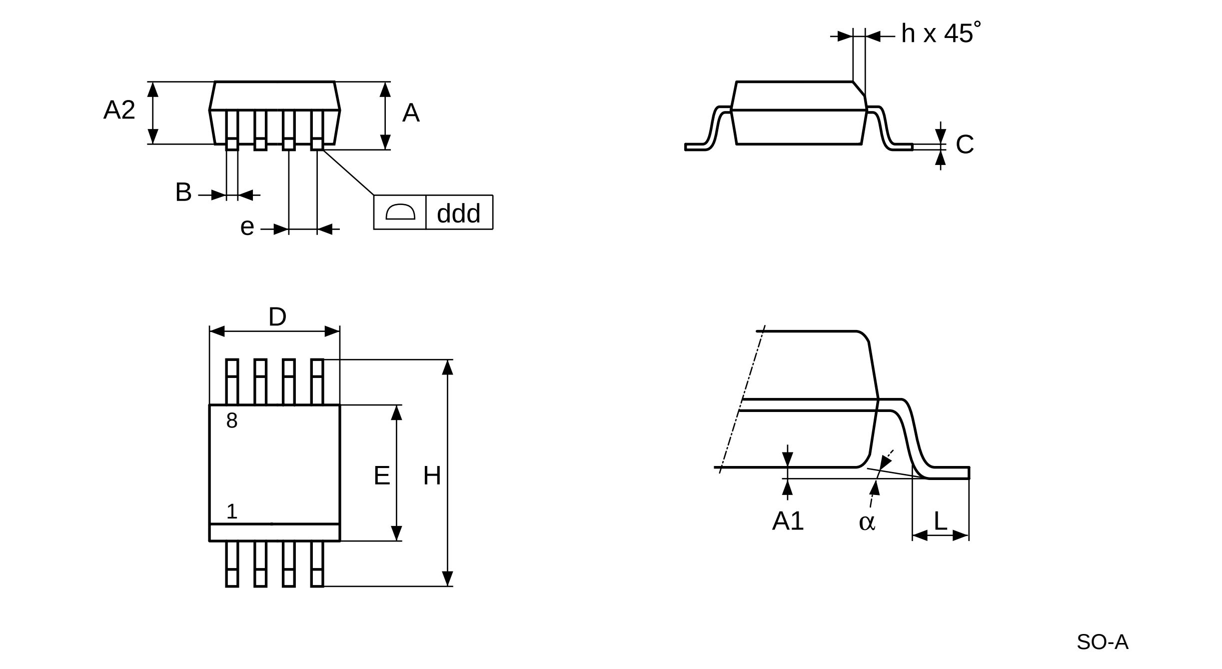
Sym	Alter-native	Description	Test Condition(1)		Min	Typ	Max	Unit
V_{OL}		Output Low Voltage ($\overline{PFO}$, $\overline{RST}$, RST, $\overline{Vccsw}$)	$V_{CC} = V_{RST}$ (max), $I_{SINK} = 3.2mA$				0.3	V
		Output Low Voltage ($\overline{E}_{CON}$)	$V_{CC} = V_{RST}$ (max), $I_{OUT} = 1.6mA$, $\overline{E} = 0V$				$0.2V_{CC}$	V
V_{OL}		Output Low Voltage ($\overline{RST}$)	$I_{OL} = 40mA$; $V_{CC} = 1.0V$; $V_{BAT} = 0V$; $T_A = 0°C$ to $85°C$				0.3	V
			$I_{OL} = 200\mu A$; $V_{CC} = 1.2V$; $V_{BAT} = 0V$				0.3	V
V_{OH}		Output High Voltage ($\overline{RST}$, RST)(7)	$I_{SOURCE} = 1mA$, $V_{CC} = V_{RST}$ (max)		2.4			V
		Output High Voltage ($\overline{E}_{CON}$)	$V_{CC} = V_{RST}$ (max), $I_{OUT} = 1.6mA$, $\overline{E} = V_{CC}$		$0.8V_{CC}$			V
		Output High Voltage ($\overline{PFO}$)	$I_{SOURCE} = 75\mu A$, $V_{CC} = V_{RST}$ (max)		$0.8V_{CC}$			V
V_{OHB}		V_{OH} Battery Back-up ($\overline{E}_{CON}$, $\overline{Vccsw}$, RST)	$I_{SOURCE} = 100\mu A$,		$0.8V_{BAT}$			V
Power-fail Comparator (NOT available on STM795)								
V_{PFI}		PFI Input Threshold	PFI Falling ($V_{CC} < 3.6V$)	STM802/ 804/806	1.212	1.237	1.262	V
				STM690/ 704/805	1.187	1.237	1.287	V
		PFI Hysteresis	PFI Rising ($V_{CC} < 3.6V$)			10	20	mV
t_{PFD}		PFI to $\overline{PFO}$ Propagation Delay				2		µs
I_{SC}		$\overline{PFO}$ Output Short to GND Current	$V_{CC} = 3.6V$, $\overline{PFO} = 0V$		0.1	0.75	2.0	mA
Battery Switchover								
V_{SO}		Battery Back-up Switchover Voltage (8,9)	Power-down	$V_{BAT} > V_{SW}$		V_{SW}		V
				$V_{BAT} < V_{SW}$		V_{BAT}		V
			Power-up	$V_{BAT} > V_{SW}$		V_{SW}		V
				$V_{BAT} < V_{SW}$		V_{BAT}		V
		V_{SW}				2.4		V
		Hysteresis				40		mV

Sym	Alter-native	Description	Test Condition(1)		Min	Typ	Max	Unit
Reset Thresholds								
V_{RST}(10)		Reset Threshold	STM690T/ 704T/795T/ 805T	V_{CC} Falling	3.00	3.075	3.15	V
				V_{CC} Rising	3.00	3.085	3.17	V
			STM802T/ 804T/806T	V_{CC} Falling	3.00	3.075	3.12	V
				V_{CC} Rising	3.00	3.085	3.14	V
			STM690S/ 704S/795S/ 805S	V_{CC} Falling	2.85	2.925	3.00	V
				V_{CC} Rising	2.85	2.935	3.02	V
			STM802S/ 804S/806S	V_{CC} Falling	2.88	2.925	3.00	V
				V_{CC} Rising	2.88	2.935	3.02	V
			STM690R/ 704R/795R/ 805R	V_{CC} Falling	2.55	2.625	2.70	V
				V_{CC} Rising	2.55	2.635	2.72	V
			STM802R/ 804R/806R	V_{CC} Falling	2.59	2.625	2.70	V
				V_{CC} Rising	2.59	2.635	2.72	V
t_{rec}		$\overline{RST}$ Pulse Width	V_{CC} < 3.6V		140	200	280	ms
Push-button Reset Input (STM704/806)								
t_{MLMH}	$t_{\overline{MR}}$	$\overline{MR}$ Pulse Width			100	20		ns
t_{MLRL}	$t_{\overline{MRD}}$	$\overline{MR}$ to $\overline{RST}$ Output Delay				60	500	ns
Watchdog Timer (NOT available on STM704/795/806)								
t_{WD}		Watchdog Timeout Period	V_{RST} (max) < V_{CC} < 3.6V		1.12	1.60	2.24	s
		WDI Pulse Width	V_{RST} (max) < V_{CC} < 3.6V		100	20		ns
Chip-Enable Gating (STM795 only)								
$\overline{E}$-to-$\overline{E}_{CON}$ Resistance			V_{CC} = V_{RST} (max)			46		Ω
$\overline{E}$-to-$\overline{E}_{CON}$ Propagation Delay			V_{CC} = V_{RST} (max)			2	7	ns
Reset-to-$\overline{E}_{CON}$ High Delay						10		µs
I_{SC}	$\overline{E}_{CON}$ Short Circuit Current		V_{CC} = 3.6V, Disable Mode, $\overline{E}_{CON}$ = 0V		0.1	0.75	2.0	mA

Note: 1. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; V_{CC} = V_{RST} (max) to 5.5V; and V_{BAT} = 2.8V (except where noted).
2. V_{CC} supply current, logic input leakage, Watchdog functionality, Push-button Reset functionality, PFI functionality, state of $\overline{RST}$ and RST tested at V_{BAT} = 3.6V, and V_{CC} = 5.5V. The state of $\overline{RST}$ or RST and $\overline{PFO}$ is tested at V_{CC} = V_{CC} (min). Either V_{CC} or V_{BAT} can go to 0V if the other is greater than 2.0V.
3. V_{CC} (min) = 1.0V for T_A = 0°C to +85°C.
4. Tested at V_{BAT} = 3.6V, V_{CC} = 3.5V and 0V.
5. Guaranteed by design.
6. The leakage current measured on the RST pin (STM804/805) or $\overline{RST}$ pin (STM795) is tested with the reset output not asserted (output high impedance).
7. Not valid for STM795/804/805 (open drain).
8. When V_{BAT} > V_{CC} > V_{SW}, V_{OUT} remains connected to V_{CC} until V_{CC} drops below V_{SW}.
9. When V_{SW} > V_{CC} > V_{BAT}, V_{OUT} remains connected to V_{CC} until V_{CC} drops below the battery voltage (V_{BAT}) – 75mV.
10. The reset threshold tolerance is wider for V_{CC} rising than for V_{CC} falling due to the 10mV (typ) hysteresis, which prevents internal oscillation.

PACKAGE MECHANICAL

Figure 38. SO8 – 8-lead Plastic Small Outline, 150 mils body width, Package Mech. Drawing

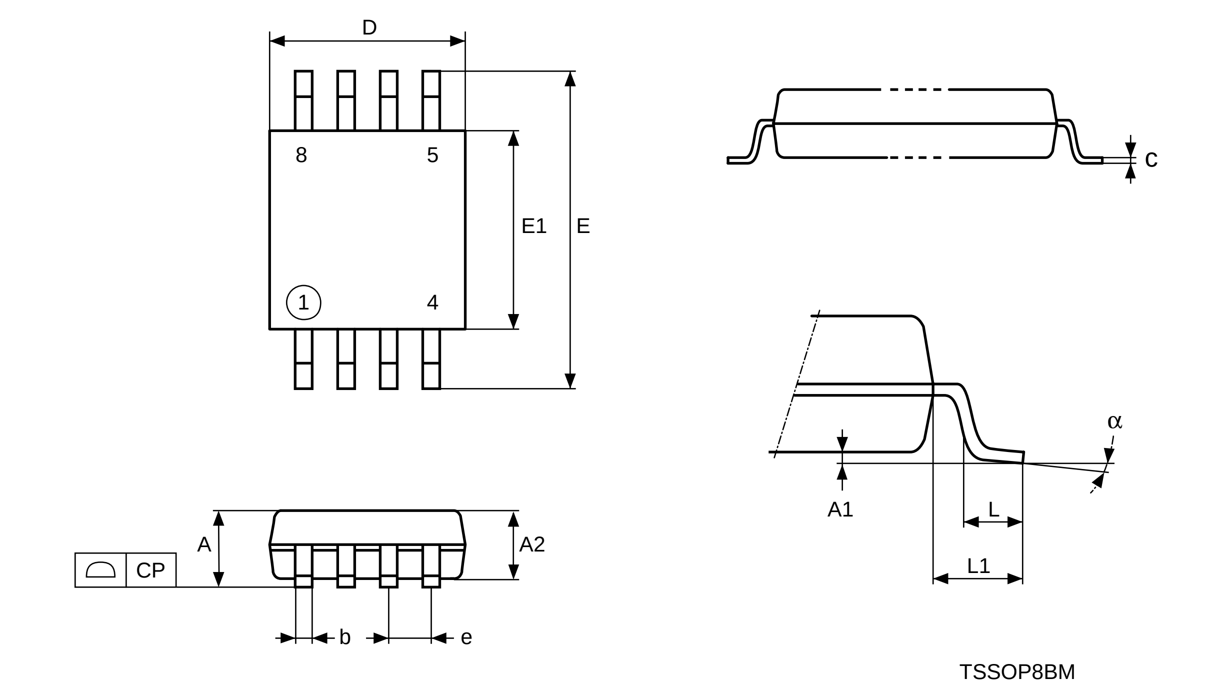


Note: Drawing is not to scale.

Table 8. SO8 – 8-lead Plastic Small Outline, 150 mils body width, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	–	1.35	1.75	–	0.053	0.069
A1	–	0.10	0.25	–	0.004	0.010
B	–	0.33	0.51	–	0.013	0.020
C	–	0.19	0.25	–	0.007	0.010
D	–	4.80	5.00	–	0.189	0.197
ddd	–	–	0.10	–	–	0.004
E	–	3.80	4.00	–	0.150	0.157
e	1.27	–	–	0.050	–	–
H	–	5.80	6.20	–	0.228	0.244
h	–	0.25	0.50	–	0.010	0.020
L	–	0.40	0.90	–	0.016	0.035
α	–	0°	8°	–	0°	8°
N	8			8		

Figure 39. TSSOP8 – 8-lead, Thin Shrink Small Outline, 3x3mm body size, Outline



Note: Drawing is not to scale.

Table 9. TSSOP8 – 8-lead, Thin Shrink Small Outline, 3x3mm body size, Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.10	–	–	0.043
A1	–	0.05	0.15	–	0.002	0.006
A2	0.85	0.75	0.95	0.034	0.030	0.037
b	–	0.25	0.40	–	0.010	0.016
c	–	0.13	0.23	–	0.005	0.009
CP	–	–	0.10	–	–	0.004
D	3.00	2.90	3.10	0.118	0.114	0.122
e	0.65	–	–	0.026	–	–
E	4.90	4.65	5.15	0.193	0.183	0.203
E1	3.00	2.90	3.10	0.118	0.114	0.122
L	0.55	0.40	0.70	0.022	0.016	0.030
L1	0.95	–	–	0.037	–	–
α	–	0°	6°	–	0°	6°
N	8			8		

PART NUMBERING

Table 10. Ordering Information Scheme

Example:	STMXXX	T	M	6	E

Device Type

STMXXX

Reset Threshold Voltage

T = STM690/704/795/805 = V_{RST} = 3.00V to 3.15V

STM802/804/806 = V_{RST} = 3.00V to 3.12V

S = STM690/704/795/805 = V_{RST} = 2.85V to 3.00V

STM802/804/806 = V_{RST} = 2.88V to 3.00V

R = STM690/704/795/805 = V_{RST} = 2.55V to 2.70V

STM802/804/806 = V_{RST} = 2.59V to 2.70V

Package

M = SO8

DS(1) = TSSOP8

Temperature Range

6 = –40 to 85°C

Shipping Method

E = Tubes (Pb-Free - ECOPACK®)

F = Tape & Reel (Pb-Free - ECOPACK®)

Note: 1. Contact local ST sales office for availability.

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

Table 11. Marking Description

Part Number	Reset Threshold	Package	Topside Marking
STM690T	3.075	SO8	690T
		TSSOP8	
STM690S	2.925	SO8	690S
		TSSOP8	
STM690R	2.625	SO8	690R
		TSSOP8	
STM704T	3.075	SO8	704T
		TSSOP8	
STM704S	2.925	SO8	704S
		TSSOP8	
STM704R	2.625	SO8	704R
		TSSOP8	
STM795T	3.075	SO8	795T
		TSSOP8	
STM795S	2.925	SO8	795S
		TSSOP8	
STM795R	2.625	SO8	795R
		TSSOP8	
STM802T	3.075	SO8	802T
		TSSOP8	
STM802S	2.925	SO8	802S
		TSSOP8	
STM802R	2.625	SO8	802R
		TSSOP8	
STM804T	3.075	SO8	804T
		TSSOP8	
STM804S	2.925	SO8	804S
		TSSOP8	
STM804R	2.625	SO8	804R
		TSSOP8	
STM805T	3.075	SO8	805T
		TSSOP8	
STM805S	2.925	SO8	805S
		TSSOP8	
STM805R	2.625	SO8	805R
		TSSOP8	
STM806T	3.075	SO8	806T
		TSSOP8	
STM806S	2.925	SO8	806S
		TSSOP8	
STM806R	2.625	SO8	806R
		TSSOP8	

REVISION HISTORY

Table 12. Document Revision History

Date	Version	Revision Details
October 31, 2003	1.0	First Issue
22-Dec-03	2.0	Reformatted; update characteristics (Figure 1, 3, 4, 11, 13, 14, 36; Table 1, 3, 4, 7, 9, 11)
16-Jan-04	2.1	Add Typical Operating Characteristics (Figure 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33)
07-Apr-04	2.2	Update characteristics (Figure 13, 25, 26, 27, 28, 31; Table 1, 3, 7)
25-May-04	3.0	Update characteristics (Table 3, 7)
02-Jul-04	4.0	Update package availability, pin description; promote document (Figure 1, 14; Table 3, 10)