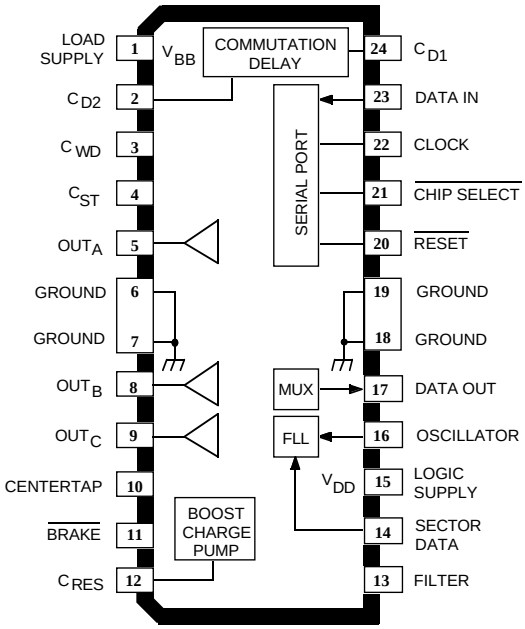
8902–A

3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER WITH BACK-EMF SENSING



Dwg. PP-040B

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Load Supply Voltage, V_{BB} . . . . . **14 V**
Output Current, I_{OUT} . . . . . **±1.25 A**
Logic Supply Voltage, V_{DD} . . . . . **6.0 V**
Logic Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Package Power Dissipation, P_D **See Graph**
Operating Temperature Range,
T_A . . . . . **0°C to +70°C**
Junction Temperature, T_J . . . . . **+150°C†**
Storage Temperature Range,
T_S . . . . . **-55°C to +150°C**

† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.

The A8902CLBA is a three-phase brushless dc motor controller/driver for use in 5 V or 12 V hard-disk drives. The three half-bridge outputs are low on-resistance n-channel DMOS devices capable of driving up to 1.25 A. The A8902CLBA provides complete, reliable, self-contained back-EMF sensing motor startup and running algorithms. A programmable digital frequency-locked loop speed control circuit together with the linear current control circuitry provides precise motor speed regulation.

A serial port allows the user to program various features and modes of operation, such as the speed control parameters, startup current limit, sleep mode, diagnostic modes, and others.

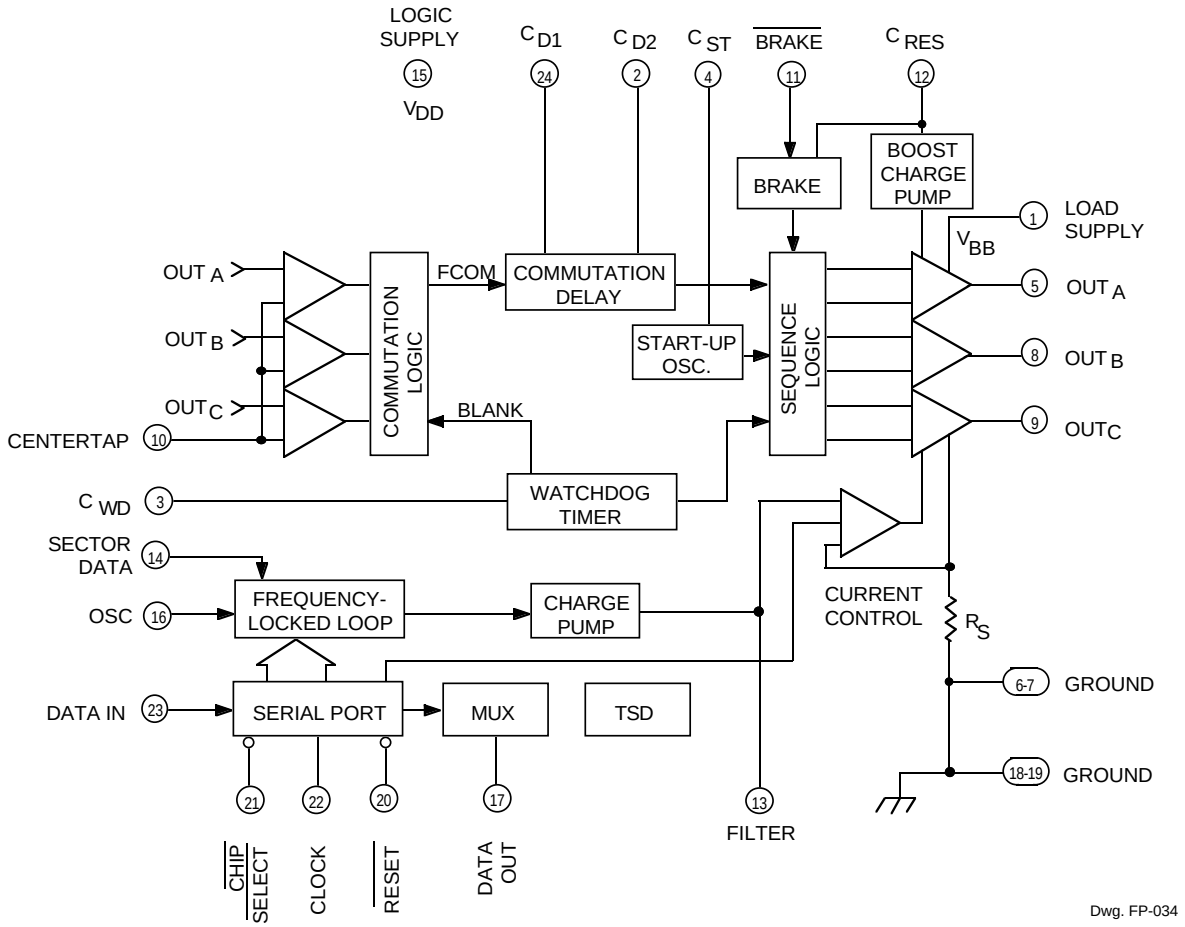
The A8902CLBA is fabricated in Allegro's BCD (Bipolar CMOS DMOS) process, an advanced mixed-signal technology that combines bipolar, analog and digital CMOS, and DMOS power devices. The A8902CLBA is provided in a 24-lead wide-body SOIC batwing package. It provides for the smallest possible construction in surface-mount applications.

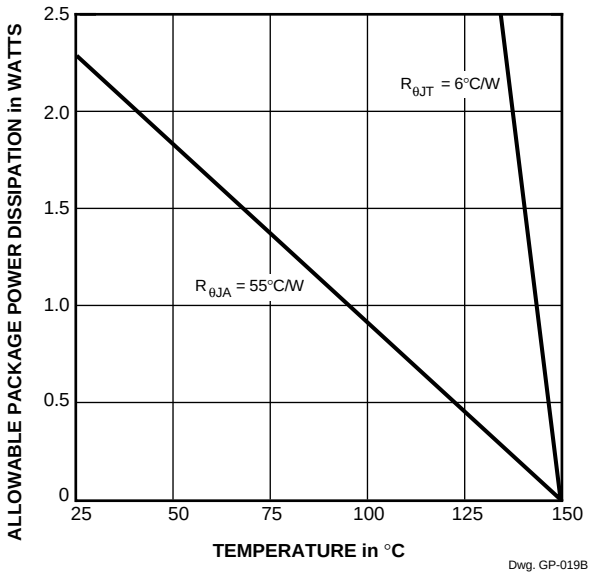
FEATURES

- DMOS Outputs
- Low $r_{DS(on)}$
- Startup Commutation Circuitry
- Back-EMF Commutation Circuitry
- Serial Port Interface
- Frequency-Locked Loop Speed Control
- Sector Data Tachometer Signal Input
- Programmable Start-Up Current
- Diagnostics Mode
- Sleep Mode
- Linear Current Control
- Internal Current Sensing
- Dynamic Braking Through Serial Port
- Power-Down Dynamic Braking
- System Diagnostics Data Out
- Data Out Ported in Real Time
- Internal Thermal Shutdown Circuitry

Always order by complete part number, e.g., **A8902CLBA**.

FUNCTIONAL BLOCK DIAGRAM





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ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5.0 V

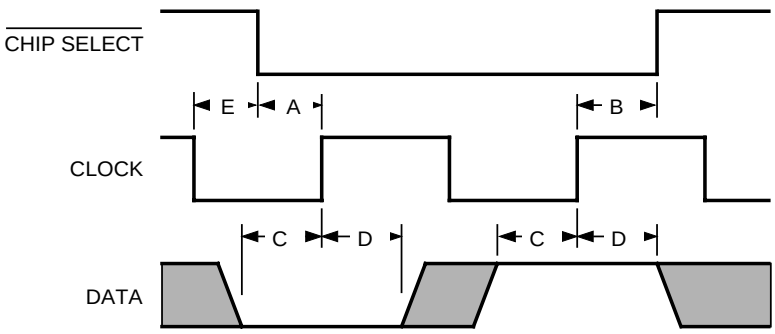
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Logic Supply Voltage	V_{DD}	Operating	4.5	5.0	5.5	V
Logic Supply Current	I_{DD}	Operating	—	7.5	10	mA
		Sleep Mode	—	250	500	µA
Load Supply Voltage	V_{BB}	Operating	4.0	—	14	V
Thermal Shutdown	T_J		—	165	—	°C
Thermal Shutdown Hysteresis	ΔT_J		—	20	—	°C
Output Drivers						
Output Leakage Current	I_{DSX}	V_{BB} = 14 V, V_{OUT} = 14 V	—	1.0	300	µA
		V_{BB} = 14 V, V_{OUT} = 0 V	—	-1.0	-300	µA
Total Output ON Resistance (Source + Sink + R_S)	$r_{DS(on)}$	I_{OUT} = 600 mA	—	1.0	1.4	Ω
Output Sustaining Voltage	$V_{DS(sus)}$	V_{BB} = 14 V, I_{OUT} = I_{OUT}(MAX), L = 3 mH	14	—	—	V
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	—	1.25	1.5	V
Control Logic						
Logic Input Voltage	$V_{IN(0)}$	SECTOR DATA, RESET, CLK,	-0.3	—	1.5	V
	$V_{IN(1)}$	CHIP SELECT, OSC	3.5	—	5.3	V
Logic Input Current	$I_{IN(0)}$	V_{IN} = 0 V	—	—	-0.5	µA
	$I_{IN(1)}$	V_{IN} = 5.0 V	—	—	1.0	µA
DATA Output Voltage	$V_{OUT(0)}$	I_{OUT} = 500 µA	—	—	1.5	V
	$V_{OUT(1)}$	I_{OUT} = -500 µA	3.5	—	—	V
C_{ST} Current	I_{CST}	Charging	-9.0	-10	-11	µA
		Discharging	—	500	—	µA
C_{ST} Threshold	V_{CSTH}		2.25	2.5	2.75	V
	V_{CSTL}		0.85	1.0	1.15	V
Filter Current	I_{FILTER}	Charging	-9.0	-10	-11	µA
		Discharging	9.0	10	11	µA
		Leakage, V_{FILTER} = 2.5 V	—	—	5.0	nA
Filter Threshold	$V_{FILTERTH}$		1.57	1.85	2.13	V
C_D Current (C_{D1} or C_{D2})	I_{CD}	Charging	-18	-20	-22	µA
		Discharging	32	40	48	µA
C_D Current Matching	—	$I_{CD(DISCHRG)}/I_{CD(CHRG)}$	1.8	2.0	2.2	—
C_D Threshold	V_{CDTH}		2.25	2.5	2.75	V

Continued next page …

ELECTRICAL CHARACTERISTICS continued

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
C_{WD} Current	I_{CWD}	Charging	-9.0	-10	-11	µA
C_{WD} Threshold Voltage	V_{TL}		0.22	0.25	0.28	V
	V_{TH}		2.25	2.5	2.75	V
Max. FLL Oscillator Frequency	f_{OSC}	V_{DD} = 5.0 V, T_A = 25°C	12	—	—	MHz
I_{OUT}(MAX)	—	D3 = 0, D4 = 0	1.0	1.2	1.4	A
		D3 = 0, D4 = 1	0.9	1.0	1.1	A
		D3 = 1, D4 = 0	0.5	0.6	0.7	A
		D3 = 1, D4 = 1	—	250	—	mA
BRAKE Threshold	V_{BRK}		1.5	1.75	2.0	V
BRAKE Hysteresis Current	I_{BRKL}	V_{BRK} = 750 mV	—	20	—	µA
Transconductance Gain	g_m		0.42	0.50	0.58	A/V
Centertap Resistors	R_{CT}		5.0	10	13	kΩ
Back-EMF Hysteresis	—	V_{BEMF} - V_{CTAP} at	5.0	20	37	mV
		FCOM Transition	-5.0	-20	-37	mV

SERIAL PORT TIMING CONDITIONS



Dwg. WP-019

A. Minimum CHIP SELECT setup time before CLOCK rising edge ..... **100 ns**

B. Minimum CHIP SELECT hold time after CLOCK rising edge ..... **150 ns**

C. Minimum DATA setup time before CLOCK rising edge ..... **150 ns**

D. Minimum DATA hold time after CLOCK rising edge ..... **150 ns**

E. Minimum CLOCK low time before CHIP SELECT ..... **50 ns**

F. Maximum CLOCK frequency ..... **3.3 MHz**

TERMINAL FUNCTIONS

Term.	Terminal Name	Function
1	LOAD SUPPLY	V_{BB}; the 5 V or 12 V motor supply.
2	C_{D2}	One of two capacitors used to generate the ideal commutation points from the back-EMF zero crossing points.
3	C_{WD}	Timing capacitor used by the watchdog circuit to disable the back-EMF comparators during commutation transients, and to detect incorrect motor position.
4	C_{ST}	Startup oscillator timing capacitor.
5	OUT_A	Power amplifier A output to motor.
6-7	GROUND	Power and logic ground and thermal heat sink.
8	OUT_B	Power amplifier B output to motor.
9	OUT_C	Power amplifier C output to motor.
10	CENTERTAP	Motor centertap connection for back-EMF detection circuitry.
11	$\overline{\text{BRAKE}}$	Active low turns ON all three sink drivers shorting the motor windings to ground. External capacitor and resistor at BRAKE provide brake delay. The brake function can also be controlled via the serial port.
12	C_{RES}	External reservoir capacitor used to hold charge to drive the source drivers' gates. Also provides power for brake circuit.
13	FILTER	Analog voltage input to control motor current. Also, compensation node for internal speed control loop.
14	SECTOR DATA	External tachometer input. Can use sector or index pulses from disk to provide precise motor speed feedback to internal frequency-locked loop.
15	LOGIC SUPPLY	V_{DD}; the 5 V logic supply.
16	OSCILLATOR	Clock input for the speed reference counter. Typical max. frequency is 10 MHz.
17	DATA OUT	Thermal shutdown indicator, FCOM, TACH, or SYNC signals available in real time, controlled by 2-bit multiplexer in serial port.
18-19	GROUND	Power and logic ground and thermal heat sink.
20	$\overline{\text{RESET}}$	When pulled low forces the chip into sleep mode; clears all serial port bits.
21	$\overline{\text{CHIP SELECT}}$	Strobe input (active low) for data word.
22	CLOCK	Clock input for serial port.
23	DATA IN	Sequential data input for the serial port.
24	C_{D1}	One of two capacitors used to generate the ideal commutation points from the back-EMF zero crossing points.

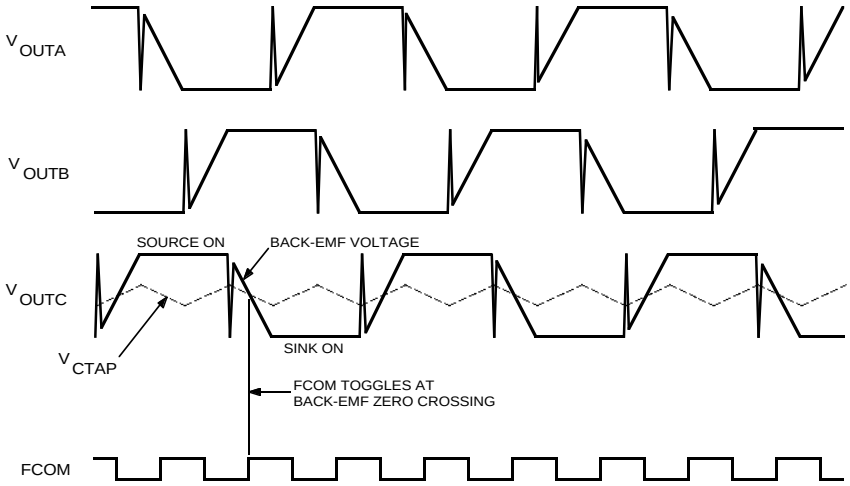
FUNCTIONAL DESCRIPTION

Power Outputs. The power outputs of the A8902CLBA are n-channel DMOS transistors with a total source plus sink $r_{DS(on)}$ of typically 1 Ω. Internal charge pump boost circuitry provides voltage above supply for driving the high-side DMOS gates. Intrinsic ground clamp and flyback diodes provide protection when switching inductive loads and may be used to rectify motor back-EMF in power-down conditions. An external Schottky power diode or pass FET is required in series with the load supply to allow motor back-EMF rectification in power down conditions.

Back-EMF Sensing Motor Startup and Running Algorithm. The A8902CLBA provides a complete self-contained back-EMF sensing startup and running commutation scheme. The three half-bridge outputs are controlled by a state machine. There are six possible combinations. In each state, one output is high (sourcing current), one low (sinking current), and one is OFF (high impedance or 'Z'). Motor back EMF is sensed at the OFF output. The truth table for the output drivers sequencing is:

Sequencer State	OUT_A	OUT_B	OUT_C
1	High	Low	Z
2	Z	Low	High
3	Low	Z	High
4	Low	High	Z
5	Z	High	Low
6	High	Z	Low

At startup, the outputs are enabled in one of the sequencer states shown. The back EMF is examined at the OFF output by comparing the output voltage to the motor centertap voltage at CENTERTAP. The motor will then either step forward, step backward, or remain stationary (if in a null-torque position). If the motor moves, the back-EMF detection circuit waits for the correct polarity back-EMF zero crossing (output crossing through centertap). True back-EMF zero crossings are used by the adaptive commutation delay circuit to advance the state sequencer (commutate) at the proper time to synchronously run the motor. Back-EMF zero crossings are indicated by FCOM, an internal signal that toggles at every zero crossing. FCOM is available at the DATA OUT terminal via the programmable data out multiplexer.



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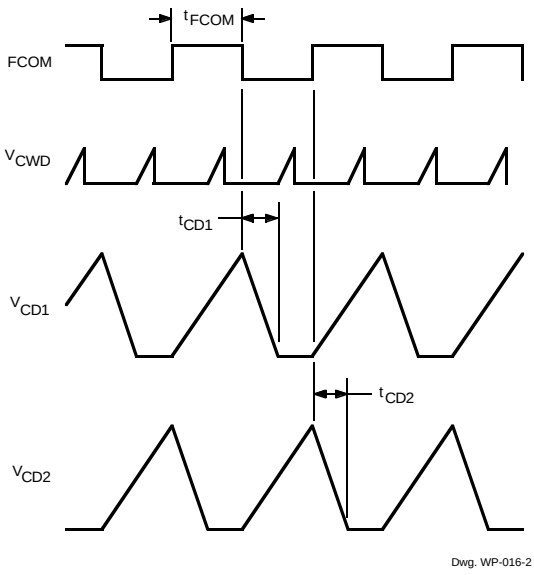
Startup Oscillator. If the motor does not move at the initial startup state, then it is in a null-torque position. In this case, the outputs are commutated automatically by the startup oscillator after a period set by the external capacitor at C_{ST} where

$$t_{CST} = \frac{4(V_{CSTH} - V_{CSTL}) \times C_{ST}}{I_{ST(charge)} + I_{ST(discharge)}}$$

In the next state, the motor will move, back EMF will be detected, and the motor will accelerate synchronously. Once normal synchronous back-EMF commutation occurs, the startup oscillator is defeated by pulses of pulldown current at C_{ST} at each commutation, which prevents C_{ST} from reaching its upper threshold and thus completing a cycle and commutating.

Adaptive Commutation Delay. The adaptive commutation delay circuit uses the back-EMF zero-crossing indicator signal (FCOM) to determine an optimal commutation time for efficient synchronous operation. This circuit commutates the outputs, delayed from the last zero crossing, using two external timing capacitors, C_{D1} and C_{D2},



to measure the time between crossings.

where $t_{CD} = t_{FCOM} \times \frac{I_{CD(charge)}}{I_{CD(discharge)}}$

C_{D1} charges up with a fixed current from its 2.5 V reference while FCOM is high. When FCOM goes low at the next zero crossing, C_{D1} is discharged at approximately twice the charging current. When CD_1 reaches the CD threshold, a commutation occurs. C_{D2} operates similarly except on the opposite phase of FCOM . Thus the commutations occur approximately halfway between zero crossings. The actual delay is slightly less than halfway to compensate for electrical delays in the motor, which improves efficiency.

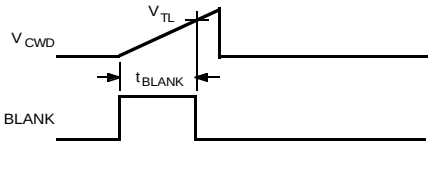
Blanking and Watchdog Timing Functions. The blanking and watchdog timing functions are derived from one timing capacitor, C_{WD}.

where $t_{BLANK} = \frac{V_{TL} \times C_{WD}}{I_{CWD}}$

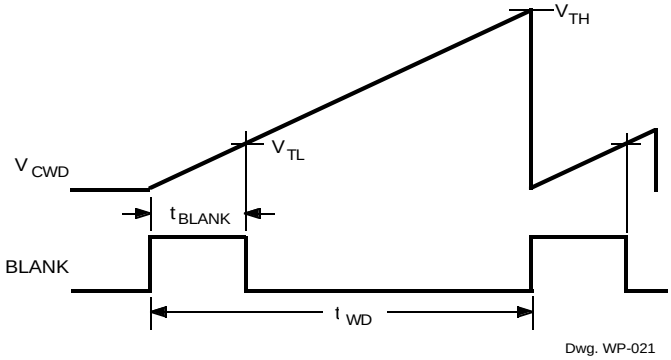
and $t_{WD} = \frac{V_{TH} \times C_{WD}}{I_{CWD}}$

The CWD capacitor begins charging at each commutation, initiating the BLANK signal. BLANK is an internal signal that inhibits the back-EMF comparators during the commutation transients, preventing errors due to inductive recovery and voltage settling transients.

The watchdog timing function allows time to detect correct motor position by checking the back-EMF polarity after each commutation. If the correct polarity is not observed between t_{BLANK} and t_{WD}, then the watchdog timer commutates the outputs to the next state to synchronize the motor. This function is useful in preventing excessive reverse rotation, and helps in resynchronizing (or starting) with a moving spindle.

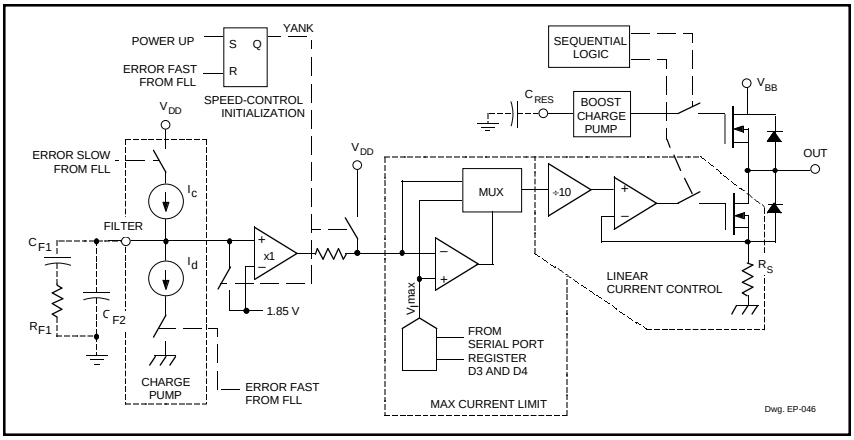


NORMAL COMMUTATION



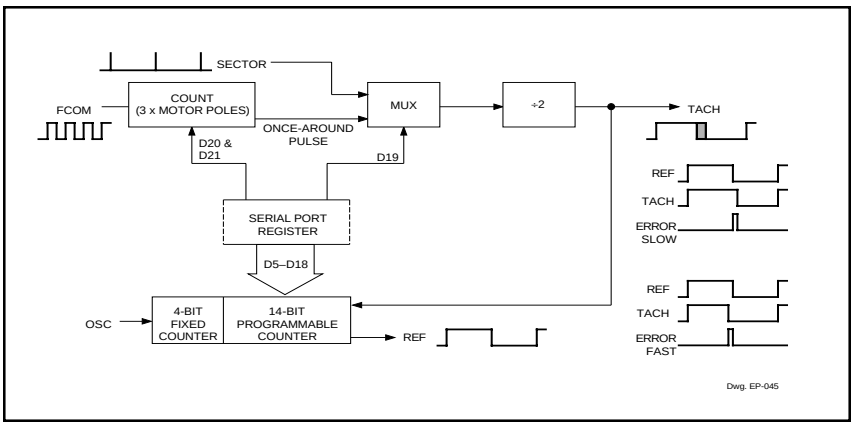
WATCHDOG-TRIGGERED COMMUTATION

Current Control. The A8902CLBA provides linear current control via the FILTER terminal, an analog voltage input. Maximum current limit is also provided, and is controlled in four steps via the serial port. Output current is sensed via an internal sense resistor (R_S). The voltage across the sense resistor is compared to one-tenth the voltage at the FILTER terminal less the filter threshold voltage, or to the maximum current limit reference, whichever is lower. This transconductance function is $I_{OUT} = (V_{FILTER} - V_{FILTERTH}) / 10R_S$, where R_S is nominally 0.2 Ω and $V_{FILTERTH}$ is approximately 1.85 V.



Speed Control. The A8902CLBA includes a frequency-locked loop speed control system. This system monitors motor speed via internal or external digital tachometer signals, generates a precision speed reference, determines the digital speed error, and corrects the motor current via an internal charge pump and external filtering components on the FILTER terminal.

A once per revolution TACH signal can be generated by counting cycles of FCOM (the number of motor poles must be selected via the serial port). TACH is then a jitter-free signal that toggles once per motor revolution. The rising edge of TACH triggers REF, a precision speed reference derived by a programmable counter. The duration of REF is set by programming the counter to count the desired number of OSC cycles



$$\text{desired total count} = \frac{60 \times f_{OSC}}{\text{desired motor speed (rpm)}}$$

where the total count (number of oscillator cycles) is equal to the sum of the selected (programmed low) count numbers corresponding to bits D5 through D18.

The speed error is detected as the difference in falling edges of TACH and REF. The speed error signals control the error-correcting charge pump on the FILTER terminal, which drive the external loop compensation components to correct the motor current.

Sector Mode. An external tachometer signal, such as sector or index pulses, may be used to create the TACH signal, rather than the internally derived once around. To use this mode, the signal is input to the SECTOR terminal, and the sector mode must be enabled via the serial port. When Switching from the once-around mode to sector mode, it is important to monitor the SYNC signal on DATA OUT, and switch modes only when SYNC is low. This ensures making the transition without disturbing the speed control loop. The speed reference counter should be reprogrammed at the same time.

Speed Loop Initialization (YANK). To improve the acquire time of the speed control loop, there is an automatic feature controlled by an internal YANK signal. The motor is started at the maximized programmed current by bypassing the FILTER terminal. The FILTER terminal is clamped to an internal reference (the filter threshold voltage), initializing it near the closed loop operating point. YANK is enabled at startup and stays high until the desired speed is reached. Once the first error-fast occurs, indicating the motor crossed through the desired speed, YANK goes low. This releases the clamp on the FILTER terminal and current control is returned to FILTER. This feature optimizes speed acquire and minimizes settling. The Current Control Block Diagram illustrates the YANK signal and its effects.

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Serial Port. The serial port functions to write various operational and diagnostic modes to the A8902CLBA. The serial port DATA IN is enabled/disabled by the CHIP SELECT terminal. When CHIP SELECT is high the serial port is disabled and the chip is not affected by changes in data at the DATA IN or CLOCK terminals.

To write data to the serial port, the CLOCK terminal should be low prior to the CHIP SELECT terminal going low. Once CHIP SELECT goes low, information on the DATA IN terminal is read into the shift register on the positive-going transition of the CLOCK. There are 24 bits in the serial input port.

Data written into the serial port is latched and becomes active upon the low-to-high transition of the CHIP SELECT terminal at the end of the write cycle. D0 will be the last bit written to the serial port.

SERIAL PORT BIT DEFINITIONS

D0- Sleep/Run Mode; LOW = Sleep, HIGH = Run
This bit allows the device to be powered down when not in use.

D1- Step Mode; LOW = Normal Operation, HIGH = Step Only
When in the step-only mode the back-EMF commutation circuitry is disabled and the power outputs are commutated by the start-up oscillator. This mode is intended for device and system testing.

D2- Brake; LOW = Run, HIGH = Brake.

D3 and D4 - These two bits set the output current limit:

D3	D4	Current Limit
0	0	1.2 A
0	1	1 A
1	0	600 mA
1	1	250 mA

D5 thru D18-This 14-bit word (active low) programs the $_{REF}$ time to set desired motor speed.

Bit Number	Count Number
D5	16
D6	32
D7	64
D8	128
D9	256
D10	512
D11	1 024
D12	2 048
D13	4 096
D14	8 192
D15	16 384
D16	32 768
D17	65 536
D18	131 072

D19-Speed-control mode switch;
LOW = internal once-around speed signal,
HIGH = external sector data.

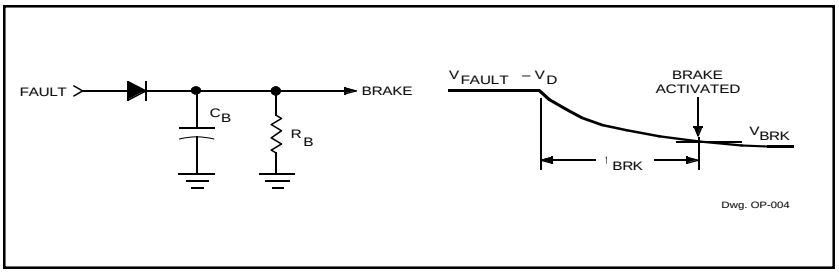
D20 and D21-These bits program the number of motor poles for the once-around $_{FCOM}$ counter:

D20	D21	Motor Poles
0	0	8
0	1	–
1	0	16
1	1	12

D22 and D23-Controls the multiplexer for DATA OUT:

D22	D23	DATA OUT
0	0	TACH (once around or sector)
0	1	Thermal Shutdown
1	0	SYNC
1	1	FCOM

Reset. The RESET terminal when pulled low clears all serial port bits, including the D0 latch, which puts the A8902CLBA in the sleep mode.



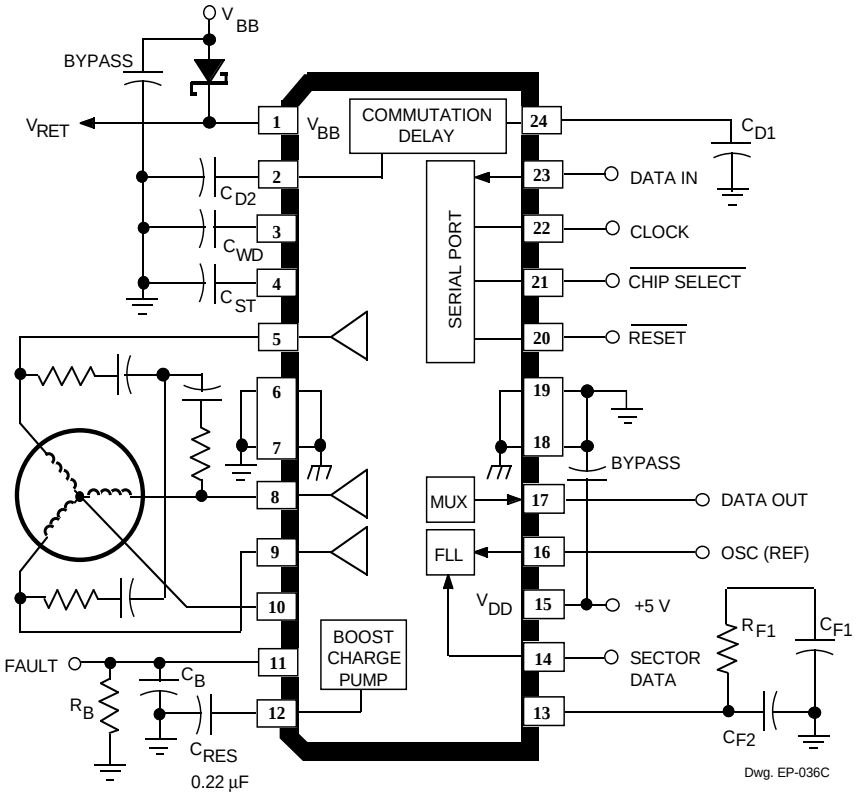
Braking. A dynamic braking feature of the A8902CLBA shorts the three motor windings to ground. This is accomplished by turning the three source drivers OFF and the three sink drivers ON. Activation of the brake can be implemented through the BRAKE input or through the D2 bit in the serial port. The supply voltage for the brake circuitry is the C_{RES} voltage, allowing the brake function to remain active after power failure. Power-down braking with delay can be implemented by using an external RC and other components to control the brake terminal, as shown. Brake delay can be set using the equation below to ensure that voice-coil head retract occurs before the spindle motor brake is activated. Once the brake is activated, due to the inherent capacitive input, the three sink drivers will remain active until the device is reset.

$$t_{BRK} = R_B C_B \left(1 - I_n \frac{V_{BRK}}{V_{FAULT} - V_D}\right)$$

Centertap. The A8902CLBA internally simulates the centertap voltage of the motor. To obtain reliable start-up performance from motor to motor, the motor centertap should be connected to this terminal.

External Component Selection. Applications information regarding the selection of external component values is available from the factory for external component selection, frequency-locked loop speed control, and commutation delay capacitor selection.

TYPICAL APPLICATION



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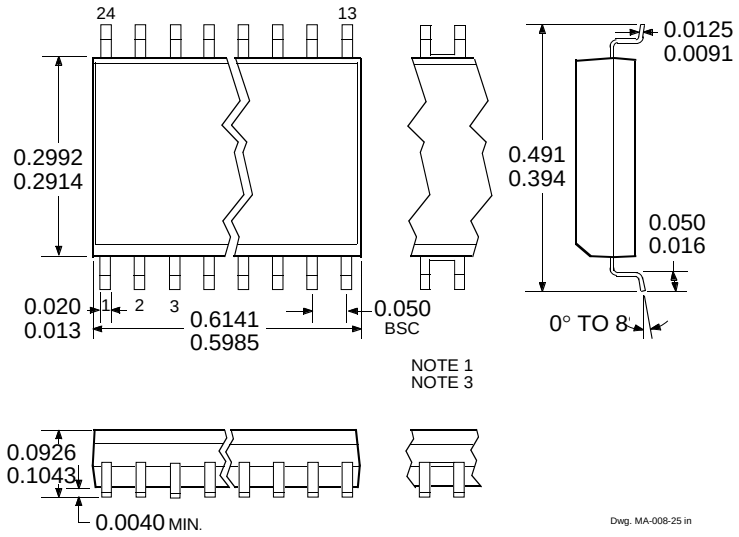
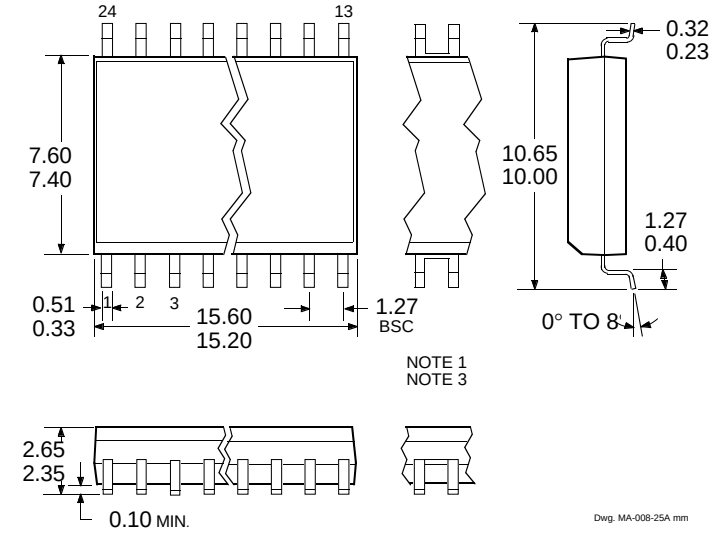
Dimensions in Inches
(for reference only)



Dimensions in Millimeters
(controlling dimensions)



NOTES: 1. Webbed lead frame. Leads 6, 7, 18, and 19 are internally one piece.
2. Lead spacing tolerance is non-cumulative.
3. Exact body and lead configuration at vendor's option within limits shown.

8902–A
3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER

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