

# SNx4HCT74 Dual D-Type Positive-Edge-Triggered Flip-Flops With Clear and Preset

## 1 Features

- Operating voltage range of 4.5 V to 5.5 V
- Outputs can drive up to 10 LSTTL loads
- Low power consumption, 40- $\mu$ A max  $I_{CC}$
- Typical  $t_{pd} = 17$  ns
- $\pm 4$ -mA output drive at 5 V
- Low input current of 1  $\mu$ A max
- Inputs are TTL-voltage compatible

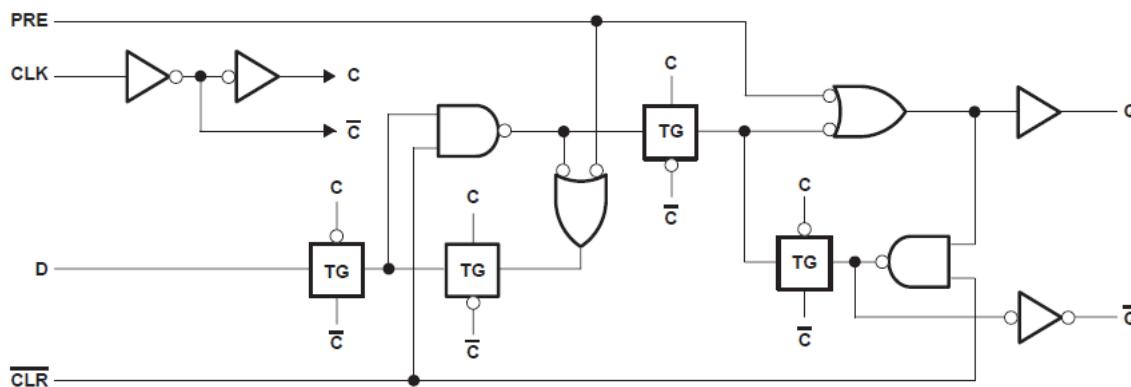
## 2 Description

The 'HCT74 devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
SN74HCT74D	SOIC (14)	8.65 mm × 3.90 mm
SN74HCT74DB	SSOP (14)	6.20 mm × 5.30 mm
SN74HCT74N	PDIP (14)	19.31 mm × 6.35 mm
SN74HCT74NS	SO (14)	10.20 mm × 5.30 mm
SN74HCT74PW	TSSOP (14)	5.00 mm × 4.40 mm
SNJ54HCT74FK	LCCC (20)	8.89 mm × 8.45 mm
SNJ54HCT74W	CFP (14)	9.21 mm × 6.29 mm
SNJ54HCT74J	CDIP (14)	19.55 mm × 6.71 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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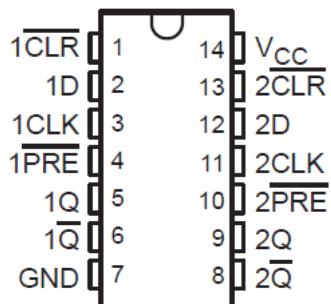
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## 3 Revision History

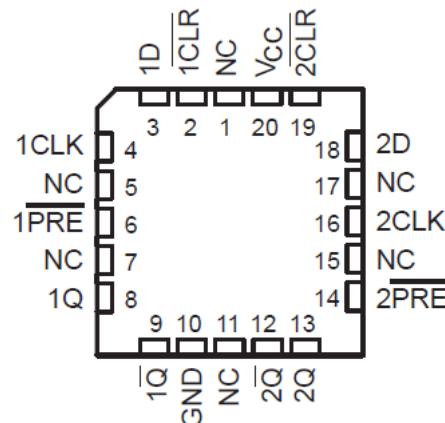
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision F (February 2022) to Revision G (October 2022)</b>	<b>Page</b>
• Changed R0JA for packages: D (86 to 138.7); N (80 to 61.1); NS (76 to 88.4); PW (113 to 114.7).....	<b>4</b>

## 4 Pin Configuration and Functions



J, W, D, DB, N, NS, or PW package  
14-Pin CDIP, CFP, SOIC, SSOP, PDIP, SO, or TSSOP  
Top View



NC - No internal connection

**FK Package**  
**20-Pin LCCC**  
Top View

## 5 Specifications

### 5.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>		± 20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		± 20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		± 25	mA
	Continuous current through V <sub>CC</sub> or GND			± 50	mA
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54HCT74 <sup>(2)</sup>			SN74HCT74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2		2			V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V		0.8			0.8	V
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	0	V <sub>CC</sub>	V <sub>CC</sub>	V
Δt/Δv	Input transition rise/fall time			500			500	ns
T <sub>A</sub>	Operating free-air temperature	-55		125	-40		85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

(2) SN54HCT74 is in product preview.

### 5.3 Thermal Information

THERMAL METRIC	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	UNIT	
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	138.7	109.8	61.1	88.4	114.7	°C/W
R <sub>θJC (top)</sub>	Junction-to-case (top) thermal resistance	93.8	54.7	48.9	46	44.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	94.7	58.6	40.9	48.9	57.6	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	49.1	15.5	28.5	13.8	4.8	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	94.3	58	40.6	48.4	57	°C/W
R <sub>θJC (bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT74 <sup>(2)</sup>		SN74HCT74		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4.5 V	4.4	4.499		4.4		4.4		V
			3.98	4.3		3.7		3.84		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	4.5 V	0.001	0.1		0.1		0.1		V
			0.17	0.26		0.4		0.33		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	5.5 V	±0.1	±100		±1000		±1000		nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	5.5 V			4		80		40	µA
ΔI <sub>CC</sub> <sup>(1)</sup>	One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>	5.5 V		1.4	2.4		3		2.9	mA
C <sub>i</sub>		4.5 V to 5.5 V		3	10		10		10	pF

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

(2) SN54HCT74 is in product preview.

## 5.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HCT74 <sup>(1)</sup>		SN74HCT74		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	4.5 V		27		18		22	MHz
		5.5 V		30		20		24	
t <sub>w</sub>	Pulse duration	PRE or CLR low	4.5 V	16		24		20	ns
			5.5 V	14		21		18	
		CLK high or low	4.5 V	18		27		23	
			5.5 V	16		24		21	
t <sub>su</sub>	Setup time before CLK↑	Data	4.5 V	12		18		15	ns
			5.5 V	11		16		14	
		PRE or CLR inactive	4.5 V	0		0		0	
			5.5 V	0		0		0	
t <sub>h</sub>	Hold time, data after CLK↑	4.5 V	0		0		0		ns
		5.5 V	0		0		0		

(1) SN54HCT74 is in product preview.

## 5.6 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see [Parameter Measurement Information](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT74 <sup>(1)</sup>		SN74HCT74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			4.5 V	27	40		18		22		MHz
			5.5 V	30	46		20		24		
t <sub>pd</sub>	PRE or CLR	Q or $\bar{Q}$	4.5 V		21	35		53		44	ns
			5.5 V		17	31		48		40	
	CLK	Q or $\bar{Q}$	4.5 V		20	28		42		35	
			5.5 V		18	25		38		31	
t <sub>t</sub>		Q or $\bar{Q}$	4.5 V		8	15		22		19	ns
			5.5 V		7	14		20		17	

(1) SN54HCT74 is in product preview.

## 5.7 Operating Characteristics

T<sub>A</sub> = 25°C

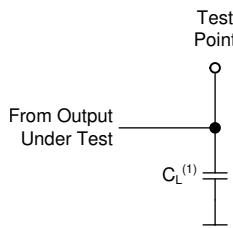
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per flip-flop	No load	35	pF

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_t < 6$  ns.

For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1)  $C_L$  includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs

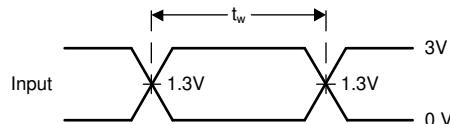


Figure 6-2. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

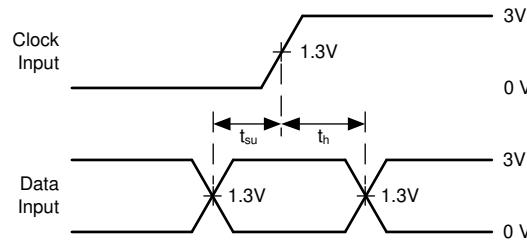
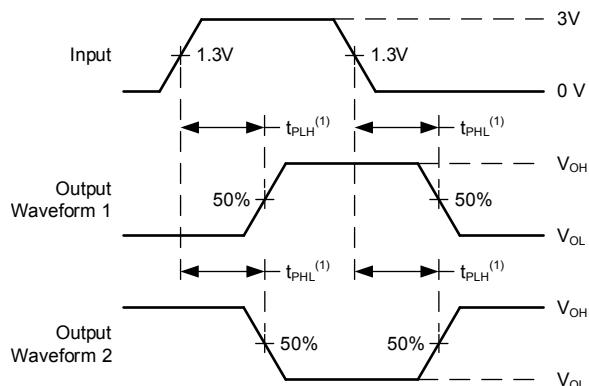


Figure 6-3. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

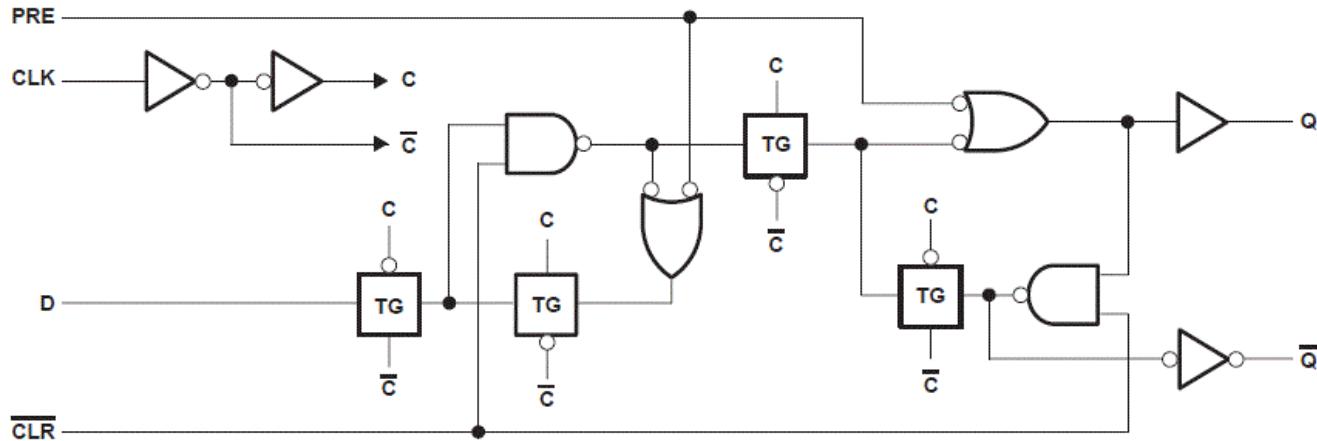
Figure 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

## 7 Detailed Description

### 7.1 Overview

The 'HCT74 devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset (PRE) or clear (CLR) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

### 7.2 Functional Block Diagram



### 7.3 Device Functional Modes

Table 7-1. Function Table

INPUTS				OUTPUT	
PRE	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>(1)</sup>	H <sup>(1)</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	$Q_0$	$\overline{Q}_0$

(1) This configuration is nonstable; that is, it does not persist when  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.

## 8 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 8.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 8.2 Layout

#### 8.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

#### [TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JM38510/65352B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65352B2A
JM38510/65352B2A.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65352B2A
JM38510/65352BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65352BCA
JM38510/65352BCA.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65352BCA
JM38510/65352BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65352BDA
JM38510/65352BDA.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65352BDA
M38510/65352B2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65352B2A
M38510/65352BCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65352BCA
M38510/65352BDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 65352BDA
<b>SN74HCT74D</b>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 85	HCT74
<b>SN74HCT74DBR</b>	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT74
<b>SN74HCT74DBR.A</b>	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT74
<b>SN74HCT74DR</b>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HCT74
<b>SN74HCT74DR.A</b>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74
<b>SN74HCT74DR.B</b>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74
<b>SN74HCT74DRE4</b>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74
<b>SN74HCT74DRE4.A</b>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74
<b>SN74HCT74N</b>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT74N
<b>SN74HCT74N.A</b>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT74N
<b>SN74HCT74NE4</b>	Active	Production	PDIP (N)   14	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HCT74N
<b>SN74HCT74NSR</b>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74
<b>SN74HCT74NSR.A</b>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT74

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74HCT74PW</a>	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 85	HT74
<a href="#">SN74HCT74PWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HT74
SN74HCT74PWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT74
SN74HCT74PWRG4	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT74

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN54HCT74, SN74HCT74 :

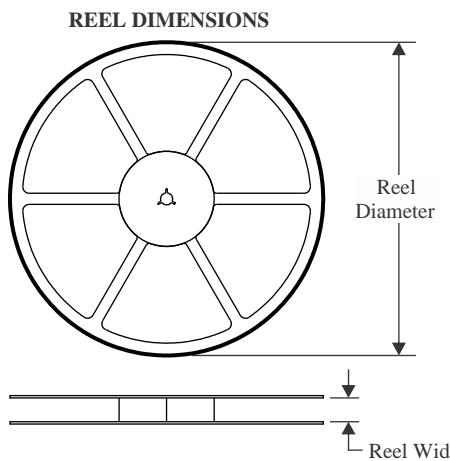
- Catalog : [SN74HCT74](#)

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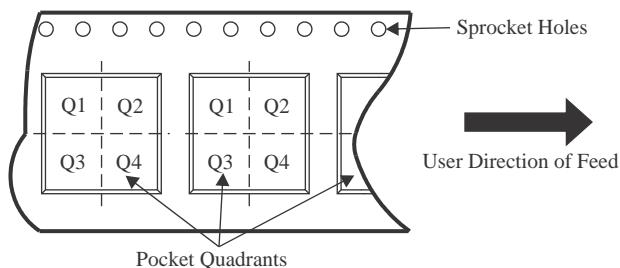
- Military : [SN54HCT74](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

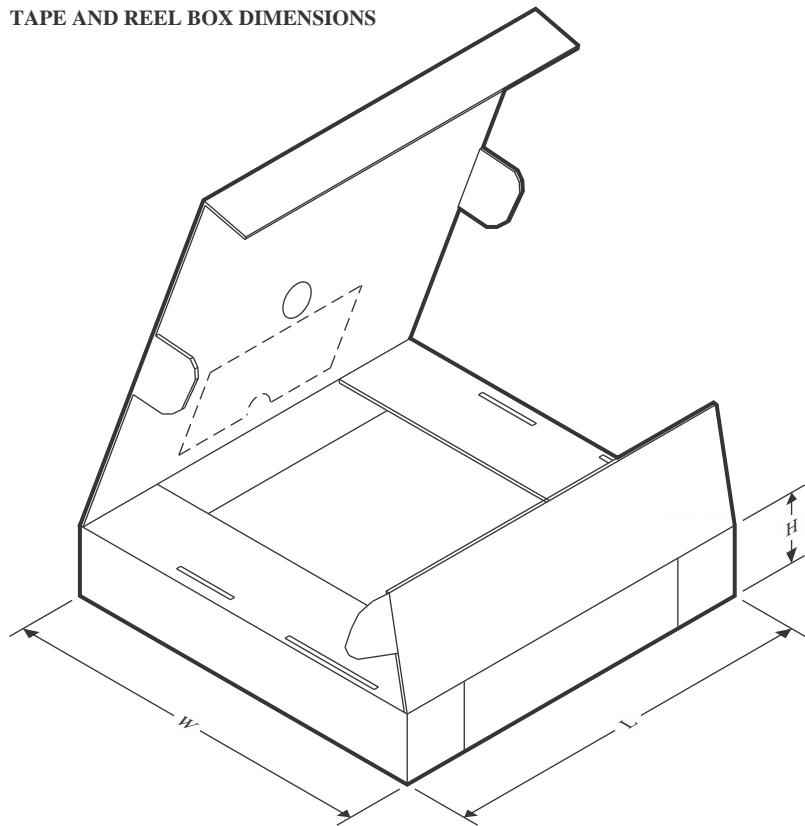
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


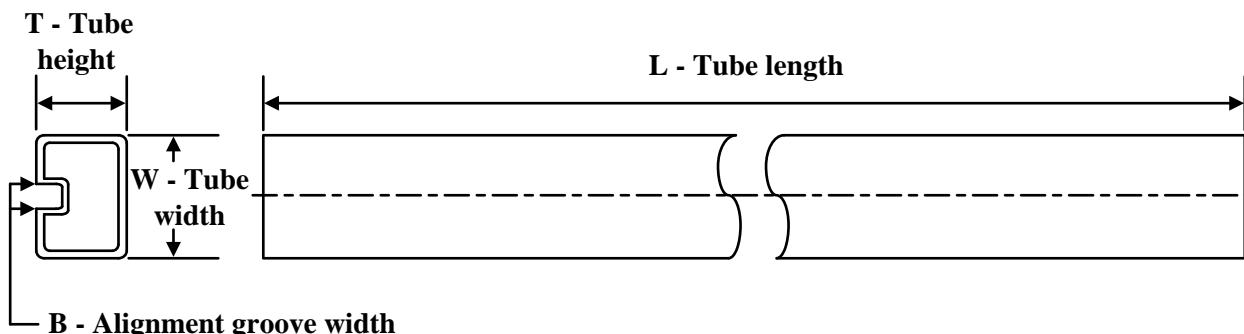
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT74DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HCT74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT74DRE4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCT74NSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HCT74PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT74PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT74PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT74DBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74HCT74DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74HCT74DRE4	SOIC	D	14	2500	353.0	353.0	32.0
SN74HCT74NSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74HCT74PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCT74PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74HCT74PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

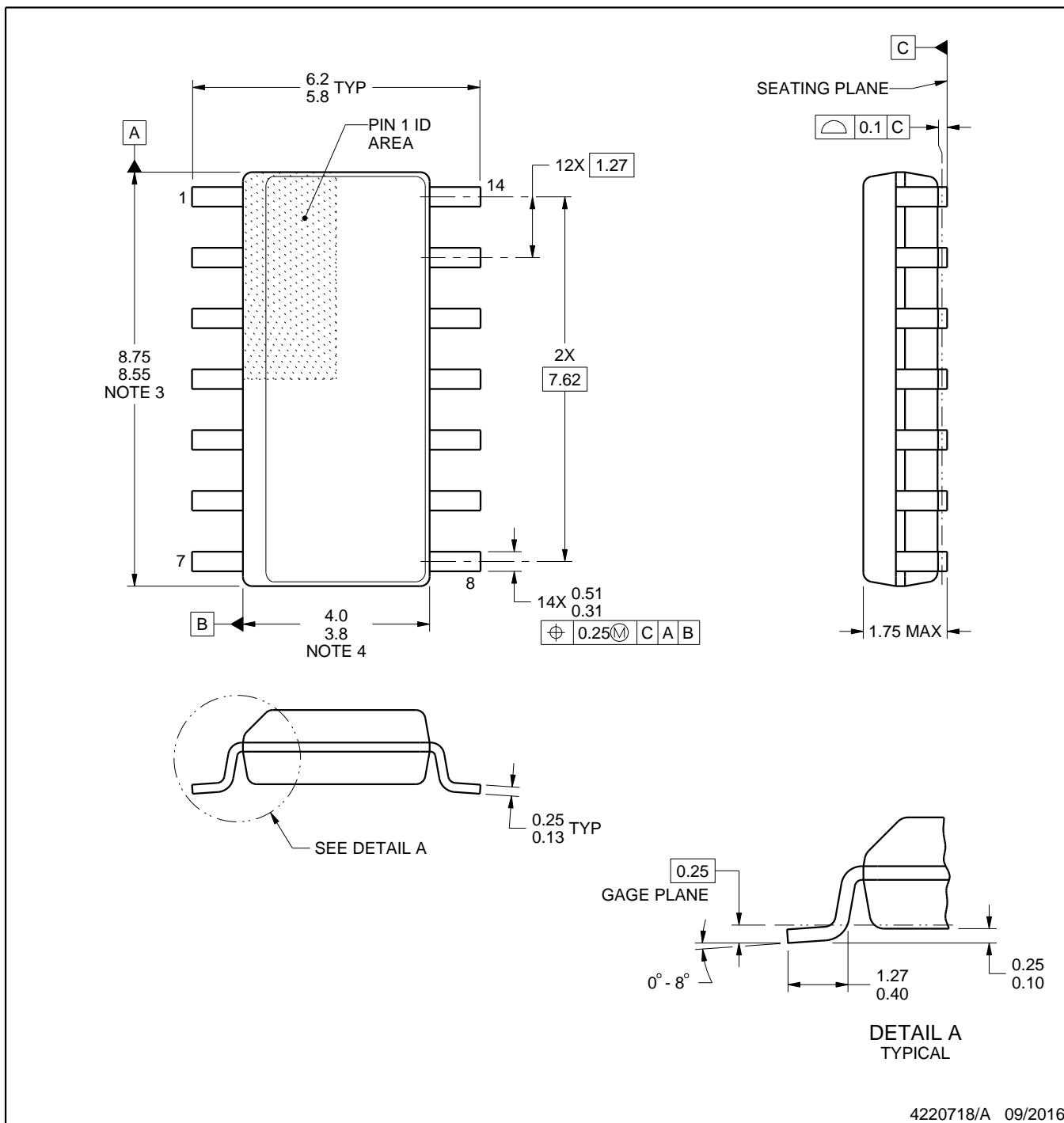
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JM38510/65352B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/65352B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/65352BDA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/65352BDA.A	W	CFP	14	25	506.98	26.16	6220	NA
M38510/65352B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/65352BDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74HCT74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT74N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT74N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT74N.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT74NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74HCT74NE4	N	PDIP	14	25	506	13.97	11230	4.32

# PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



## NOTES:

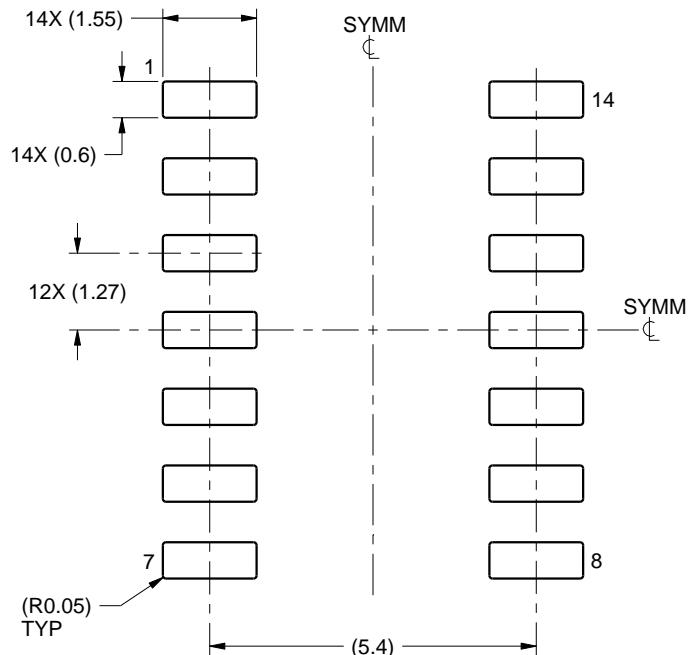
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

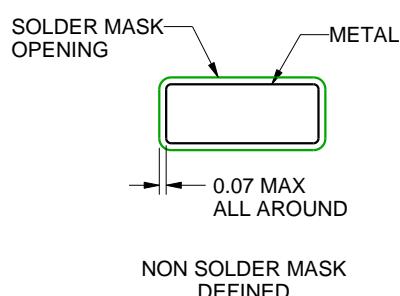
D0014A

SOIC - 1.75 mm max height

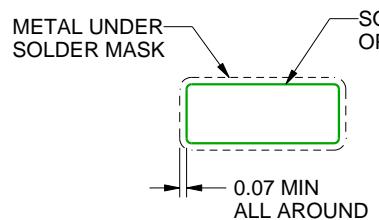
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

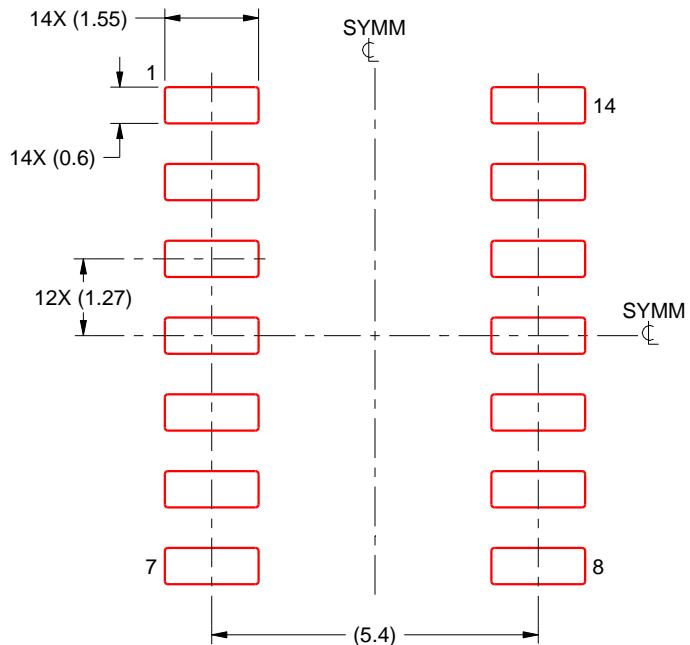
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

## PLASTIC SMALL-OUTLINE PACKAGE

**14-PINS SHOWN**

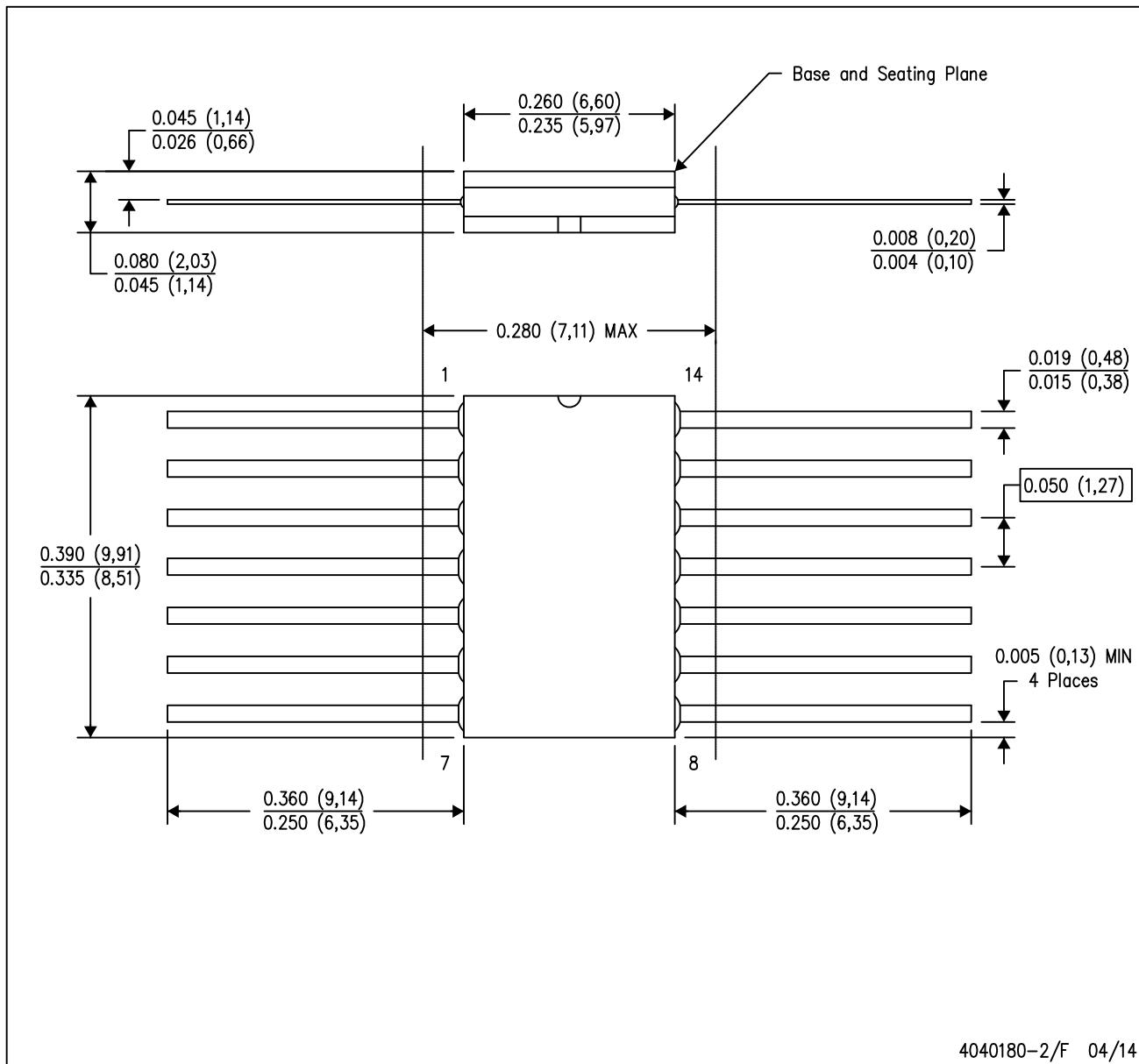


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



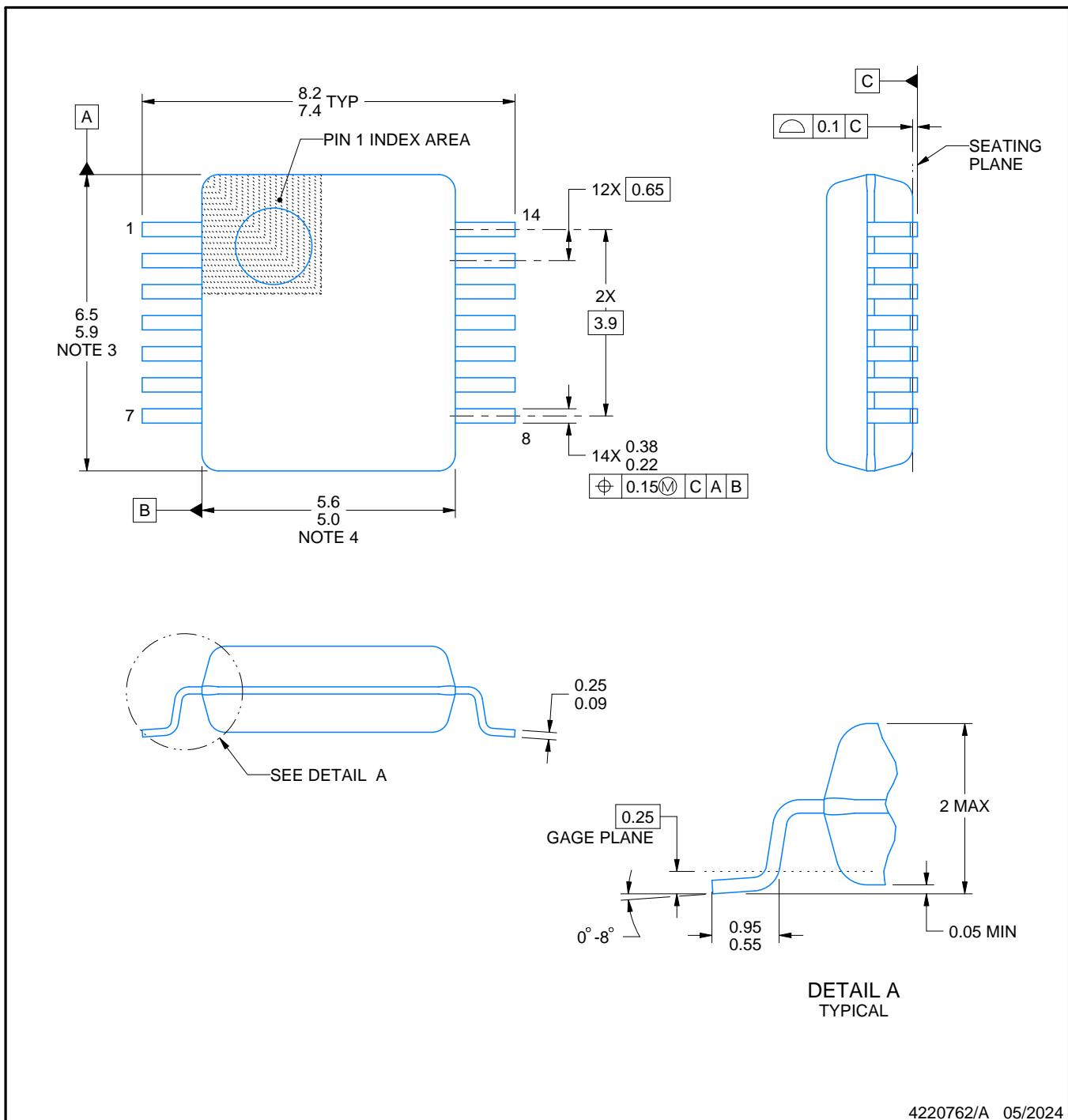
NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL-STD 1835 GDFP1-F14

# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

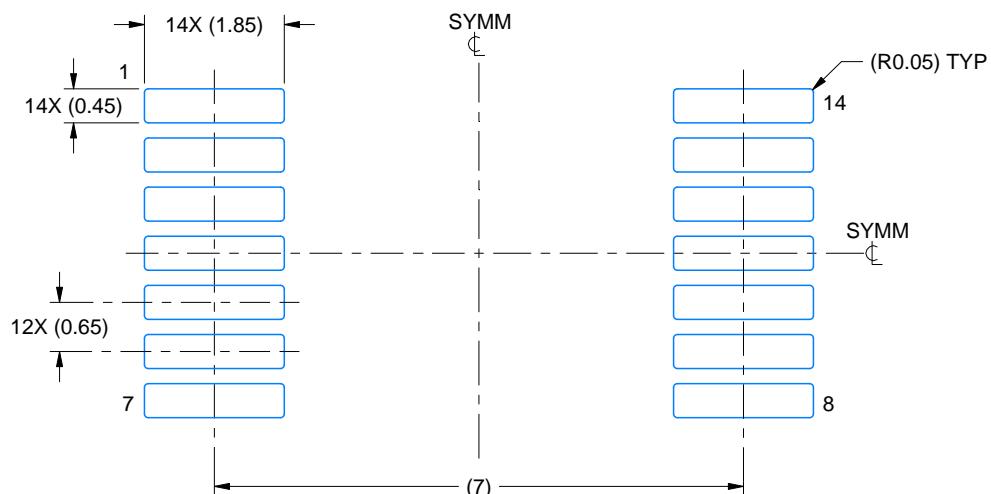
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

## EXAMPLE BOARD LAYOUT

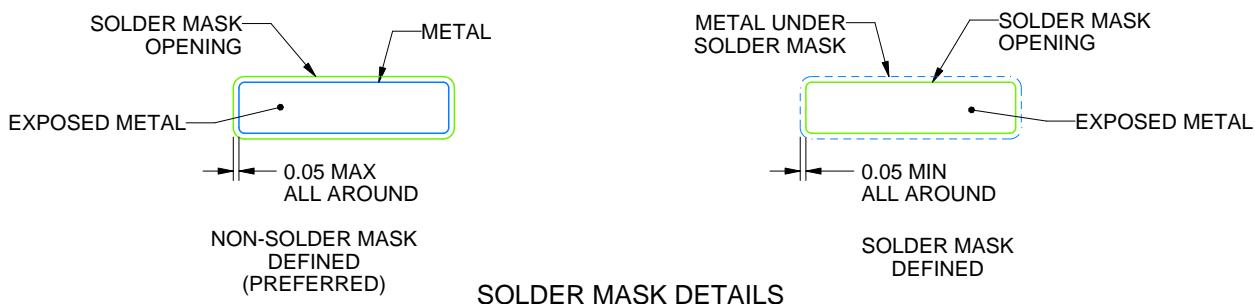
**DB0014A**

## SSOP - 2 mm max height

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

#### NOTES: (continued)

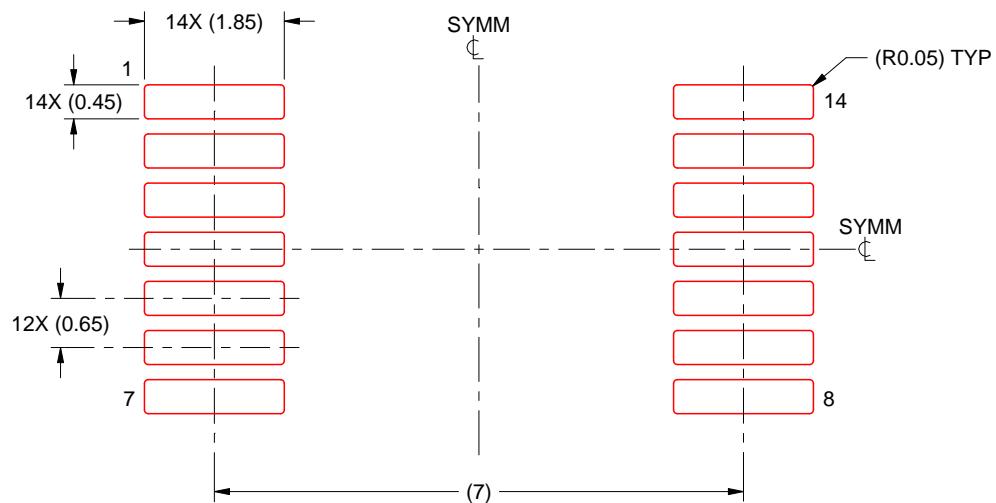
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

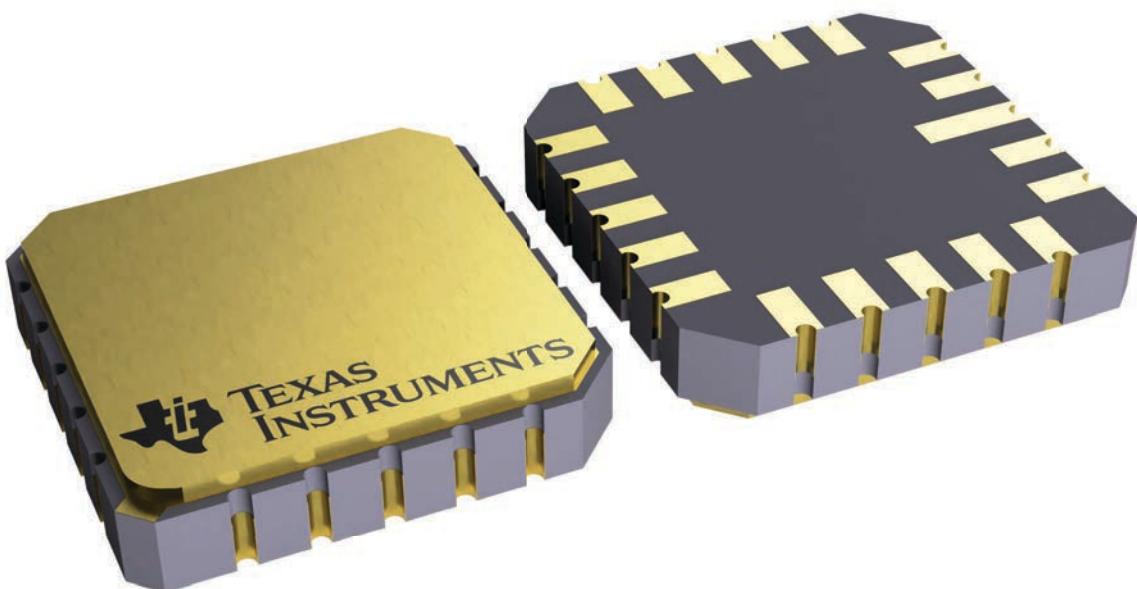
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



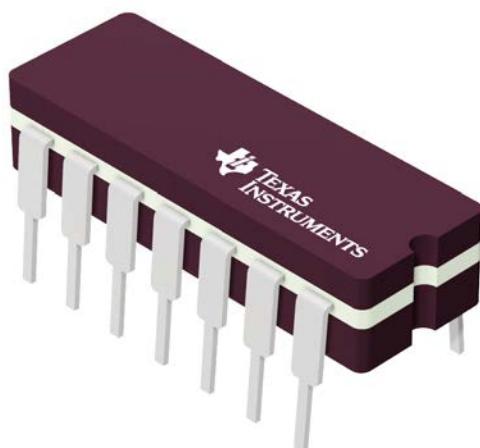
4229370VA\

# GENERIC PACKAGE VIEW

**J 14**

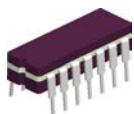
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

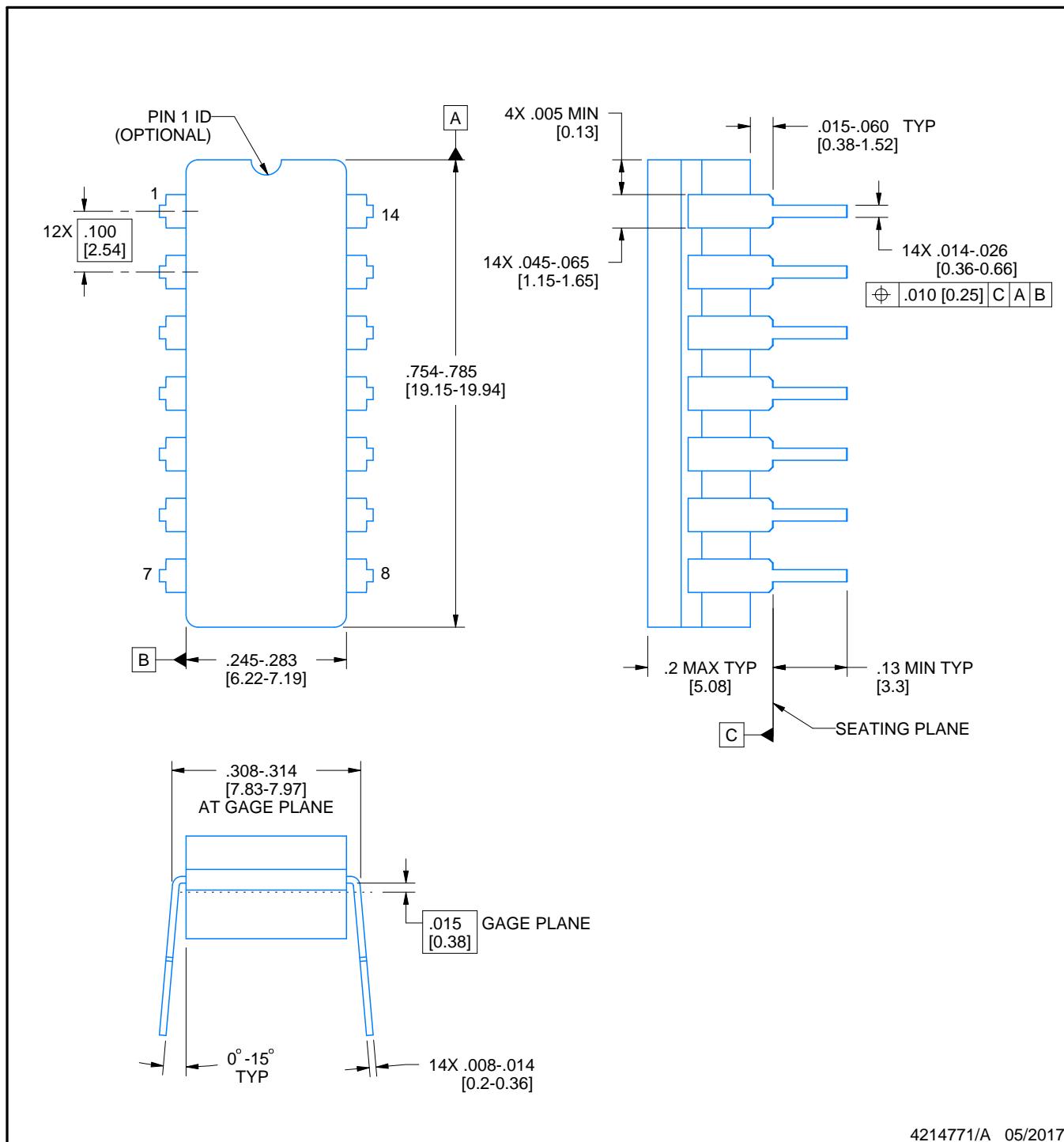


# PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

## NOTES:

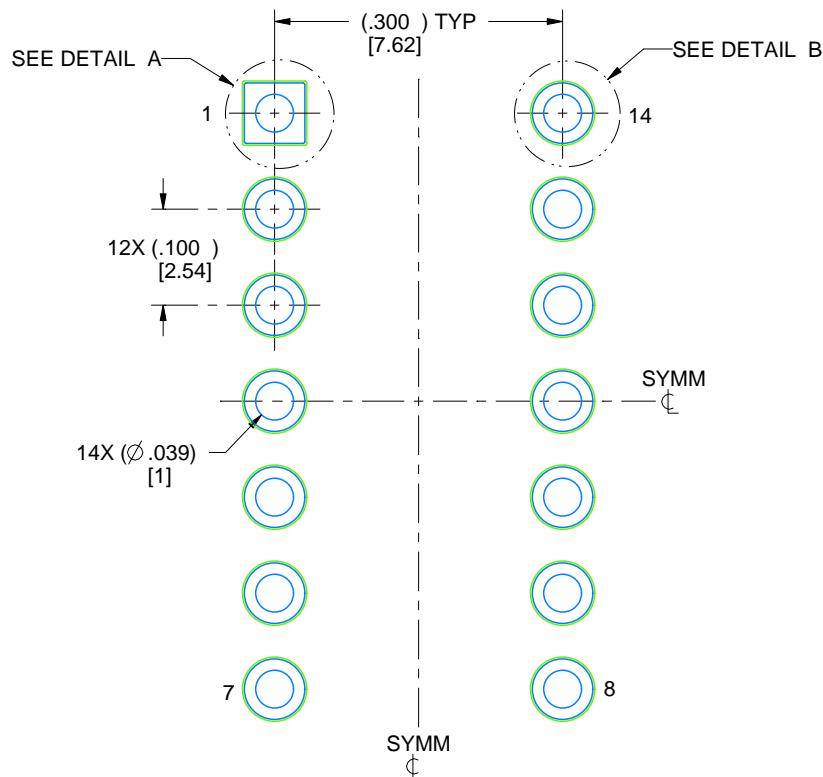
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

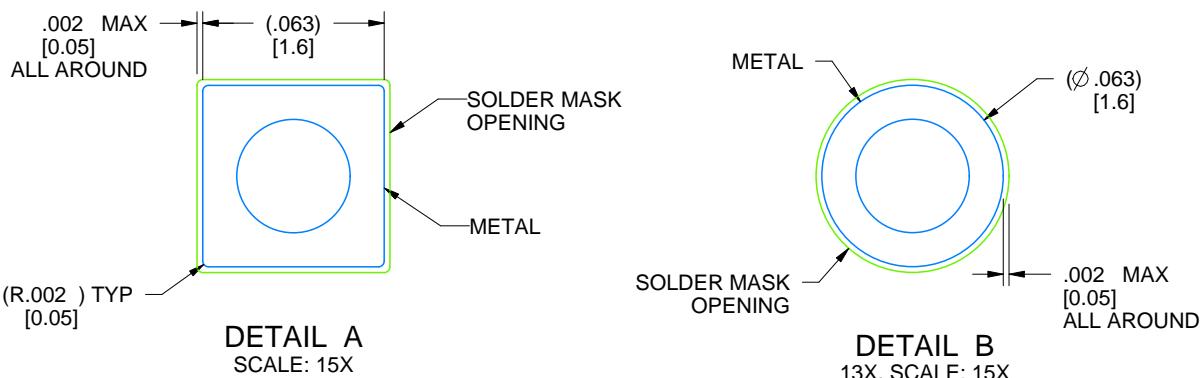
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X

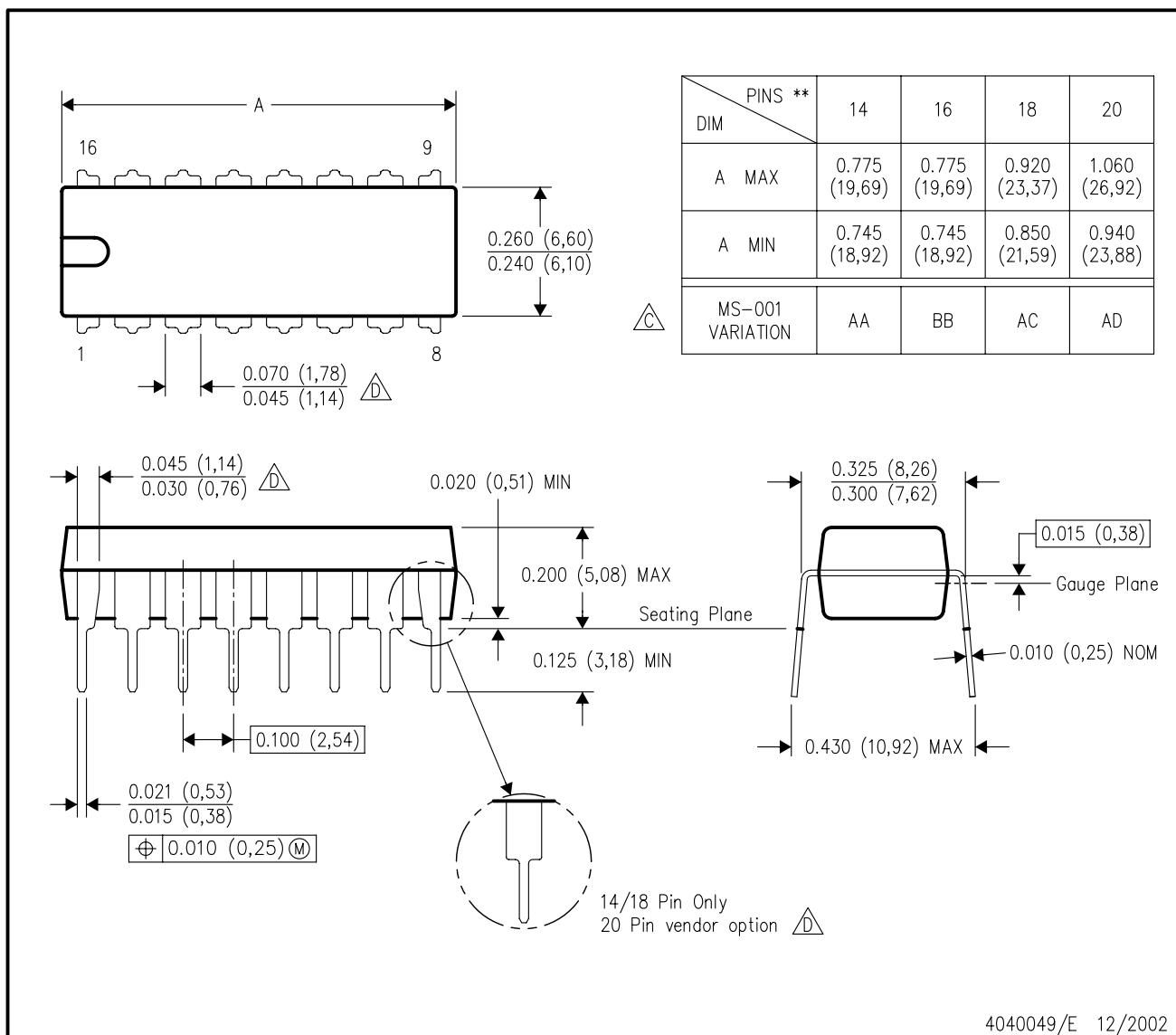


4214771/A 05/2017

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



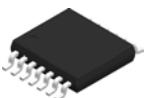
NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

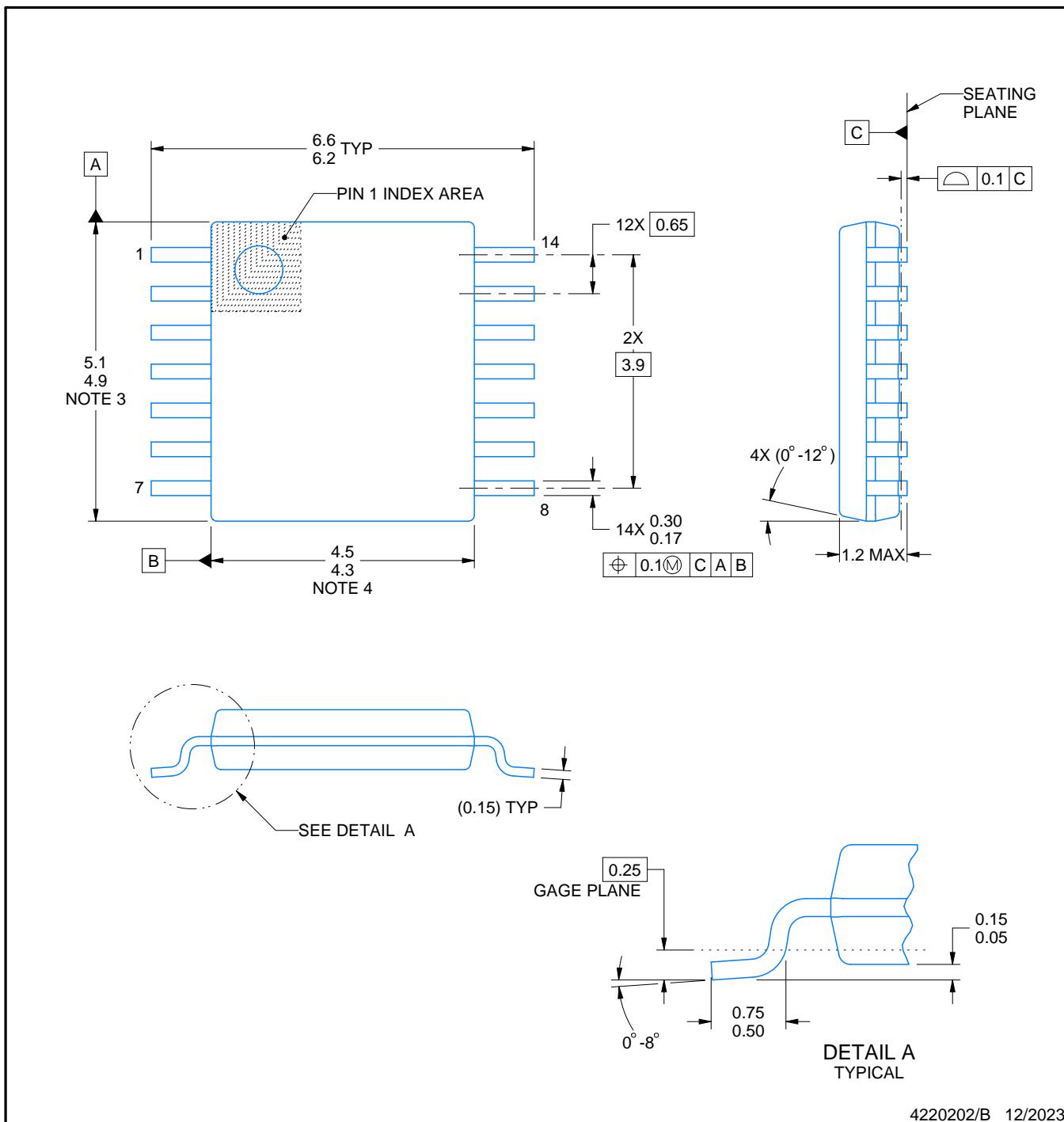
# PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

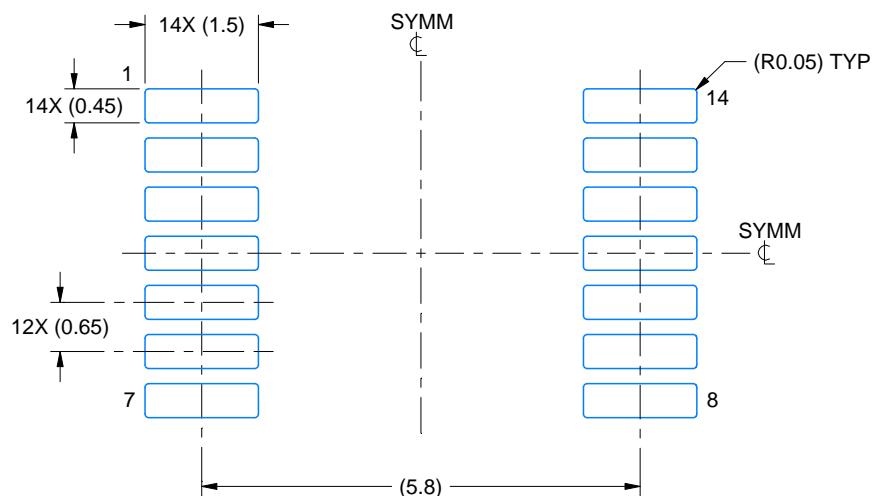
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

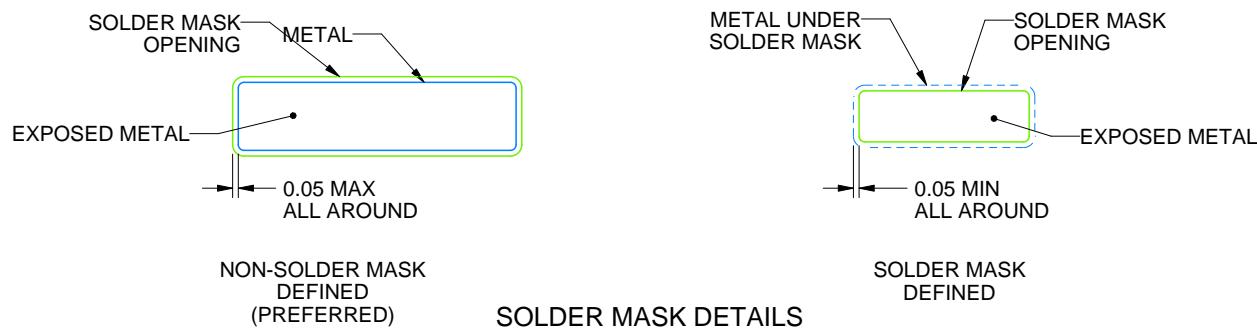
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

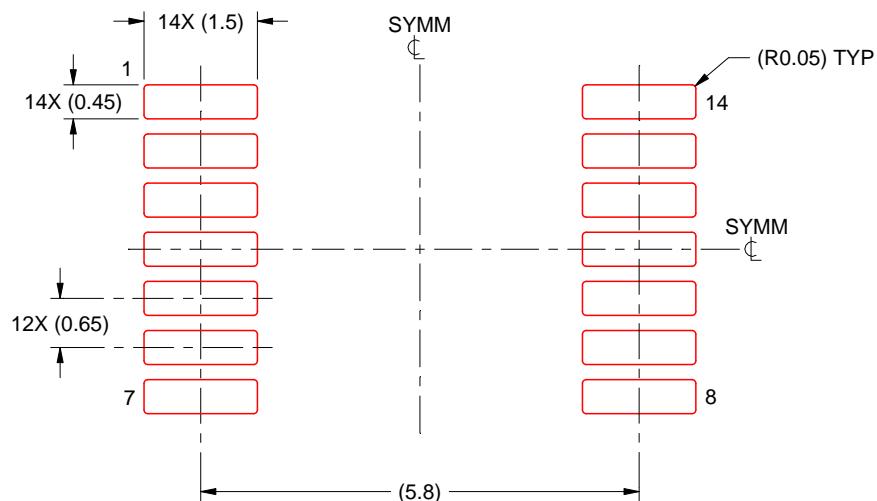
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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