Intel® 41210 Serial to Parallel PCI Bridge

Specification Update

July 2004

Notice: The Intel® 41210 Serial to Parallel PCI Bridge may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Document Number: 301208-003

Contents

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Revision History

Date	Version	Description
July 2004	003	• Added Erratum 31 • Added Specification Change 6 • Removed Documentation Changes 2 and 3 • Added Documentation Change 4
May 2004	002	• Updated status of Erratum 15, 16, 17, 21, 22, and 23. • Added Marking Information • Added Erratum 24 through 30. • Added Specification Changes 2 through 5. • Added Documentation Changes 1 through 3.
March 2004	001	Initial release

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel® 41210 Serial to Parallel PCI Bridge Developer's Manual	278890
Intel® 41210 Serial to Parallel PCI Bridge Design Guide	278801
Intel® 41210 Serial to Parallel PCI Bridge Datasheet	278875

Nomenclature

Errata are design defects or errors. These may cause the Intel® 41210 Serial to Parallel PCI Bridge's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® 41210 Serial to Parallel PCI Bridge product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.
Plan Fix:	This erratum may be fixed in a future stepping of the product.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata (Sheet 1 of 2)

No.	Steppings				Page	Status	Errata
	A1	B0	C0	C1			
1	X				12	Fixed	JTAG HIGHZ command does not function
2	X				12	Fixed	Boundary scan input data inverted
3	X				12	Fixed	Some correctable errors may result in system hang
4	X				12	Fixed	Incorrect default value for PCI Express Next Pointer register in EXP_NXTP interrupt controller register set
5	X				13	Fixed	PxM66EN set to incorrect voltage
6	X				13	Fixed	Intel® 41210 Serial to Parallel PCI Bridge data corruption without error forwarding to MCH
7	X				13	Fixed	Link-Level Retry Buffer (LLRB) data parity error triggers link down instead of forwarding error
8	X				14	Fixed	Link-Level Retry Buffer (LLRB) header parity error forwarding to MCH instead of causing link down
9	X				14	Fixed	SERR# set to incorrect voltage
10	X				14	Fixed	JTAG TDO set to incorrect voltage
11	X				15	Fixed	PCI-Express link fails to train when using polarity inversion
12	X	X			15	Fixed	Secondary bus may not initialize correctly at 100 MHz PCI-X or 133 MHz
13	X	X			16	Fixed	PCI-X memory write with data parity error on either bus A or bus B, sets the bus A Master Data Parity Error bit
14	X	X			16	Fixed	Signaled system error set when message is not escalated
15	X	X	X		17	Fixed	Intermittent PCI 33 MHz operation when PCI-X initialization is expected
16	X	X	X	X	17	No Fix	Secondary bus PxPCIRST# pulse prior to the rising edge of PWROK
17	X	X			17	No Fix	Unable to train in ×1 on Lane 3, 4, or 7 when Lane 0 is broken
18	X	X	X	X	17	No Fix	IOxAPIC End-Of-Interrupt (EOI) register is read/write but should be write-only
19	X	X	X	X	18	No Fix	Unreliable PCI Express* link operation when L0s active state power management is enabled
20		X	X	X	18	No Fix	Slow edge rates are observed when the Intel® 41210 Serial to Parallel PCI Bridge is driving the PCI-X bus at specific temperatures
21			X		18	Fixed	PCI link training failures on cold reset
22			X		18	Fixed	PCI Express* link retraining fails after MCH issues secondary bus reset
23	X	X	X		19	Fixed	ACK/NAK DLLP with reserved encoding causes compliance issue
24	X	X	X	X	19	No Fix	SSE bit set for PERR# assertion when error reporting is masked

Errata (Sheet 2 of 2)

No.	Steppings				Page	Status	Errata
	A1	B0	C0	C1			
25	X	X	X	X	19	No Fix	Data Parity Error detected on PCI/X interface fails to propagate bad parity
26	X	X	X	X	19	No Fix	41210 Bridge Fails to train down in the Presence of a degraded lane
27	X	X	X	X	20	No Fix	PCI Express and PCI-X Header Logs and First Error Pointers do not remain sticky through reset.
28	X	X	X	X	20	No Fix	Incorrect Default Value for PCI Express Flow Control Protocol Error Severity Bit.
29	X	X	X	X	20	No Fix	Power State Bits in PCI Express Power Management Control/Status Register mistakenly accept reserved values.
30	X	X	X	X	21	No Fix	Performance across an Upstream x1 PCI Express Link is less than expected.
31	X	X	X	X	21	No Fix	SKP Ordered Set may not be sent within required interval during link recovery if a packet is pending

Specification Changes

No.	Steppings			Page	Specification Changes
	A1	B0	C0		
1		X	X	22	Ball pad T24 changes from an NC (No Connect NC17) to a pin that requires an external pull-up resistor
2	X	X	X	22	L0s state is not supported
3	X	X	X	22	Linear Voltage Regulators are Recommended for 1.5 V supplies
4	X	X	X	22	Updated Power Sequencing Steps for VCC15 and VCC33 Voltages
5	X	X	X	23	Use Microcontroller When Implementing Some Erratum Workarounds
6	X	X	X	23	BCNF Bit 3 Changed to Reserved bit

Specification Clarifications

No.	Steppings			Page	Status	Specification Clarifications
	A1	B0	C0			
None for this revision of this specification update.						

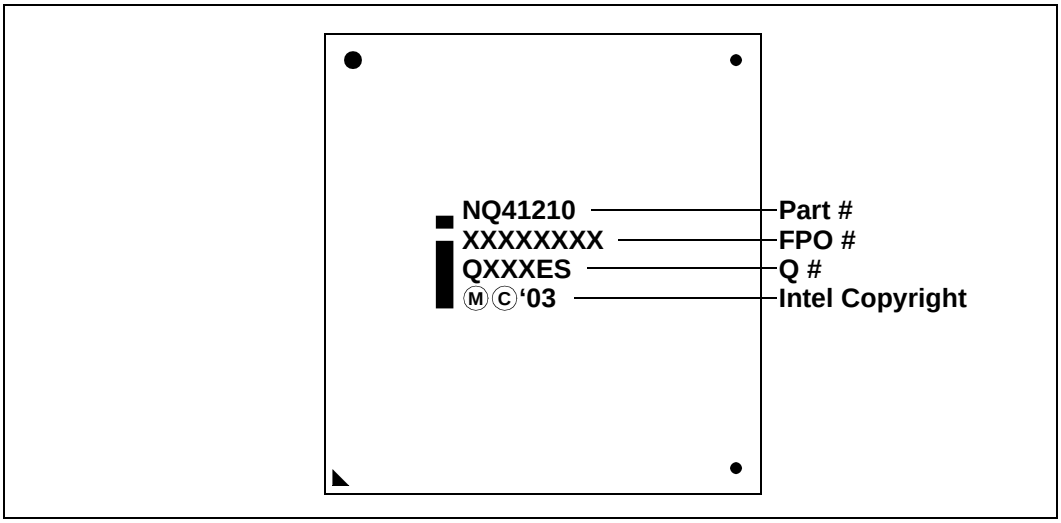
Documentation Changes

No.	Document Revision	Page	Documentation Changes
1	278890-001 278801-001	25	L0s state is not supported.
2	278801-001	25	Removed; incorporated into Design Guide
3	278801-001	25	Removed; incorporated into Design Guide
4	278890-001	25	Offset 40h: BCNF - Bridge Configuration Register Bit 3 Changed to Reserved

Identification Information

Markings

Figure 1. Marking Information



Stepping	Q Number	MM Number†	Notes
A1	Q645ES	857075	
B0	Q584ES	856480	
C0 with burn-in	Q718ES	858281	
C0 without burn-in	Q719ES	858282	
C1 with burn-in	Q812ES	861105	
C1 without burn-in	Q813ES	860905	
Production	SL7JE	860909	

NOTE:

† MM = Material Master ID. Reference the MM when placing an order.

Errata

1. JTAG HIGHZ command does not function

Problem: When in JTAG mode, the HIGHZ command given through the Test Access Port (TAP) does not force the Intel® 41210 Serial to Parallel PCI Bridge (called hereafter the "41210 Bridge" or "41210") outputs to the High-Z state.

Implication: The JTAG HIGHZ command does not work. Each bit must be set individually.

Workaround: Use the boundary scan chain to force all outputs to High-Z state. This workaround is effective but consumes more time than issuing a HIGHZ instruction, which forces all outputs to a high impedance with one bit being set.

Status: Fixed. See the "Summary Table of Changes" on page 7.

2. Boundary scan input data inverted

Problem: Data driven in during boundary scan gets inverted during the capture phase (all of the 41210 I/O pins, except for SDTA, SCLK, PWROK, and RSTIN#). This is not in compliance with the IEEE Standard Test Access Port and Boundary Scan Architecture 1149.1a Specification.

Implication: Boundary scan tests show errors on most I/O pins.

Workaround: Invert the TDO signal for all but SDTA, SCLK, PWROK, and RSTIN# when using boundary scan software.

Status: Fixed. See the "Summary Table of Changes" on page 7.

3. Some correctable errors may result in system hang

Problem: Some correctable errors, including errors in configuration retries, power management messages, and traffic on the PCI Express* link may result in bad internal parity, resulting in a fatal error.

Implication: Some errors that would otherwise be correctable result in bridge failure and probable system hang. This erratum does not affect normal (error-free) operation.

Workaround: None.

Status: Fixed. See the "Summary Table of Changes" on page 7.

4. Incorrect default value for PCI Express Next Pointer register in EXP_NXTP interrupt controller register set

Problem: The PCI Express Next Pointer register at offset 45H should have a default value of 6CH, indicating Power Management Capability Identifier, but instead is set at 00H, indicating that this is the last capability.

Implication: BIOS-based power management that attempts to access this capability by means of this register does not function.

Workaround: BIOS-based power management can function by accessing the EXP power management capability at offset 6CH.

Status: Fixed. See the "Summary Table of Changes" on page 7.

5. PxM66EN set to incorrect voltage

Problem: The PxM66EN signal is pulled up to 3.3 V with a 5.1 KΩ resistor on the board, but the measured voltage is 1.0 V with or without an add-in card present. PxM66EN should be at 3.3 V without an add-in card present.

Implication: Auto-detection of 66 MHz PCI devices is prevented. The bus speed is forced to 33 MHz when not in PCI-X mode. Only buses that should be set to 66 MHz PCI are impacted.

Workaround: None.

Status: Fixed. See the "Summary Table of Changes" on page 7.

6. Intel® 41210 Serial to Parallel PCI Bridge data corruption without error forwarding to MCH

Problem: Posted transactions with poisoned data may be received by the MCH without detecting a parity error.

Implication: The MCH handles the poisoned data as a normal packet, resulting in silent corrupted data. When the parity error is a result of a transaction from the PCI/PCI-X bus or PCI/PCI-X buffer RAM parity error, the error-message escalation occurs from the 41210, when enabled. When the parity error is the result of PCI Express buffer RAM parity error, no error escalation occurs. In the latter case, none of the registers indicate a failure.

Workaround: None.

Status: Fixed. See the "Summary Table of Changes" on page 7.

7. Link-Level Retry Buffer (LLRB) data parity error triggers link down instead of forwarding error

Problem: A posted transaction (replayed) with data that utilizes a three-DWord header and encounters an LLRB RAM parity error in the location where the last DWord is stored triggers a link polling LTSSM state instead of forwarding the error.

Implication: System failure is likely to occur, causing the 41210 to be reset, all in-flight transactions within the 41210 to be lost, and the PCI/PCI-X busses on the 41210 to be reset. The 41210 error escalation does not occur due to the link going down, but MCH registers may notify that the link is down.

Workaround: None.

Status: Fixed. See the "Summary Table of Changes" on page 7.

8. Link-Level Retry Buffer (LLRB) header parity error forwarding to MCH instead of causing link down

Problem: A posted transaction (replayed) with data followed by a non-posted transaction is enqueued in the LLRB. When the non-posted header control bits [63:48] of the request header encounter a RAM parity error, the request is forwarded over the PCI Express* bus as a poisoned Transaction Layer Packet (TLP) instead of bringing the link down. The packet is forwarded with the header fields (Byte Enable or tag) corrupted, resulting in possible side effects of data corruption, completion timeouts, and unexpected completions.

Implication: A non-posted transaction from the 41210 occurs with setting the received poisoned TLP in MCH. The transaction may have incorrect Byte Enables, which may result in incorrect values returned to the requestor on the 41210. When the tag field is corrupted, the completion returns and matches an incorrect read request or is flagged as an unexpected completion in the 41210. The original request eventually gets a completion timeout. When the MCH supports inbound non-posted write transactions, these transactions may be accepted and data corruption may be seen. When the MCH does not support inbound non-posted write transactions, the unsupported request is returned.

Workaround: None.

Status: Fixed. See the "Summary Table of Changes" on page 7.

9. SERR# set to incorrect voltage

Problem: SERR# is being driven to 1 V. The 41210 detects SERR# being asserted on both segments of the 41210 during boot up and does not detect SERR# assertion when a device on the PCI-X bus asserts SERR#.

Implication: The 41210 falsely detects and logs SERR# assertion for both bridge segments during boot-up due to the SERR# pin being held at 1 V, which the 41210 detects as a logic low (asserted). Devices assert SERR# for a minimum of one clock when an SERR# occurs. Since SERR# is being held low, devices asserting SERR# are not detected by the 41210.

Workaround: None.

Status: Fixed. See the "Summary Table of Changes" on page 7.

10. JTAG TDO set to incorrect voltage

Problem: The JTAG TDO pin voltage should range from 0 V to 3.3 V, but is being set incorrectly to range from 1 V to 2.34 V.

Implication: The effects of this are platform specific. The output voltages for TDO are incorrect, causing difficulty for test equipment and other silicon to analyze JTAG data.

Workaround: When JTAG testing is required, external voltage translation circuitry may be needed to convert TDO voltage levels to the correct functional voltages.

Status: Fixed. See the "Summary Table of Changes" on page 7.

11. PCI-Express link fails to train when using polarity inversion

Problem: On platforms that implement Polarity Inversion on the 41210 Bridge-to-MCH PCI Express link, the link does not train.

Implication: The 41210 is not seen by OS or BIOS and is not configured. This does not affect platforms that do not use polarity inversion.

Workaround: Platform-specific BIOS workarounds have been identified. Please refer to the appropriate BIOS specification.

Status: Fixed. See the "Summary Table of Changes" on page 7.

12. Secondary bus may not initialize correctly at 100 MHz PCI-X or 133 MHz PCI-X mode 1

Problem: When a 133 MHz PCI-X–capable device is plugged into a bus supporting PCI-X greater than 100 MHz, the 41210 may not initialize the bus correctly at 100 MHz PCI-X or 133 MHz PCI-X.

Implication: The bus may initialize at 66 MHz PCI-X.

Workaround: A software and a hardware workaround have been identified for non-hot-plug buses.

Software workaround: For buses with hot-plug disabled, force the bus to the correct frequency by writing to bits[10:9] (PFREQ) of the 41210 Bridge Configuration Register [Bus 0, Device 0, Function 0 (segment A) and Function 2 (segment B), Offset 40–41], and issuing a Secondary Bus Reset (SBR) with bit[6] (SBR) in the Bridge Control Register (Bus 0, Device 0, Function F0 and F2, Offset 3E). This is not a valid workaround to configure a bus in one-slot-no-glue mode.

Hardware workaround: Replace the 3.3 KΩ pull-up resistor on PxPCIXCAP with a 1.5 KΩ resistor. This workaround works only with Conventional PCI and PCI-X mode 1 cards. When this workaround is used on a PCI-X mode 2 capable bus with a PCI-X mode 2 card, improper frequency and mode selection occur.

Status: Fixed. See the "Summary Table of Changes" on page 7.

13. PCI-X memory write with data parity error on either bus A or bus B, sets the bus A Master Data Parity Error bit

Problem: When the SERR# Enable (SEE) bit in 41210 Bridge configuration space (Bus 0, Device 0, Function 0, Offset 04H–05H, bit[8]) is set to enable SERR# reporting on bus A, and a Memory Write is issued with a Data Parity Error (DPE) on either of the secondary buses (A or B), the bus A Master Data Parity (MDP) error bit (Bus 0, Device 0, Function 0, Offset 06H–07H, bit[8]) in the Status (STS) register is set regardless of whether there is a parity error on bus A or bus B. The Parity Error Response (PER) bit (Bus 0, Device 0, Function 0 and 2, Offset 04H–05h, bit[6]) is set to disabled on the side that has the data parity error injected for this case.

The STS MDP bit should not depend on SEE being enabled and should not get set when the PER bit disables DPE reporting. Bus B does not exhibit the same behavior.

Table 1 summarizes the conditions under which this erratum can be reproduced.

Table 1. Errata Conditions

Bus A		Bus B		DPE Injected into Bus	Bus A	Bus B
SEE	PER	SEE	PER		MDP	MDP
1	0	0	0	A	1	0
1	0	0	0	B	1	0

Implication: This erratum nay result in system hang, depending on error handling. This erratum occurs only when the SERR# Enable bit is set.

Workaround: None.

Status: Fixed. See the "Summary Table of Changes" on page 7.

14. Signaled system error set when message is not escalated

Problem: An outbound transaction from the processor to the 41210 Bridge that receives an unsupported request (that is, the 41210 Bridge aborts the transaction internally) does not escalate an error message, but the Status Register Signaled System Error bit (Bus 0, Device 0, Function 0 and 2, Offset 06H–07H, bit 14) is set for each bridge that has the SERR# Enable bit set, in the following scenario:

- SERR# Enable (Bus 0, Device 0, Function 0, 1, 2, and 3, Offset 04H–05H, bit[8]) is set for function 0 and function 2.
- Unsupported Request Reporting Enable, Fatal Error Reporting Enabled, Non-Fatal Error Reporting Enabled, and Correctable Error Reporting Enable bits are set to "disable" in the PCI Express* Device Status Register (Bus 0, Device 0, Function 0, 1, 2, and 3, Offset 4CH–4DH, bits[3:0]).
- PCI Express* Uncorrectable Mask bits are clear (Bus 0, Device 0, Function 0 and 2, Offset 108H–10BH, bits[31:0]).

Implication: There is an indication in 41210 Bridge that an error message was escalated when it was not.

Workaround: None.

Status: Fixed. See the "Summary Table of Changes" on page 7.

15. Intermittent PCI 33 MHz operation when PCI-X initialization is expected

Problem: The secondary bus may intermittently initialize at 33 MHz conventional PCI when the bus should be configured in PCI-X mode.

Implication: Incorrect bus initialization. The secondary bus may initialize at 33 MHz PCI.

Workaround: None.

Status: Fixed. See the "Summary Table of Changes" on page 7.

16. Secondary bus PxPCIRST# pulse prior to the rising edge of PWROK

Problem: During system power on and prior to the 41210 Bridge receiving the rising edge of PWROK, a pulse is observed on the secondary bus PxPCIRST# signals.

Implication: PCI/PCI-X controllers on the secondary bus segments could interpret this PxPCIRST# pulse as a true rising edge and initialize into an undetermined state.

Workaround: A temporary HW workaround has been identified. The PWROK signal that is received by the 41210 Bridge component should be used to gate the secondary bus PxPCIRST# signals.

Status: No Fix. See the "Summary Table of Changes" on page 7.

17. Unable to train in ×1 on Lane 3, 4, or 7 when Lane 0 is broken

Problem: The 41210 fails to train as a ×1 width on either Lane 3, 4, or 7 when Lane 0 is broken (in other words, not electrically visible to the MCH/XMB/TMB).

Implication: This problem prevents 41210 Bridge training as a ×1 in Lane 3, 4, or 7 (when Lane 0 is broken or otherwise electrically disconnected).

Workaround: None

Status: No Fix. See the "Summary Table of Changes" on page 7.

18. IOxAPIC End-Of-Interrupt (EOI) register is read/write but should be write-only

Problem: The IOxAPIC End-Of-Interrupt register (EOI) (Bus 0, Device 0, Functions 1 and 3, Direct Memory Space Register, Offset 40h) should be write-only. The APIC specification specifies that this register must be implemented as write-only. In the 41210, this register is inadvertently implemented as read-write.

Implication: When implemented as write-only, this register returns the value FFh when read. Since this register is implemented as read-write, the 41210 Bridge returns the "real" value of the register contents when read.

There is no impact to functionality.

Workaround: None.

Status: No Fix. See the "Summary Table of Changes" on page 7.

19. Unreliable PCI Express* link operation when L0s active state power management is enabled

Problem: PCI Express* link operation is unreliable after the L0s state is enabled in the 41210 Bridge.

Implication: When L0s is enabled, the system may hang or behave in an unstable manner.

Workaround: The link control register must be written to prevent the 41210 from entering L0s. A platform-dependent BIOS workaround has been identified. Please refer to Specification Changes "L0s state is not supported" on page 22 and to the *Intel® 41210 Serial to Parallel PCI Bridge Initialization by the SMB Bus Using The PIC16F876A Microcontroller White Paper (302281)* for details on how to disable L0s support and implement this workaround.

Status: No Fix. See the "Summary Table of Changes" on page 7.

20. Slow edge rates are observed when the Intel® 41210 Serial to Parallel PCI Bridge is driving the PCI-X bus at specific temperatures

Problem: Signal-integrity issues may occur at a specific temperature when 41210 Bridge is driving the PCI/PCI-X bus. This issue is highly sensitive to temperature and occurs within a narrow range (1–2 °C) within the normal operating temperature range. The failing temperature varies for each die. The cause of the problem is that a hidden register is loaded with an inappropriate value, causing incorrect drive strength on PCI signals.

Implication: Parity errors and system hangs may occur.

Workaround: Write 1s to the bridge configuration space (address offset 224h, bits[29:17], function 0 and 2). This must be done before any PCI-X bus access occurs. Please refer to the *Intel® 41210 Serial to Parallel PCI Bridge Initialization by the SMB Bus Using The PIC16F876A Microcontroller White Paper (302281)* for details on implementing this workaround.

Status: No Fix. The workaround must be in place for all steppings of the 41210 Bridge. See the "Summary Table of Changes" on page 7.

21. PCI link training failures on cold reset

Problem: On a front-panel reset (cold reset), the ×8 PCI Express* link may train to degraded link widths or fail to train. This is caused by the timing of state transitions on the PCIE link.

Implication: After a cold reset, a ×8 PCI Express* link may degrade to ×4 or ×1 link widths, or fail to train.

Workaround: A platform-dependant BIOS workaround has been identified. Please refer to the appropriate BIOS specification.

Status: Fixed. See the "Summary Table of Changes" on page 7.

22. PCI Express* link retraining fails after MCH issues secondary bus reset

Problem: When the MCH issues a secondary bus reset (hot reset), the link width may degrade or link training may fail.

Implication: After a hot reset, the PCI Express* link may fail to train, or train to a degraded link width.

Workaround: None at this time

Status: Fixed. See the "Summary Table of Changes" on page 7.

23. ACK/NAK DLLP with reserved encoding causes compliance issue

Problem: The 41210 can occasionally issue an ACK or NAK with reserved encoding.

Implication: There is no known implication, but PCIE compliance may be an issue.

Workaround: None

Status: Fixed. See the "Summary Table of Changes" on page 7.

24. SSE bit set for PERR# assertion when error reporting is masked

Problem: During a downstream memory write to 41210 Bridge, the following erroneous behavior is seen when PERR# is asserted on the secondary bus:

- Signaled System Error (SSE) in the STS_REG register (D:0, F:0&2, offset 06h, bit 14) is set when SERR# Enable (SEE) (D:0, F:0&2, offset 04h, bit 8) and Parity Error Response Enable (PERE) (D:0, F:0&2, offset 04h, bit 6) are set in the CMD register.
- The PERE bit in the BRDG_CNTL register is set (D:0, F:0&2, offset 3Eh, bit 0).
- Error reporting is disabled in the UNC_PXERRMSK register (D:0, F:0&2, offset 130h).

Implication: False indication of an error message escalated as recorded in SSE of the STS_REG register being set. This is considered low risk since the escalation of the message is functioning properly.

Workaround: None at this time.

Status: No Fix. See the "Summary Table of Changes" on page 7

25. Data Parity Error detected on PCI/X interface fails to propagate bad parity

Problem: In PCI and PCI-X mode using 32-bit data transfers, when a read request gets disconnected at an even dword boundary with data parity error, such that the subsequent request for partial data gets retried, the completion for this request is issued over PCI Express to the MCH (root complex) without the poisoned data EP field set in the PCI-Express TLP header.

Implication: Corrupted Data forwarded without error indication if error escalation is not enabled.

Workaround: Uncorrectable error escalation must be enabled in the MCH and 41210 Bridge to contain this data parity escape. Therefore, a complete workaround for this Erratum will also require MCH/root complex escalate parity errors correctly appropriate platform. Please refer to the *Intel® 41210 Serial to Parallel PCI Bridge Initialization by the SMB Bus Using The PIC16F876A Microcontroller White Paper (302281)* for details on implementing this workaround.

Status: No Fix. See the "Summary Table of Changes" on page 7

26. 41210 Bridge Fails to train down in the Presence of a degraded lane

Problem: Problem:During the PCI Express training sequence, if a broken endpoint has correct receiver termination on a lane and transmits training sequences on the lane which are invalid, the 41210 Bridge will fail to link train.

Implication: The PCI Express specification intends that, if some lanes are transmitting bogus data instead of valid training sequences, those lanes should be treated as broken, and the link should fail down to an acceptable width, such as x1. If Lane 0 were failing in this manner, the PCI-E specification would anticipate that the link would fail to train. If a higher-numbered lane were failing in this manner, the PCI-E specification requires that the link attempt to train as a x1 on lane 0. In either case, 41210 Bridge will not train for the problem scenario.

On production material, failures are anticipated to be either a broken transmitter path or a broken receiver path, or a silent transmitter. 41210 Bridge will train properly for these failure modes, since either the receiver termination will be missing, or the transmitted signals will not be seen at the 41210 Bridge. In order to see invalid transmitted data on lanes at the 41210 Bridge, either a logic bug in the other PCI-E endpoint would be required, or a signal integrity issue so severe as to make operation impossible, such as a broken or intermittent connection.

Workaround: None. A non-compliant or broken device could exhibit this erratum.

Status: No Fix. See the "Summary Table of Changes" on page 7

27. PCI Express and PCI-X Header Logs and First Error Pointers do not remain sticky through reset.

The PCI Express and PCI-X header logs and First Error pointers are not maintaining their values after a warm/hot reset. These registers should be unaffected by a warm/hot reset, but instead, they are reset to default values. The following registers with "sticky" bits are affected: ADVERR_CTL (offset 118h), HDR_LOG (offset 11Ch), PCIXERRUNC_PTR (offset 138h), PCIXHDR_LOG (offset 13Ch).

Implication: Errors detected will be logged and escalated properly, but after a warm/hot reset, the header logs and first error pointers will reset to their default values.

Note: Error status registers are unaffected, and properly maintain their values through reset.

Workaround: None at this time.

Status: No Fix. See the "Summary Table of Changes" on page 7

28. Incorrect Default Value for PCI Express Flow Control Protocol Error Severity Bit.

Problem: The PCI Express Flow Control Error Severity bit, register offset 10C, bit 13, is programmed to a default value of 0, indicating an uncorrectable flow control error will be reported as non-fatal. This is in contradiction with the PCI Express Specification, which requires a default value of 1, indicating an uncorrectable flow control error will be reported as fatal.

Implication: Implications for this erratum depend upon the error response strategy implemented in a specific system.

This bit can be reprogrammed to match the specified default value if desired. Refer to the *Intel® 41210 Serial to Parallel PCI Bridge Initialization by the SMB Bus Using The PIC16F876A Microcontroller White Paper (302281)* for details on this workaround.

Status: No Fix. See the "Summary Table of Changes" on page 7.

29. Power State Bits in PCI Express Power Management Control/Status Register mistakenly accept reserved values.

Problem: The Power State bits, bit 1:0 of PM_PMCSR (Offset 70h) will allow a reserved value of 01 or 10 to be written. This is contrary to the specification, which originally stated that if software attempted to

write an unsupported reserved state to this field, the data would be discarded and no state change would occur.

Implication: If a reserved state is written to this field, there will be a mismatch between the actual power state of the part and the state reported in configuration space. In some cases, writing a reserved value to this field could cause the 41210 Bridge to transition to the D0 power state, regardless of the previous power state.

Workaround: Never write a reserved value to this bit field.

Status: No Fix. See the "Summary Table of Changes" on page 7.

30. Performance across an Upstream x1 PCI Express Link is less than expected.

Problem: When the 41210 Bridge is configured with an upstream x1 PCI Express link, the realized performance is significantly less than the predicted linear assumption that a x1 link will provide ¼ the performance of a x4 link. This is caused by circumstances where 41210 Bridge must discard a large portion of the data it receives across the upstream link. Notably; anytime 41210 Bridge services an incorrect prefetch, or anytime 41210 Bridge services interleaved requests from multi-function devices, 41210 Bridge must discard data.

Implication: Devices that rely heavily on prefetching, or multi-function devices that request data in an interleaved fashion are the most likely to experience degraded performance.

Workaround: System designers should reduce the amount of prefetching allowed to devices behind 41210 Bridge if possible.

Status: No Fix. See the "Summary Table of Changes" on page 7

31. SKP Ordered Set may not be sent within required interval during link recovery if a packet is pending

Problem: During Link Recovery on the PCI Express port, the device may fail to transmit a SKP Ordered set within the required time interval as defined in the PCI Express 1.0a Specification if a TLP or DLLP was pending when the link entered Recovery.Idle state.

Implication: If the receiving device depends upon receipt of a SKP Ordered set to progress through Link Recovery, a timeout will occur resulting in Link Down and automatic reinitialization of the PCI Express Link. A link transitions through Recovery only under exceptional operational conditions. Following the Link Recovery timeout and reinitialization, the PCI Express link should resume normal operation unless the original Link Recovery condition was entered as a result of a hard failure mechanism.

Workaround: None.

Status: No Fix. See the "Summary Table of Changes" on page 7.

Specification Changes

1. Ball pad T24 changes from an NC (No Connect NC17) to a pin that requires an external pull-up resistor

Issue: Pin NC17 previously had an internal pull-up resistor; this internal pull-up resistor is now removed. In normal operating mode, this pin must be tied high. To prevent this pin from floating, an external pull-up resistor to 3.3 V must be provided.

Affected Docs: Intel® 41210 Serial to Parallel PCI Bridge Datasheet (278885-001)
Intel® 41210 Serial to Parallel PCI Bridge Developer's Manual (278890-001)
Intel® 41210 Serial to Parallel PCI Bridge Design Guide (278801-001)

2. L0s state is not supported

Issue: The L0s state has been defeatured in the 41210 Bridge.

Affected Docs: Intel® 41210 Serial to Parallel PCI Bridge Datasheet (278885-001)
Intel® 41210 Serial to Parallel PCI Bridge Developer's Manual (278890-001)
Intel® 41210 Serial to Parallel PCI Bridge Design Guide (278801-001)

3. Linear Voltage Regulators are Recommended for 1.5 V supplies

Issue: Linear Voltage regulators are recommended when using 1.5 Volt power supplies.

Affected Docs: Intel® 41210 Serial to Parallel PCI Bridge Design Guide (278801-001)

4. Updated Power Sequencing Steps for VCC15 and VCC33 Voltages

Issue: The following three steps are the power sequencing requirements that must be followed with the 41210 Bridge:

1. The 41210 Bridge requires that the VCC33 voltage rail be no less than 0.5V below VCC15 (absolute voltage value) at all times during 41210 operation, including during system power up and power down. In other words, the following must always be true:

   VCC33 >= (VCC15 – 0.5V)

   This can be accomplished by placing a diode (with a voltage drop <0.5V) between VCC15 and VCC33. A node will be connected to VCC15 and cathode will be connected to VCC33.

   If VCC15 (1.5V PCI-X I/O voltage) and VCC (1.5V core voltage) are tied together on the platform, then both voltages must meet the above rule.

Note: Linear voltage regulators are recommended when using 1.5 Volt power supplies.

2. If a voltage regulator solution is used which shunts VCC15 to ground while VCC33 is powered, the maximum allowable time that VCC15 can be shunted to ground while VCC33 is fully powered is 20ms. This includes configurations where VCC and VCC15 are powered by the same power source.

3. The maximum allowed time between VCC33 and VCC15 ramping is 525ms.

Note: There is no minimum sequencing time requirement other than requirements in Steps 2 and 3.

Affected Docs: Intel® 41210 Serial to Parallel PCI Bridge Design Guide (278801-001)

5. Use Microcontroller When Implementing Some Erratum Workarounds

Issue: The workarounds for a number of erratum observed in the 41210 Serial to Parallel PCI Bridge (Erratum 19, 20, and 23) require that Configuration Space registers be loaded with specific values. Intel requires that this be done using the microcontroller attached to the 41210 Bridge SM Bus prior to releasing the CFGRETRY signal.

Affected Docs: Intel® 41210 Serial to Parallel PCI Bridge Developer's Manual (278890-001)
Intel® 41210 Serial to Parallel PCI Bridge Design Guide (278801-001)

6. BCNF Bit 3 Changed to Reserved bit

Issue: Bit 3 in the Bridge Configuration Register (Offset 40 in both A- and B- bridges) is currently defined as 'Downstream Delayed Transaction Resource Partitioning (ODTP)' with a default setting of '0'. Setting this bit to '1' may cause undesired functionality; therefore BCNF.3 is changed to 'reserved'. As a 'reserved' bit, the default condition of '0' should be maintained and BIOS firmware should never set this bit to a '1'.

Affected Docs: Intel® 41210 Serial to Parallel PCI Bridge Developer's Manual (278890-001)

Specification Clarifications

None for this revision of this specification update.

Documentation Changes

1. L0s state is not supported.

Issue: The L0s state has been defeatured in the 41210 Bridge.

Affected Docs: Intel® 41210 Serial to Parallel PCI Bridge Datasheet (278885-001)
Intel® 41210 Serial to Parallel PCI Bridge Developer's Manual (278890-001)
Intel® 41210 Serial to Parallel PCI Bridge Design Guide (278801-001)

2. Removed; incorporated into Design Guide

3. Removed; incorporated into Design Guide

4. Offset 40h: BCNF - Bridge Configuration Register Bit 3 Changed to Reserved

Issue: In Section 12.2.21, Table 55, Bit 3 in the Bridge Configuration Register (Offset 40) is currently defined as Downstream Delayed Transaction Resource Partitioning (ODTP) with a default setting of '0'. Setting this bit to '1' may cause undesired functionality; therefore BCNF Bit 3 is changed to 'reserved'. As a 'reserved' bit, the default condition of '0' should be maintained and BIOS firmware should never set this bit to a '1'.

The row in Table 55 containing the Bit 3 description now appears as follows:

3	RsvdP	0b	Preserved

Affected Docs: Intel® 41210 Serial to Parallel PCI Bridge Developer's Manual (278890-001)