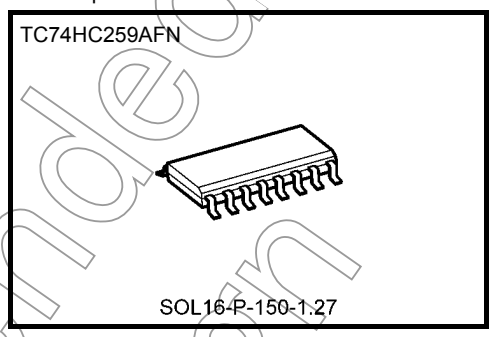
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC259AFN

8-Bit Addressable Latch

Note: xxxFN (JEDEC SOP) is not available in Japan.



Weight
SOL16-P-150-1.27 : 0.13 g (typ.)

The TC74HC259A is a high speed CMOS ADDRESSABLE LATCH fabricated with silicon gate C^2MOS technology.

It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The respective bits are controlled by address inputs A, B, and C. When $\overline{\text{CLEAR}}$ input is held high and enable input G is held low, the data is written into the bit selected by address inputs, the other bit hold their previous conditions.

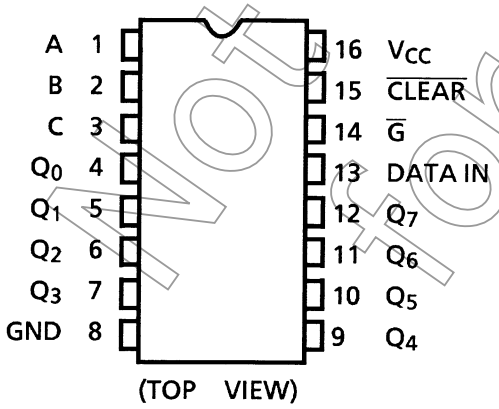
When both $\overline{\text{CLEAR}}$ and $\overline{\text{G}}$ held high, writing of all bits is inhibited regardless of adress inputs, and their previous condition are held. When $\overline{\text{CLEAR}}$ is held low and $\overline{\text{G}}$ is held high, all bits are resent to low regardless of the other inputs. When both of $\overline{\text{CLEAR}}$ and $\overline{\text{G}}$ held low, all bits which isn't selected by adress inputs are resent to low.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

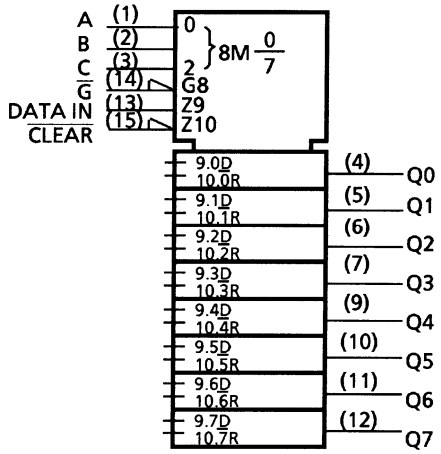
Features

- High speed: t_{pd} = 15 ns (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2~6 V
- Pin and function compatible with 74LS259

Pin Assignment



IEC Logic Symbol



Truth Table

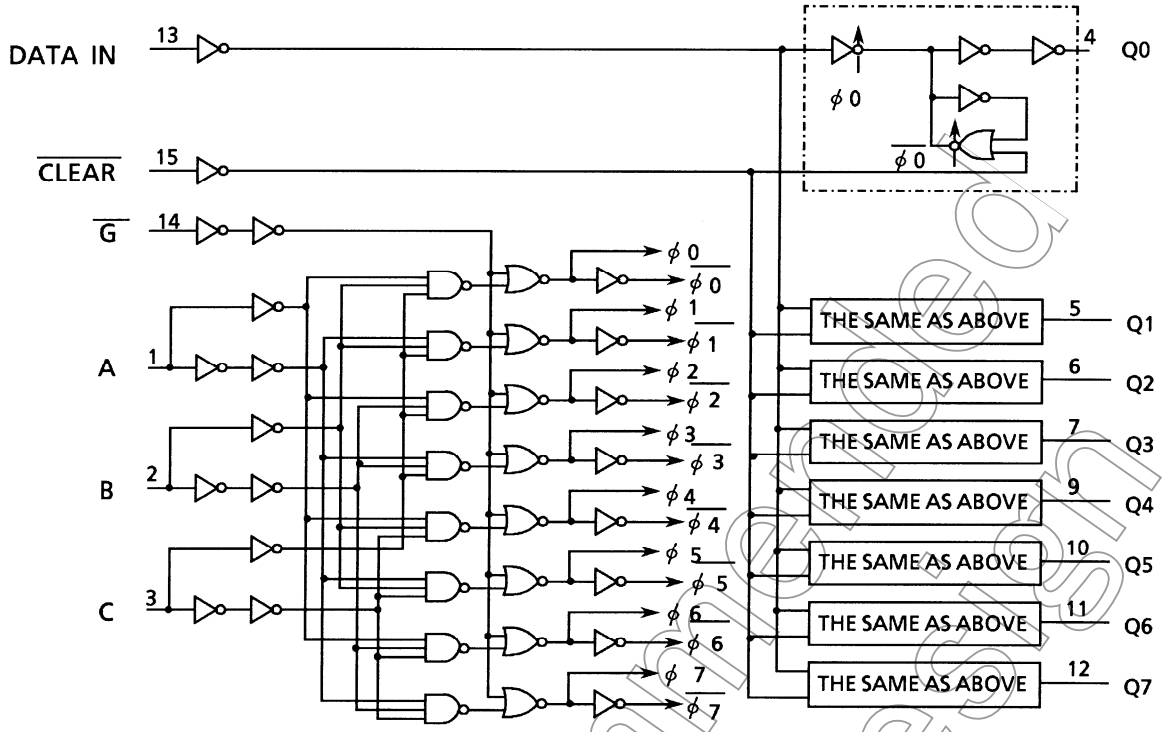
Inputs		Output of Addressed Latch	Each Other Output	Function
$\overline{CLEAR}$	$\overline{G}$			
H	L	D	QiO	Addressable Latch
H	H	QiO	QiO	Memory
L	L	D	L	8-Line Demultriplexer
L	H	L	L	Clear All Bits to “L”

Select Inputs			Latch Addressed
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D: The level at the data input.

QiO: The level before the indicared steady-state input conditions were established (i = 0, 1, ... 7)

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5~7.0	V
DC input voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2~6	V
Input voltage	V_{IN}	0~V_{CC}	V
Output voltage	V_{OUT}	0~V_{CC}	V
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	t_r, t_f	0~1000 (V_{CC} = 2.0 V) 0~500 (V_{CC} = 4.5 V) 0~400 (V_{CC} = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40~85°C		Unit
				V_{CC} (V)	Min	Typ.	Max	Min	Max	
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	
			I_{OH} = −5.2 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 ~85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width ($\overline{G}$)	$t_{W(L)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($\overline{CLEAR}$)	$t_{W(L)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (DATA)	t_s	—	2.0	—	50	60	ns
			4.5	—	10	12	
			6.0	—	9	11	
Minimum set-up time (A, B, C)	t_s	—	2.0	—	25	30	ns
			4.5	—	5	6	
			6.0	—	5	5	
Minimum hold time (DATA)	t_h	—	2.0	—	25	30	ns
			4.5	—	5	6	
			6.0	—	5	5	
Minimum hold time (A, B, C)	t_h	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	

AC Characteristics ($C_L = 15$ pF, $V_{CC} = 5$ V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation delay time (DATA-Q)	t_{pLH} t_{pHL}	—	—	15	22	ns
Propagation delay time (A, B, C-Q)	t_{pLH} t_{pHL}	—	—	21	32	ns
Propagation delay time ($\overline{G}$ -Q)	t_{pLH} t_{pHL}	—	—	16	28	ns
Propagation delay time ($\overline{CLEAR}$ -Q)	t_{pHL}	—	—	13	23	ns

AC Characteristics (C_L = 50 pF, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40~85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (DATA-Q)	t_{pLH} t_{pHL}	—	2.0	—	56	130	—	165	ns
			4.5	—	18	26	—	33	
			6.0	—	15	22	—	28	
Propagation delay time (A, B, C-Q)	t_{pLH} t_{pHL}	—	2.0	—	83	185	—	230	ns
			4.5	—	25	37	—	46	
			6.0	—	21	31	—	39	
Propagation delay time ($\overline{G}$-Q)	t_{pLH} t_{pHL}	—	2.0	—	67	165	—	205	ns
			4.5	—	20	33	—	41	
			6.0	—	17	28	—	35	
Propagation delay time ($\overline{CLEAR}$-Q)	t_{pHL}	—	2.0	—	52	135	—	170	ns
			4.5	—	16	27	—	34	
			6.0	—	14	23	—	29	
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD} (Note)	—		—	35	—	—	—	pF

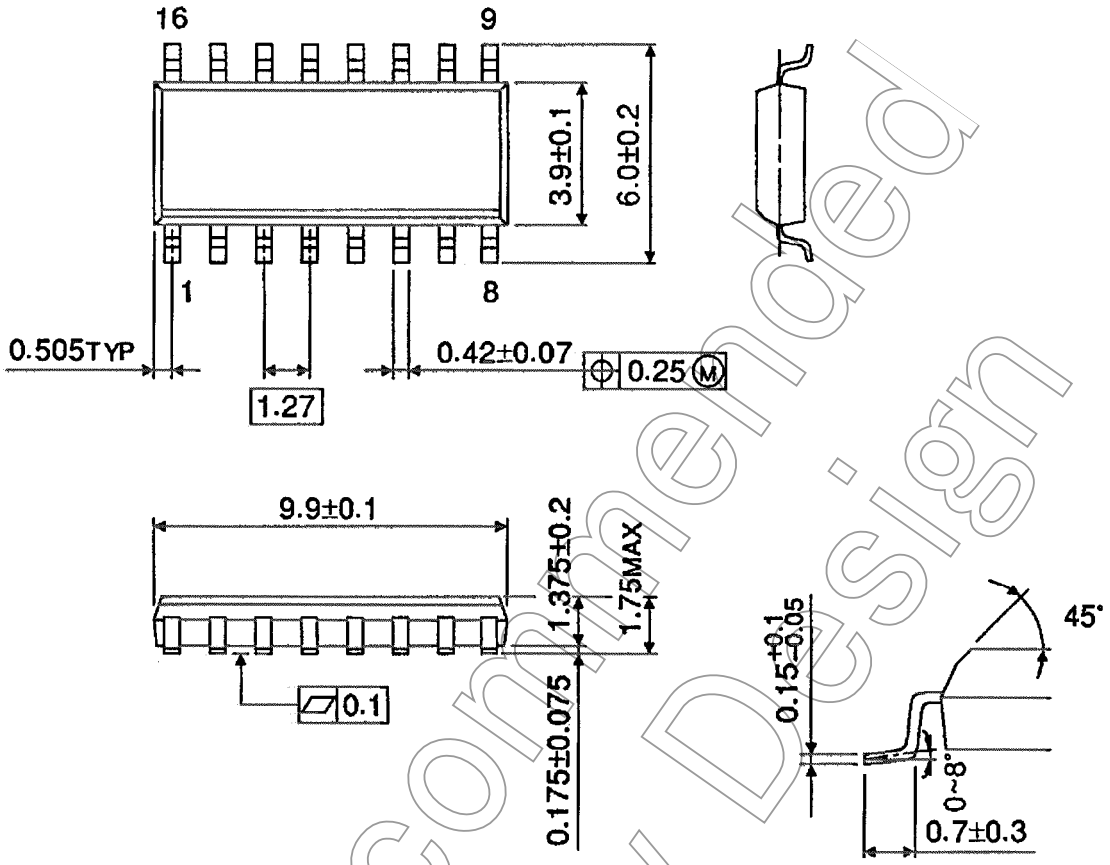
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Package Dimensions (Note)

SOL16-P-150-1.27 Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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