

# SN5472, SN7472 AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

SDLS117 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

## description

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave

The logical states of the J and K inputs must not be allowed to change when the clock pulse is in a high state.

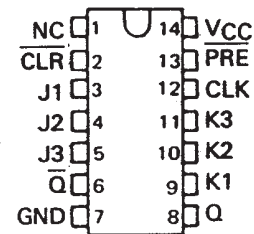
The SN5472, and the SN54H72 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7472 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

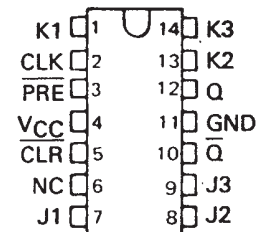
INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	$H^{\dagger}$	$H^{\dagger}$
H	H	$\square$	L	L	$Q_0$	$\bar{Q}_0$
H	H	$\square$	H	L	H	L
H	H	$\square$	L	H	L	H
H	H	$\square$	H	H	TOGGLE	TOGGLE

$\dagger$  This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

SN5472 . . . J PACKAGE  
SN7472 . . . N PACKAGE  
(TOP VIEW)

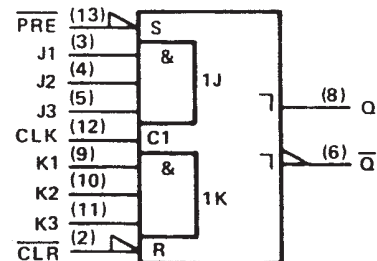


SN5472 . . . W PACKAGE  
(TOP VIEW)



NC - No internal connection

## logic symbol†



$\dagger$  This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J and N packages.

## positive logic

$$J = J1 \cdot J2 \cdot J3$$

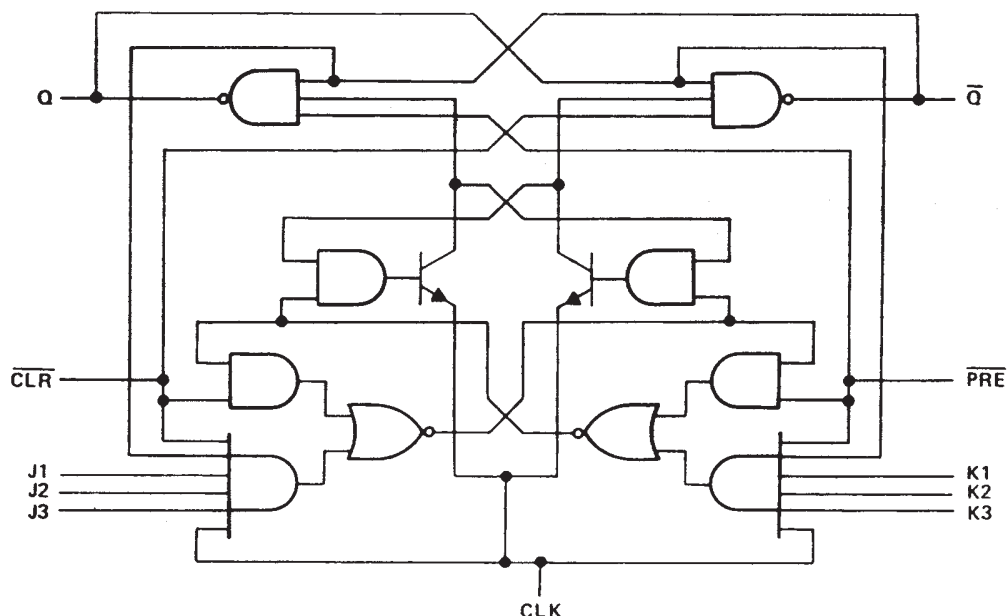
$$K = K1 \cdot K2 \cdot K3$$

# SN5472, SN7472

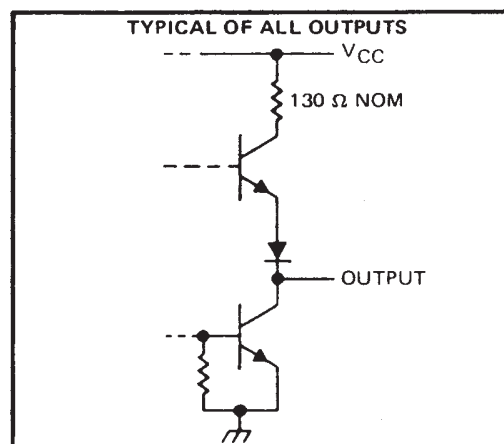
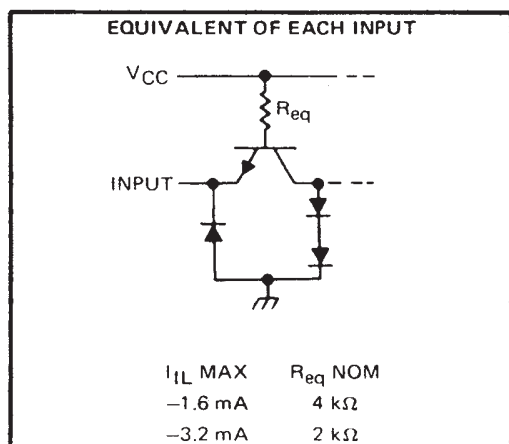
## AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

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### logic diagram (positive logic)



### schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

# SN5472, SN7472

## AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

SDLS117 – DECEMBER 1983 – REVISED MARCH 1988

### recommended operating conditions

		SN5472			SN7472			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>OH</sub>	High-level output current			− 0.4			− 0.4	mA
I <sub>OL</sub>	Low-level output current			16			16	mA
t <sub>w</sub>	Pulse duration	CLK high		20	20		ns	
		CLK low		47	47			
		PRE or CLR		25	25			
t <sub>su</sub>	Input setup time before CLK ↑	0		0		ns		
t <sub>h</sub>	Input hold time-data after CLK ↓	0		0		ns		
T <sub>A</sub>	Operating free-air temperature	− 55		125		0 70 °C		

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †		SN5472			SN7472			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$		$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$				– 1.5			– 1.5	V
$V_{OH}$		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$		2.4	3.4		2.4	3.4		V
$V_{OL}$		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$			0.2	0.4		0.2	0.4	V
$I_I$		$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$				1			1	mA
$I_{IH}$	J or K	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$				40			40	$\mu\text{A}$
	All other					80			80	
$I_{IL}$	J or K	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$				– 1.6			– 1.6	mA
	All other					– 3.2			– 3.2	
$I_{OS}§$		$V_{CC} = \text{MAX}$		– 20		– 57	– 18		– 57	mA
$I_{CC}$		$V_{CC} = \text{MAX}, \text{ See Note 2}$			10	20		10	20	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open,  $I_{CC}$  is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>			R <sub>L</sub> = 400 Ω,                      C <sub>L</sub> = 15 pF	15	20		MHz
t <sub>PLH</sub>	PRE or CLR	Q or Q̄			16	25	ns
t <sub>PHL</sub>					25	40	ns
t <sub>PLH</sub>					16	25	ns
t <sub>PHL</sub>	CLK	Q or Q̄			25	40	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN5472J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN7472N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7472N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7472N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7472N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SNJ5472J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ5472J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ5472W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SNJ5472W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



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  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
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  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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4040083/F 03/03

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W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



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N (R-PDIP-T\*\*)

16 PINS SHOWN

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MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
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		Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>