

M5M27C202K, JK-10, -12, -15

2097152-BIT(131072-WORD BY 16-BIT)
CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

The Mitsubishi M5M27C202K, JK is a high-speed 2097152-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M27C202K, JK is fabricated by N-channel double polysilicon gate for Memory and CMOS technology for peripheral circuits, and is available in a 40 pin DIP or 44 pin CLCC with a transparent lid.

FEATURES

- 131072 word × 16 bit organization
- Access time
 - M5M27C202K-10, JK-10 100ns (max.)
 - M5M27C202K-12, JK-12 120ns (max.)
 - M5M27C202K-15, JK-15 150ns (max.)
- Two line control \overline{OE} , \overline{CE}
- Low power current (I_{cc}): Active 30mA (max.)
(I_{sbz}): Stand-by 0.1mA (max.)
- Single 5V power supply (read operation)
- Programming voltage 12.5V
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 40 pin DIP
- Word programming algorithm
- Page programming algorithm

APPLICATION

Microcomputer systems and peripheral equipment

FUNCTION

Read

Set the \overline{CE} and \overline{OE} terminals to the read mode (low level). Low level input to \overline{CE} and \overline{OE} and address signals to the address inputs ($A_0 \sim A_{16}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_{15}$). When the \overline{CE} or \overline{OE} signal is high, data input/output are in a floating state.

When the \overline{CE} signal is high, the device is in the stand by mode or power-down mode.

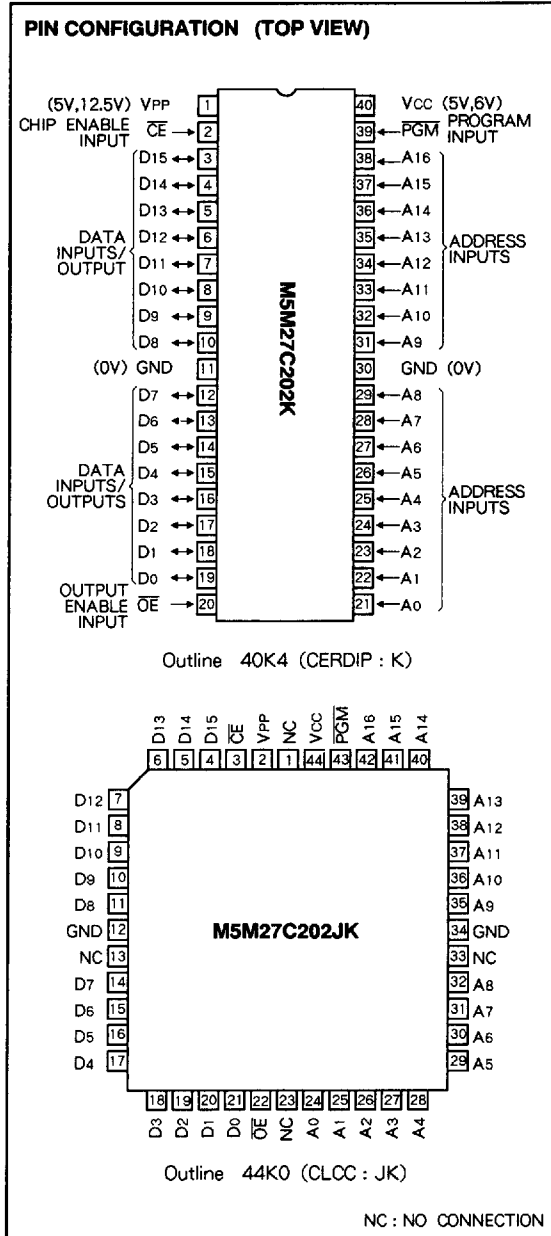
Programming

(Word programming algorithm)

The M5M27C202K, JK enters the word programming mode when 12.5V is supplied to the V_{PP} power supply input, \overline{CE} is at low level and \overline{OE} is at high level. A location is designated by address signals ($A_0 \sim A_{16}$), and the data to be programmed must be applied at 16-bits in parallel to the data inputs ($D_0 \sim D_{15}$). In this state, word programming is completed when \overline{PGM} is at low level.

(Page programming algorithm)

Page programming feature of the M5M27C202K, JK allows 2 words of data to be simultaneously programmed. The destination addresses for a page programming operation must reside on the same page; that is, A_1 through A_{16} must not change. At first, the M5M27C202K, JK enters the page data latch mode when $V_{PP} = 12.5V$, $\overline{CE} = "H"$, $\overline{OE} = "L"$ and $\overline{PGM} =$



H". A first and second locations in same page are designated by address signals ($A_0 \sim A_{16}$), and the data to be programmed must be applied to each location at 16-bits in parallel to the data inputs ($D_0 \sim D_{15}$). In this state, the data (2 words) latch is completed. Then the M5M27C202K, JK enters the page programming mode when $\overline{OE} = "H"$. In this state, page (2 words) programming is completed when $\overline{PGM} = "L"$.

Erase

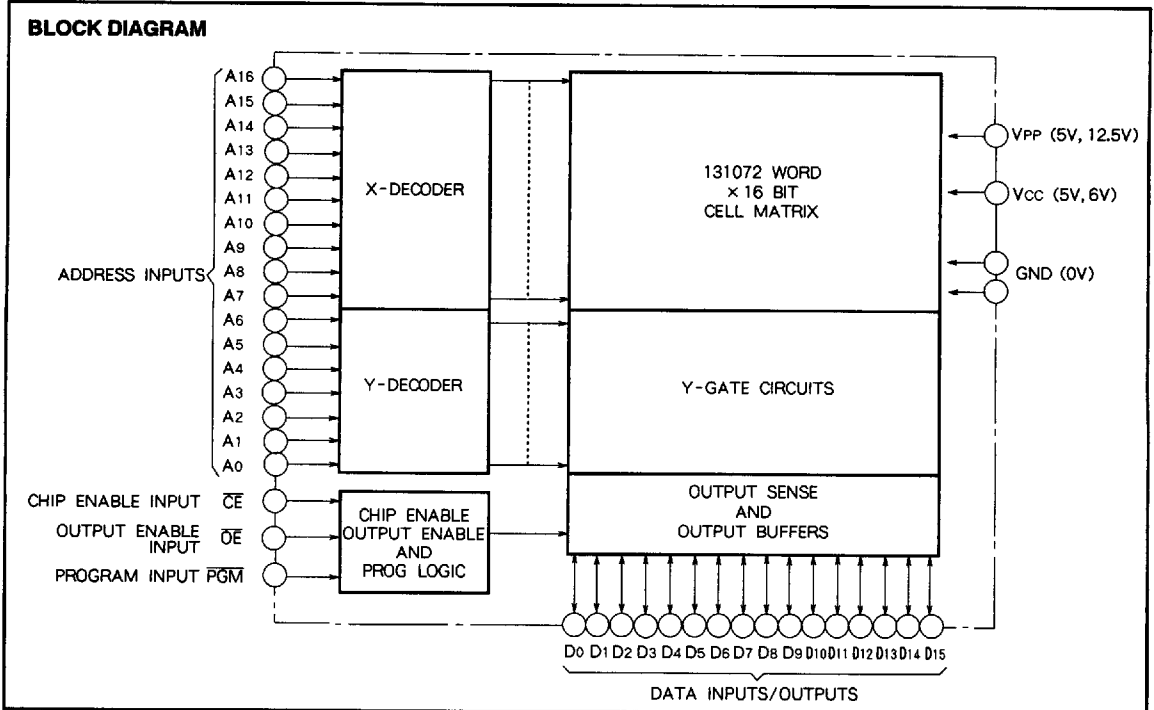
Erase is effected by exposure to ultraviolet light with a wavelength of 2537 Å at an intensity of approximately

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15WS/cm². Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any

operation in the read mode, the transparent lid should be covered with opaque tape.



MODE SELECTION

Mode	Pins (K/JK)	\overline{CE} (2/3)	\overline{OE} (20/22)	\overline{PGM} (39/43)	V_{PP} (1/2)	V_{CC} (40/44)	Data I/O (3~10, 12~19/4~11, 14~21)
Read		V_{IL}	V_{IL}	X*	5V	5V	Data out
Output disable		V_{IL}	V_{IH}	X*	5V	5V	Floating
Stand-by (Power down)		V_{IH}	X*	X*	5V	5V	Floating
Word program		V_{IL}	V_{IH}	V_{IL}	12.5V	6V	Data in
Program verify		V_{IL}	V_{IL}	V_{IH}	12.5V	6V	Data out
Page data latch		V_{IH}	V_{IL}	V_{IH}	12.5V	6V	Data in
Page program		V_{IH}	V_{IH}	V_{IL}	12.5V	6V	Floating
Program inhibit		V_{IL}	V_{IL}	V_{IL}	12.5V	6V	Floating
		V_{IL}	V_{IH}	V_{IH}	12.5V	6V	
		V_{IH}	V_{IL}	V_{IL}	12.5V	6V	
		V_{IH}	V_{IH}	V_{IH}	12.5V	6V	

* : X can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Conditions	Ratings	Unit
V_{I1}	All input or output voltage except $V_{PP} \cdot A_9$	With respect to Ground	- 0.6~7	V
V_{I2}	V_{PP} supply voltage		- 0.6~14.0	V
V_{I3}	A_9 supply voltage		- 0.6~13.5	V
T_{opr}	Operating temperature		- 10~80	°C
T_{stg}	Storage temperature		- 65~125	°C

Note 1 : Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

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READ OPERATION

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, Vpp = Vcc, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
ILI	Input leakage current	VIN = 0~Vcc			10	μA
ILO	Output leakage current	VOUT = 0~Vcc			10	μA
IPPI	VPP current read/stand-by	VPP = Vcc = 5.5V		1	100	μA
ISB1	Vcc current stand-by	CE = VIH			1	mA
ISB2		CE = Vcc		1	100	μA
ICC1	Vcc current Active	CE = OE = VIL, DC, IOUT = 0mA			30	mA
ICC2		CE = VIL, f = 10MHz, IOUT = 0mA			30	mA
VIL	Input low voltage		-0.1		0.8	V
VIH	Input high voltage		2.2		Vcc + 1	V
VOL	Output low voltage	IOL = 2.1mA			0.45	V
VOH	Output high voltage	Ioh = -400 μA	2.4			V

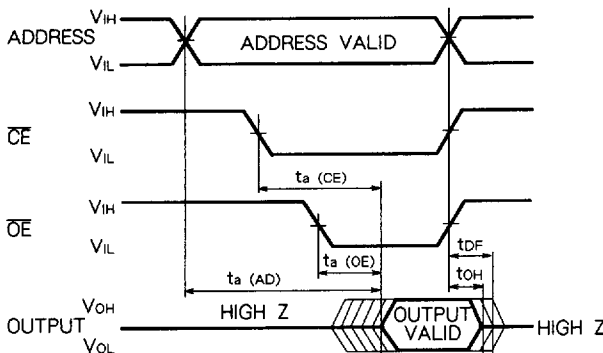
Note 2: Typical values are at Ta = 25°C and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, Vpp = Vcc, unless otherwise noted)

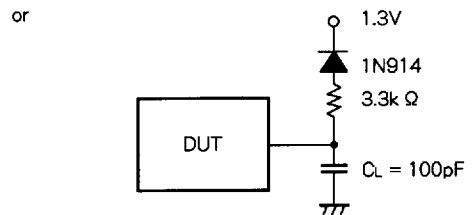
Symbol	Parameter	Test conditions	Limits						Unit
			M5M27C202K-10		M5M27C202K-12		M5M27C202K-15		
			Min	Max	Min	Max	Min	Max	
ta (AD)	Address to output delay	CE = OE = VIL		100		120		150	ns
ta (CE)	CE to output delay	OE = VIL		100		120		150	ns
ta (OE)	OE to output delay	CE = VIL		50		60		60	ns
tDF	OE high to output float	CE = VIL	0	45	0	50	0	50	ns
tOH	Output hold from CE,OE or address		0		0		0		ns

Note 3: Vcc must be applied simultaneously VPP and removed simultaneously VPP.

AC WAVEFORMS



Test conditions A.C characteristics
Input voltage : VIL = 0.45V , VIH = 2.4V
Input rise and fall times : ≤ 10ns
Reference voltage at timing measurement : 1.5V
Output load : 1TTL gate + CL (= 100pF)



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CIN	Input capacitance (Address,CE,OE,PGM)	Ta = 25°C, f = 1MHz, Vi = Vo = 0V			15	pF
COUT	Output capacitance				15	pF

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PROGRAM OPERATION

WORD PROGRAMMING ALGORITHM

First set $V_{CC} = 6V$, $V_{PP} = 12.5V$ and then set an address to first address to be programmed. After applying 0.2ms program pulse (PGM) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 0.2ms program pulse. The programmer continues 0.2ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains

its total number of 0.2ms pulse applied to that address in register X. And then applied a program pulse X times of 0.2ms width as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. When the entire addresses have been programmed completely, all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

DC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5^\circ C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I _{LI}	Input leakage current	$V_{IN} = 0 \sim V_{CC}$			10	μA
V _{OL}	Output low voltage (verify)	$I_{OL} = 2.1mA$			0.45	V
V _{OH}	Output high voltage (verify)	$I_{OH} = -400 \mu A$				V
V _{IL}	Input low voltage		-0.1		0.8	V
V _{IH}	Input high voltage		2.2		V_{CC}	V
I _{CC}	V_{CC} supply current				30	mA
I _{PP}	V_{PP} supply current	PGM = V _{IL}			50	mA

AC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5^\circ C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$, unless otherwise noted)

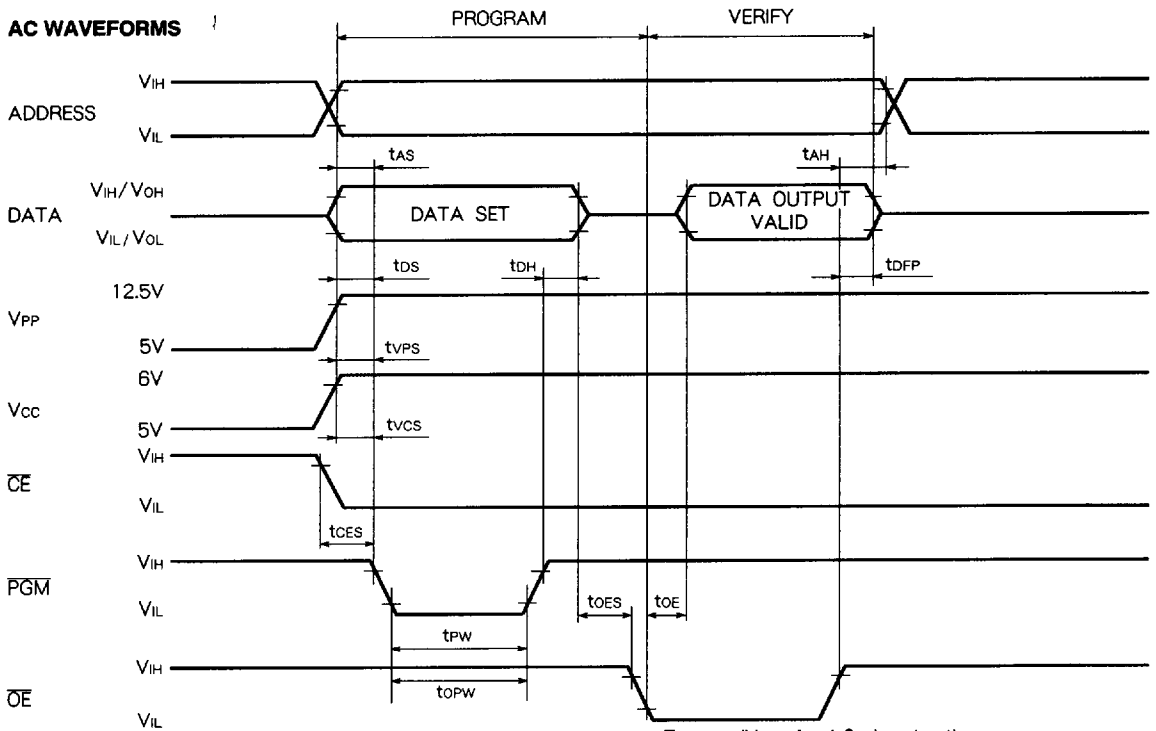
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{AS}	Address setup time		2			μs
t _{oES}	\overline{OE} setup time		2			μs
t _{DS}	Data setup time		2			μs
t _{AH}	Address hold time		0			μs
t _{DH}	Data hold time		2			μs
t _{DFP}	Chip enable to output float delay		0		130	ns
t _{VCS}	V_{CC} setup time		2			μs
t _{VPS}	V_{PP} setup time		2			μs
t _{PW}	PGM initial program pulse width		0.19	0.2	0.21	ms
t _{OPW}	PGM over program pulse width		0.19		5.25	ms
t _{CES}	\overline{CE} setup time		2			μs
t _{oE}	Data valid from \overline{OE}				150	ns

Note 4: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP} .

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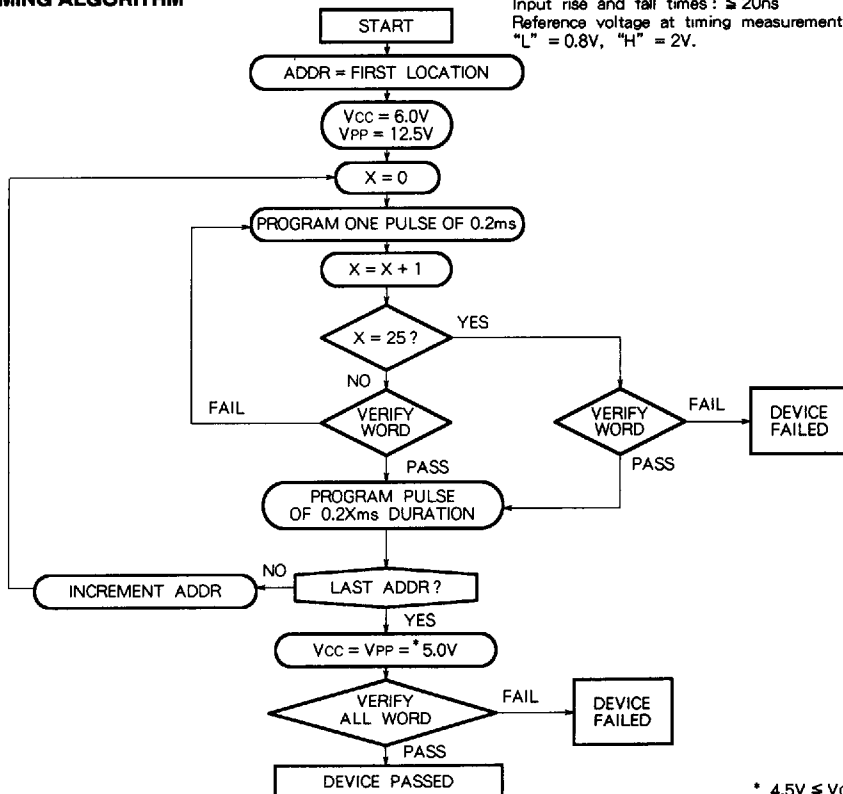
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AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: $V_{IL} = 0.45V$, $V_{IH} = 2.4V$
Input rise and fall times: $\leq 20ns$
Reference voltage at timing measurement: Input, Output
"L" = 0.8V, "H" = 2V.

WORD PROGRAMMING ALGORITHM FLOW CHART



* 4.5V \leq VCC = VPP \leq 5.5V

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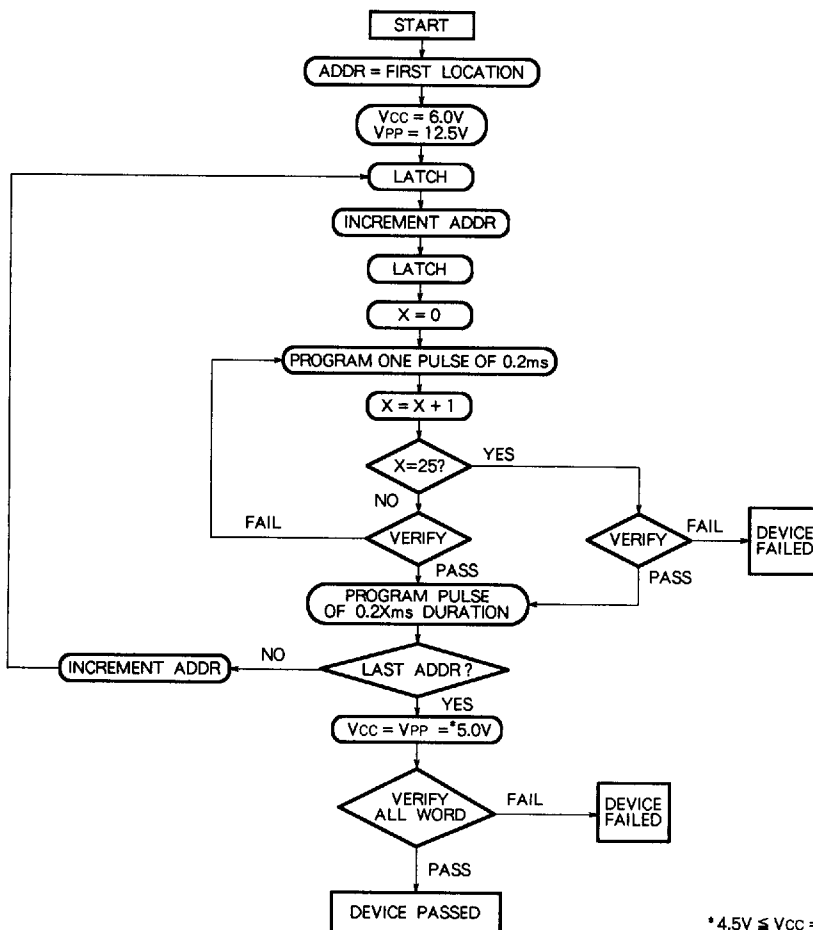
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PAGE PROGRAMMING ALGORITHM

First set $V_{CC} = 6V$, $V_{PP} = 12.5V$ and then set an address to first page address to be programmed. After data of 2 words are latched, these latch data are programmed simultaneously by applying 0.2ms program pulse. Then a verify is performed. If each output data is not verified correctly, apply one more 0.2ms program pulse. The programmer continues 0.2ms pulse-then-verify routines until each output data is verified correctly or twenty five of these pulse-then-verify routines have been completed.

The programmer also maintains its total number of 0.2ms pulse applied to that page addresses in register X. And then applied a program pulse X times of 0.2ms width as an overprogram pulse. When the programming procedure above is finished, step to the next page address and repeat this procedure till last page address to be programmed. When the entire page addresses have been programmed completely, all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

**PAGE PROGRAMMING ALGORITHM
FLOW CHART**



* 4.5V ≤ V_{CC} = V_{PP} ≤ 5.5V

DC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input leakage current	$V_{IN} = 0 \sim V_{CC}$			10	μA
V_{OL}	Output low voltage (verify)	$I_{OL} = 2.1\text{mA}$			0.45	V
V_{OH}	Output high voltage (verify)	$I_{OH} = -400\ \mu\text{A}$	2.4			V
V_{IL}	Input low voltage		-0.1		0.8	V
V_{IH}	Input high voltage		2.2		V_{CC}	V
I_{CC}	V_{CC} supply current				30	mA
I_{PP}	V_{PP} supply current	$PGM = V_{IL}$			100	mA

AC ELECTRICAL CHARACTERISTICS ($T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$, unless otherwise noted)

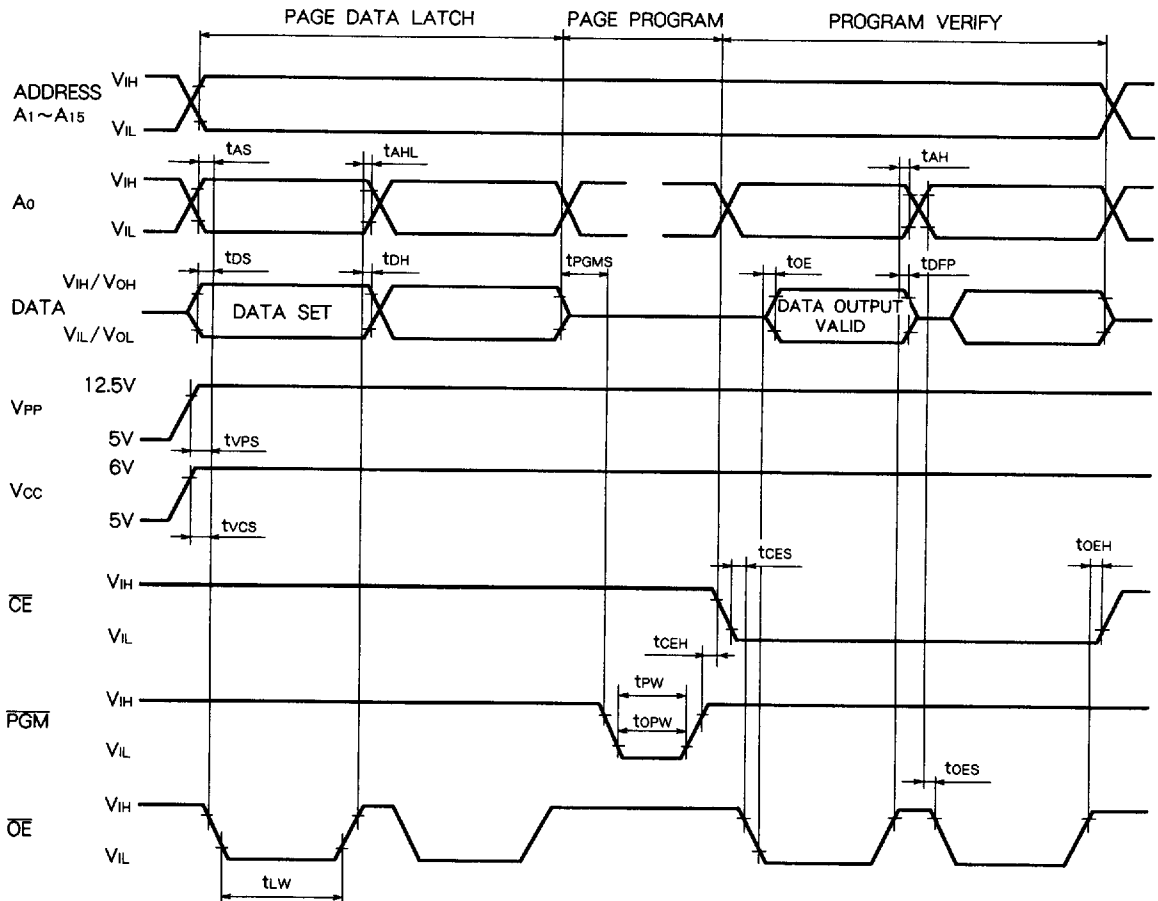
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	\overline{OE} setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{AHL}			2			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	\overline{OE} to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{PW}	PGM initial program pulse width		0.19	0.2	0.21	ms
t_{OPW}	PGM over program pulse width		0.19		5.25	ms
t_{CES}	\overline{CE} setup time		2			μs
t_{OE}	Data valid from \overline{OE}				150	ns
t_{LW}	Data latch time		1			μs
t_{PGMS}	PGM setup time		2			μs
t_{CEH}	\overline{CE} hold time		2			μs
t_{OEH}	\overline{OE} hold time		2			μs

Note 5: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP} .

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AC WAVEFORMS



Test condition for A.C characteristics
 Input voltage : $V_{IL} = 0.45V, V_{IH} = 2.4V$
 Input rise and fall time : (10%~90%) : $\leq 20ns$
 Reference voltage at timing measurement : Input, Output "L" = 0.8V, "H" = 2V.

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DEVICE IDENTIFIER MODE

The Device Identifier Mode allows the reading of a binary code from the EPROM that identifies the manufacturer and device type.

The EPROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

M5M27C202K, JK DEVICE IDENTIFIER CODE

Code \ Pin	A ₀ (21/24)	D ₁₅ (3/4)	D ₁₄ (4/5)	D ₁₃ (5/6)	D ₁₂ (6/7)	D ₁₁ (7/8)	D ₁₀ (8/9)	D ₉ (9/10)	D ₈ (10/11)	D ₇ (12/14)	D ₆ (13/15)	D ₅ (14/16)	D ₄ (15/17)	D ₃ (16/18)	D ₂ (17/19)	D ₁ (18/20)	D ₀ (19/21)	Hex Data
Manufacturer code	V _{IL}	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	001C
Device code	V _{IH}	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	000B

Note 6: A₉ = 12.0 ± 0.5V

A₁~A₈, A₁₀~A₁₆, \overline{CE} , \overline{OE} = V_{IL}, \overline{PGM} = V_{IH}

V_{CC} = V_{PP} = 5V ± 10%