



# BUK7880-55

## N-channel TrenchMOS standard level FET

Rev. 3 — 21 April 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- AEC Q101 compliant
- Electrostatically robust due to integrated protection diodes
- Low conduction losses due to low on-state resistance

### 1.3 Applications

- Automotive and general purpose power switching

### 1.4 Quick reference data

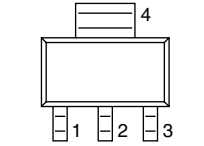
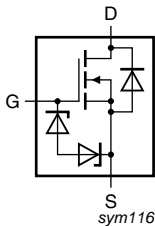
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	55	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$	-	-	7.5	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; $T_{amb} = 25\text{ °C}$	-	-	1.8	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$	-	65	80	mΩ
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 2.5\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; $R_{GS} = 50\text{ Ω}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped	-	-	30	mJ



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT223 (SOT223)	 sym116
2	D	drain		
3	S	source		
4	D	mounting base; connected to drain		

## 3. Ordering information

Table 3. Ordering information

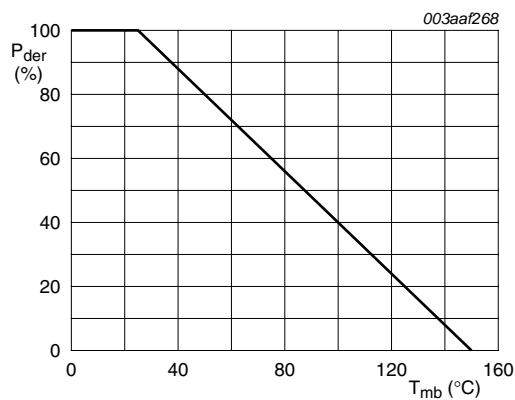
Type number	Package		
	Name	Description	Version
BUK7880-55	SOT223	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

## 4. Limiting values

Table 4. Limiting values

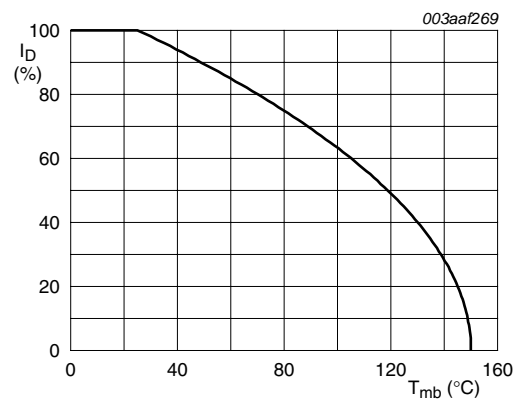
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$ ; $T_j \leq 150\text{ }^{\circ}\text{C}$	-	55	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$V_{GS}$	gate-source voltage		-16	16	V
$I_D$	drain current	$T_{amb} = 25\text{ }^{\circ}\text{C}$	-	3.5	A
		$T_{sp} = 25\text{ }^{\circ}\text{C}$	-	7.5	A
		$T_{amb} = 100\text{ }^{\circ}\text{C}$	-	2.2	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}$ ; pulsed	-	40	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ }^{\circ}\text{C}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	1.8	W
		$T_{sp} = 25\text{ }^{\circ}\text{C}$	-	8.3	W
$T_{stg}$	storage temperature		-55	150	$^{\circ}\text{C}$
$T_j$	junction temperature		-55	150	$^{\circ}\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current	$T_{sp} = 25\text{ }^{\circ}\text{C}$	-	7.5	A
$I_{SM}$	peak source current	pulsed; $T_{sp} = 25\text{ }^{\circ}\text{C}$	-	40	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 2.5\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; unclamped	-	30	mJ
<b>Electrostatic discharge</b>					
$V_{esd}$	electrostatic discharge voltage	HBM; $C = 100\text{ pF}$ ; $R = 1.5\text{ k}\Omega$	-	2	kV



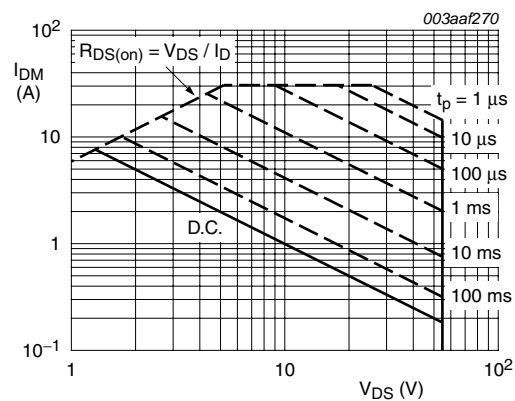
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



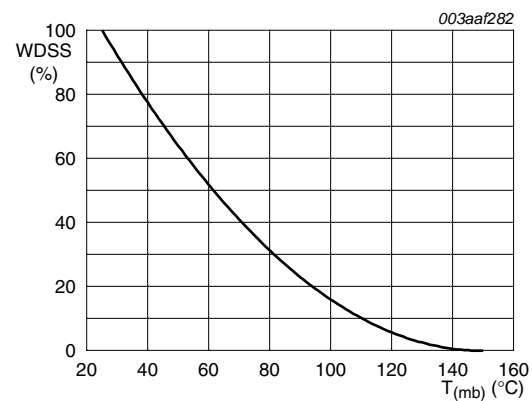
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



$T_{sp} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



$I_D = 2.5\text{ A}$

Fig 4. Normalised drain-source non-repetitive avalanche energy as a function of mounting-base temperature

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on any printed-circuit board	-	12	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Mounted on FR4 PCB, mounting pad for drain 6.5 cm <sup>2</sup>	-	-	70	K/W

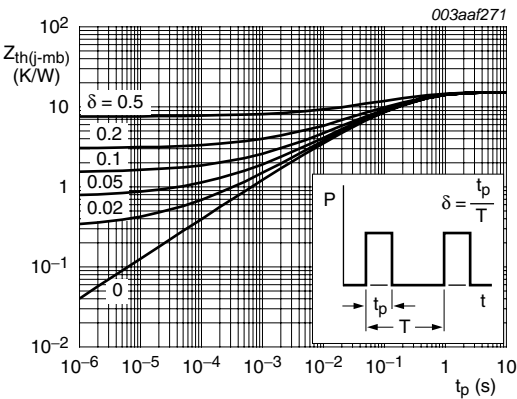


Fig 5. Transient thermal impedance from junction to solder point as a function of pulse duration

## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	55	-	-	V
		I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	50	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 150 °C	1.2	-	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C	2	3	4	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = -55 °C	-	-	4.4	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 55 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.05	10	μA
		V <sub>DS</sub> = 55 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 150 °C	-	-	100	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.04	1	μA
		V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.04	1	μA
		V <sub>GS</sub> = 10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 150 °C	-	-	10	μA
		V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 150 °C	-	-	10	μA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 5 A; T <sub>j</sub> = 150 °C	-	-	148	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 5 A; T <sub>j</sub> = 25 °C	-	65	80	mΩ
V <sub>(BR)GSS</sub>	gate-source breakdown voltage	V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C; I <sub>G</sub> = 1 mA	16	-	-	V
		V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C; I <sub>G</sub> = -1 mA	16	-	-	V
Dynamic characteristics						
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C	-	365	500	pF
C <sub>oss</sub>	output capacitance		-	110	135	pF
C <sub>rss</sub>	reverse transfer capacitance		-	60	85	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 4.3 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 10 Ω; T <sub>mb</sub> = 25 °C; I <sub>D</sub> = 7 A	-	9	14	ns
t <sub>r</sub>	rise time		-	15	25	ns
t <sub>d(off)</sub>	turn-off delay time		-	18	27	ns
t <sub>f</sub>	fall time		-	12	18	ns
g <sub>fs</sub>	transfer conductance	V <sub>DS</sub> = 25 V; I <sub>D</sub> = 5 A; T <sub>j</sub> = 25 °C	1	4	-	S
Source-drain diode						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 5 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> ≥ -55 °C; T <sub>j</sub> ≤ 175 °C	-	0.85	1.1	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 5 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 30 V; T <sub>j</sub> ≥ -55 °C; T <sub>j</sub> ≤ 175 °C	-	38	-	ns
Q <sub>r</sub>	recovered charge		-	0.2	-	μC

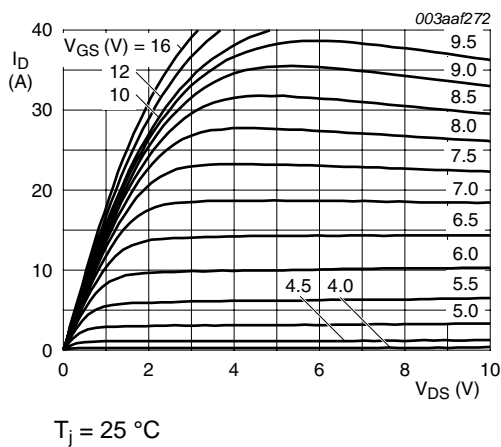


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

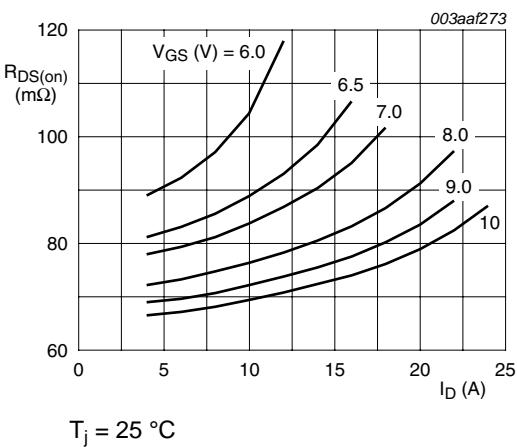


Fig 7. Drain-source on-state resistance as a function of drain current; typical values

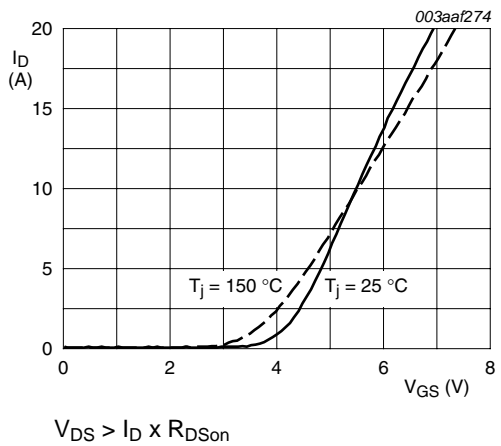


Fig 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

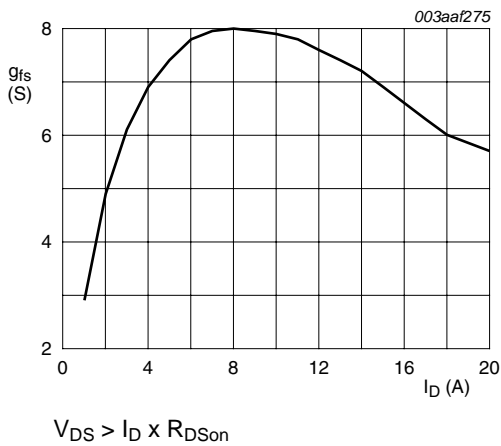
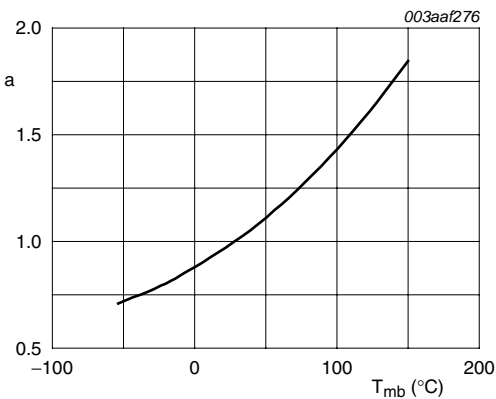


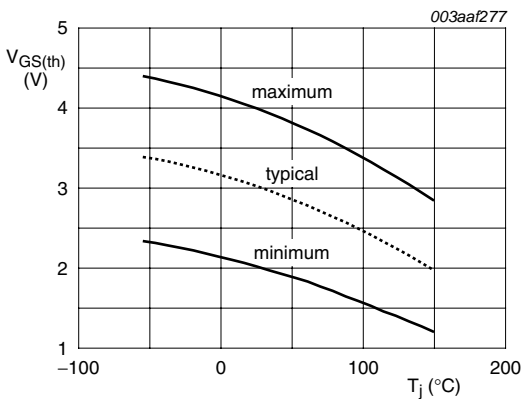
Fig 9. Forward transconductance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

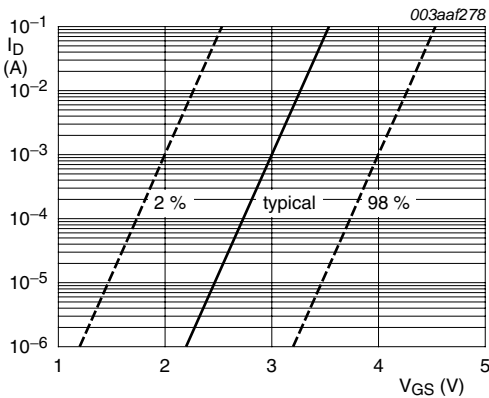
$I_D = 5\text{ A}; V_{GS} = 10\text{ V}$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



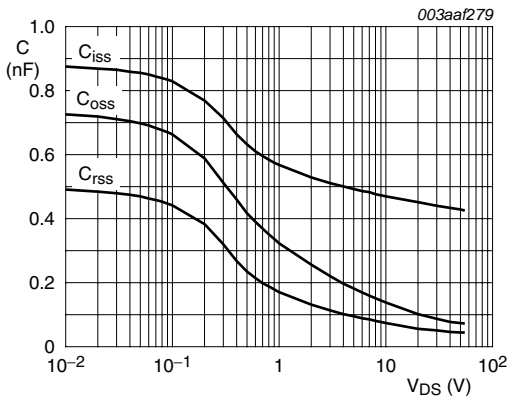
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$T_j = 25^{\circ}C; V_{DS} = V_{GS}$

Fig 12. Sub-threshold drain current as a function of gate-source voltage



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

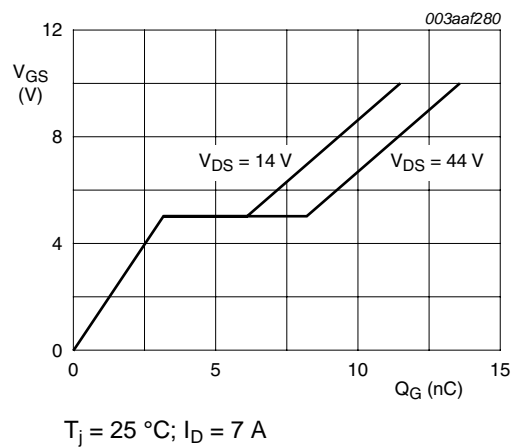


Fig 14. Gate-source voltage as a function of gate charge; typical values

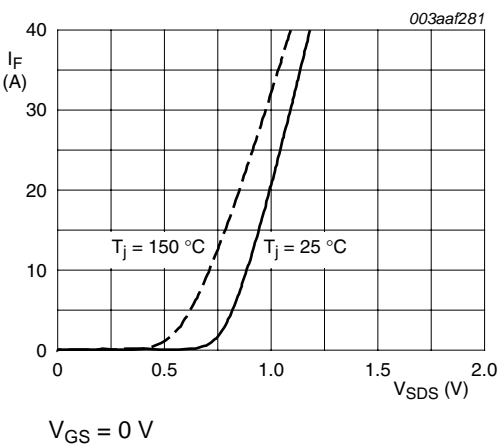


Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



7. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223

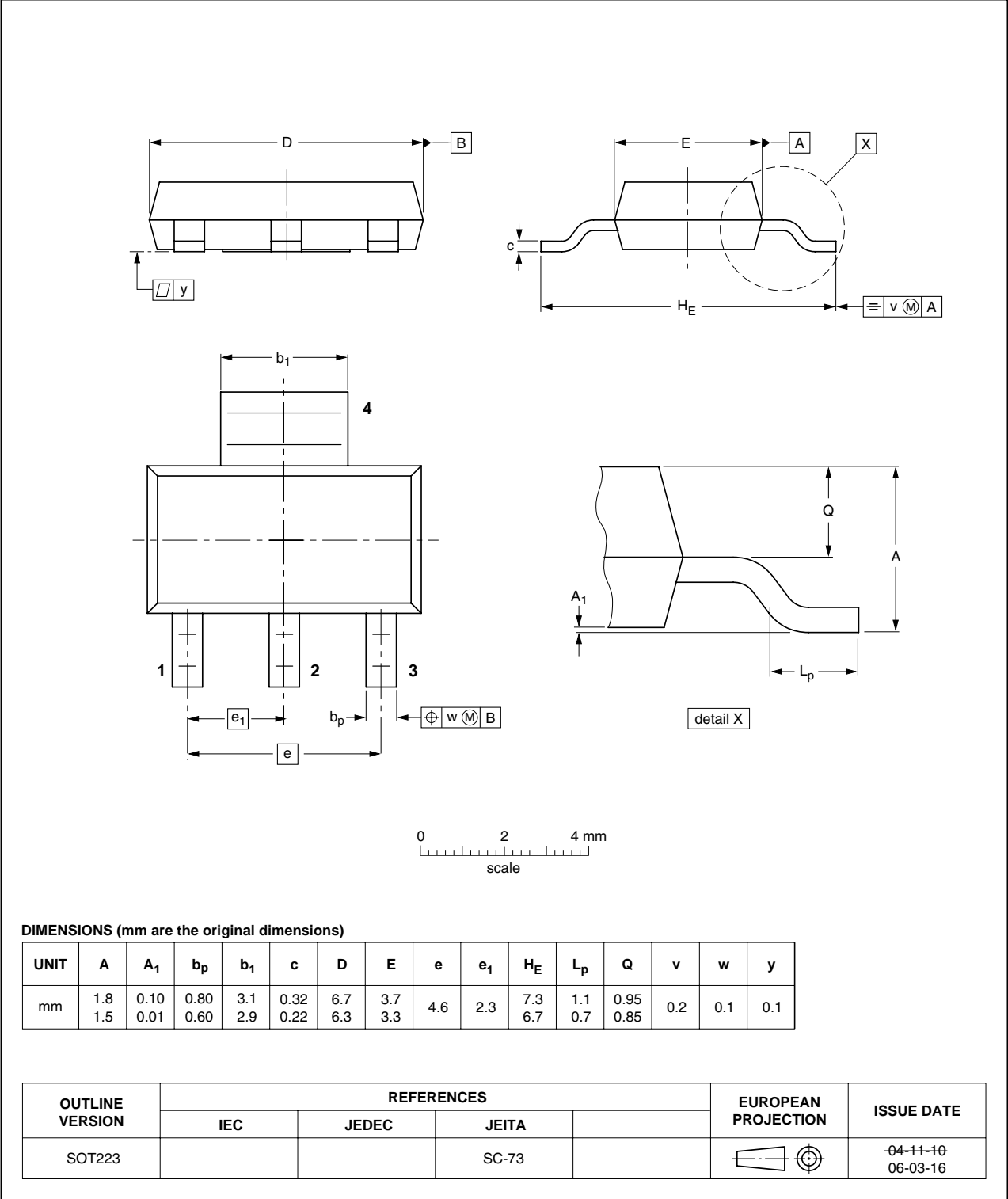


Fig 16. Package outline SOT223 (SOT223)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7880-55 v.3	20110421	Product data sheet	-	BUK7880-55_2
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>			
BUK7880-55_2	19980401	Product specification	-	-

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Document status <sup>[1] [2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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