TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM6N7002FU

High Speed Switching Applications Analog Switch Applications

Small package

• Low ON resistance : $R_{on} = 3.3 \Omega \text{ (max) } (@V_{GS} = 4.5 \text{ V})$

: R_{on} = 3.2 Ω (max) (@V_{GS} = 5 V)

: $R_{on} = 3.0 \Omega \text{ (max) (@V_{GS} = 10 V)}$

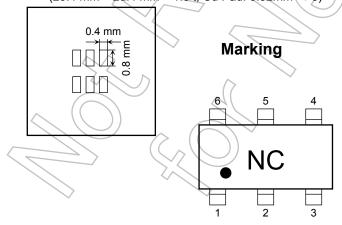
Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

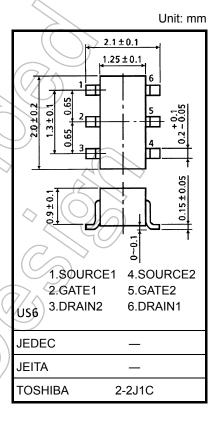
Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V_{DS}	60	V	
Gate-Source voltage		V_{GSS}	± 20	(A)	
Drain current	DC	ID	200	mA	
	Pulse	I _{DP}	800		
Drain power dissipation (Ta = 25°C)		P _D (Note 1)	300	mW	
Channel temperature		T _{ch}	150	> °C	
Storage temperature range		T _{stg}	-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

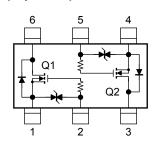
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating, mounted on FR4 board (25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.32mm² × 6





Equivalent Circuit (top view)



Handling Precaution

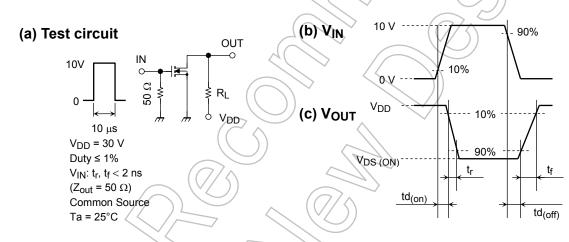
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Start of commercial production 2002-11

Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Test Condition	Min	Тур	Max	Unit	
Gate leakage current		I _{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$	_	_	± 10	μА	
Drain-Source breakdown voltage		V (BR) DSS	I _D = 0.1 mA, V _{GS} = 0	60	_	_	V	
Drain cut-off curre	nt	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0	/	_	1	μА	
Gate threshold vo	Itage	V _{th}	V _{DS} = 10 V, I _D = 0.25 mA	1.0	_	2.5	V	
Forward transfer a	admittance	Y _{fs}	V _{DS} = 10 V, I _D = 200 mA	170) /_	_	mS	
Drain-Source ON resistance		R _{DS} (ON)	I _D = 500 mA, V _{GS} = 10 V	7	2.0	3.0		
			I _D = 100 mA, V _{GS} = 5 V	\mathcal{C}	2.1	3.2	2 Ω	
			I _D = 100 mA, V _{GS} = 4.5 V		2.2	3.3		
Input capacitance		C _{iss}		_	17	_	pF	
Reverse transfer capacitance		C _{rss}	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz	_	1.4	_	pF	
Output capacitance		Coss			5.8	\rightarrow	pF	
Switching time	Turn-on delay time	td _(on)	V _{DD} = 30V, I _D = 200 mA,	-	2.4	4.0	20	
	Turn-off delay time	td _(off)	V _{GS} = 0 to 10V	(26	40	ns	

Switching Time Test Circuit

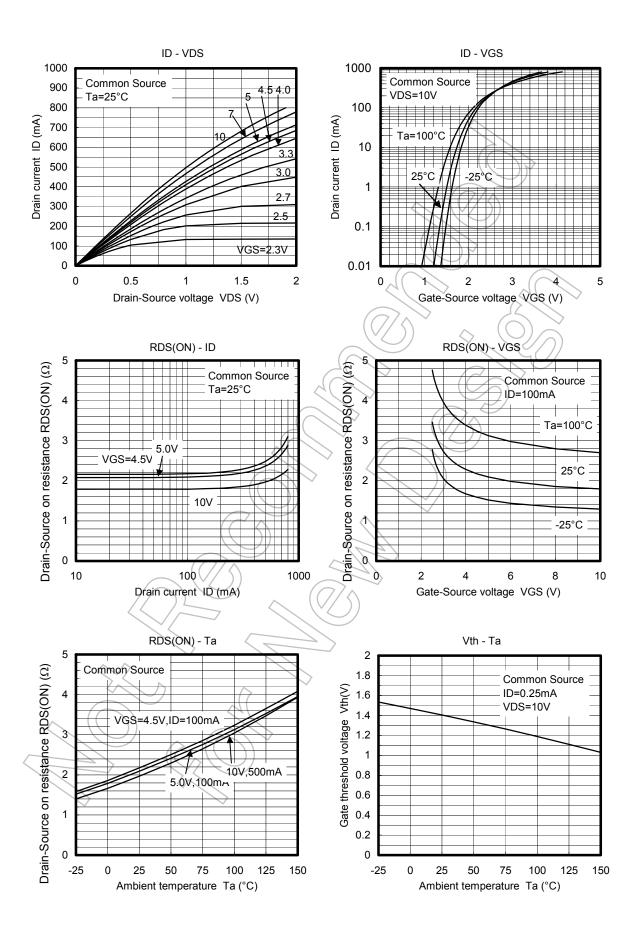


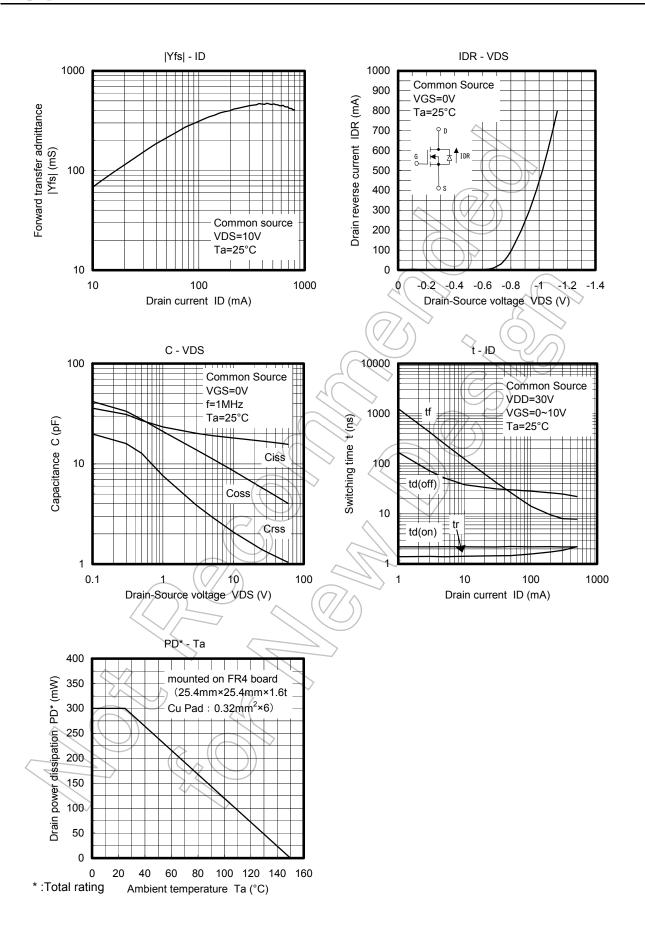
Precaution

 V_{th} can be expressed as voltage between gate and source when low operating current value is I_D =250 μ A for this product. For normal switching operation, V_{GS} (on) requires higher voltage than V_{th} and V_{GS} (off) requires lower voltage than V_{th} . (Relationship can be established as follows: V_{GS} (off) < V_{th} < V_{GS} (on))

Please take this into consideration for using the device.

2 2014-03-01





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