

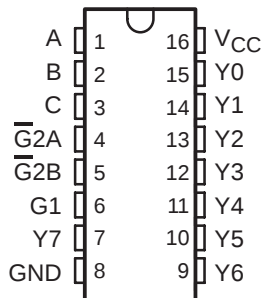
SN54HCT138, SN74HCT138 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

SCLS171E – MARCH 1984 – REVISED SEPTEMBER 2003

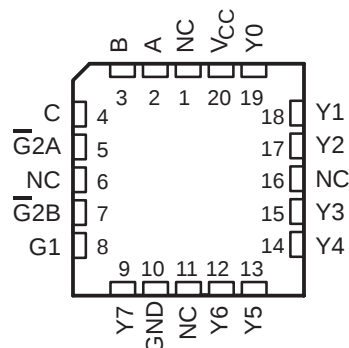
- Operating Voltage Range of 4.5 V to 5.5 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 17$ ns
- ± 4 -mA Output Drive at 5 V

- Low Input Current of 1 μ A Max
- Inputs Are TTL-Voltage Compatible
- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporate Three Enable Inputs to Simplify Cascading and/or Data Reception

SN54HCT138 . . . J OR W PACKAGE
SN74HCT138 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HCT138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'HCT138 devices are designed for high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, these decoders can minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HCT138N	SN74HCT138N
	SOIC – D	Tube of 40	SN74HCT138D	HCT138
		Reel of 2500	SN74HCT138DR	
		Reel of 250	SN74HCT138DT	
	SOP – NS	Reel of 2000	SN74HCT138NSR	HCT138
	TSSOP – PW	Tube of 90	SN74HCT138PW	HT138
		Reel of 2000	SN74HCT138PWR	
Reel of 250		SN74HCT138PWT		
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HCT138J	SNJ54HCT138J
	CFP – W	Tube of 150	SNJ54HCT138W	SNJ54HCT138W
	LCCC – FK	Tube of 55	SNJ54HCT138FK	SNJ54HCT138FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low ($\overline{G}$) and one active-high (G) enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L



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The logic diagram shows a 3-to-8 decoder implemented using NAND gates. The inputs are A (1), B (2), and C (3). The outputs are Y0 (15), Y1 (14), Y2 (13), Y3 (12), Y4 (11), Y5 (10), Y6 (9), and Y7 (7). The decoder is composed of two stages of NAND gates. The first stage has three inputs (A, B, C) and three outputs (G1, G2A, G2B). The second stage has three inputs (G1, G2A, G2B) and three outputs (Y0, Y1, Y2). The third stage has three inputs (Y0, Y1, Y2) and three outputs (Y3, Y4, Y5). The fourth stage has three inputs (Y3, Y4, Y5) and three outputs (Y6, Y7, Y8). The fifth stage has three inputs (Y6, Y7, Y8) and three outputs (Y9, Y10, Y11). The sixth stage has three inputs (Y9, Y10, Y11) and three outputs (Y12, Y13, Y14). The seventh stage has three inputs (Y12, Y13, Y14) and three outputs (Y15, Y16, Y17). The eighth stage has three inputs (Y15, Y16, Y17) and three outputs (Y18, Y19, Y20). The ninth stage has three inputs (Y18, Y19, Y20) and three outputs (Y21, Y22, Y23). The tenth stage has three inputs (Y21, Y22, Y23) and three outputs (Y24, Y25, Y26). The eleventh stage has three inputs (Y24, Y25, Y26) and three outputs (Y27, Y28, Y29). The twelfth stage has three inputs (Y27, Y28, Y29) and three outputs (Y30, Y31, Y32). The thirteenth stage has three inputs (Y30, Y31, Y32) and three outputs (Y33, Y34, Y35). The fourteenth stage has three inputs (Y33, Y34, Y35) and three outputs (Y36, Y37, Y38). The fifteenth stage has three inputs (Y36, Y37, Y38) and three outputs (Y39, Y40, Y41). The sixteenth stage has three inputs (Y39, Y40, Y41) and three outputs (Y42, Y43, Y44). The seventeenth stage has three inputs (Y42, Y43, Y44) and three outputs (Y45, Y46, Y47). The eighteenth stage has three inputs (Y45, Y46, Y47) and three outputs (Y48, Y49, Y50). The nineteenth stage has three inputs (Y48, Y49, Y50) and three outputs (Y51, Y52, Y53). The twentieth stage has three inputs (Y51, Y52, Y53) and three outputs (Y54, Y55, Y56). The twenty-first stage has three inputs (Y54, Y55, Y56) and three outputs (Y57, Y58, Y59). The twenty-second stage has three inputs (Y57, Y58, Y59) and three outputs (Y60, Y61, Y62). The twenty-third stage has three inputs (Y60, Y61, Y62) and three outputs (Y63, Y64, Y65). The twenty-fourth stage has three inputs (Y63, Y64, Y65) and three outputs (Y66, Y67, Y68). The twenty-fifth stage has three inputs (Y66, Y67, Y68) and three outputs (Y69, Y70, Y71). The twenty-sixth stage has three inputs (Y69, Y70, Y71) and three outputs (Y72, Y73, Y74). The twenty-seventh stage has three inputs (Y72, Y73, Y74) and three outputs (Y75, Y76, Y77). The twenty-eighth stage has three inputs (Y75, Y76, Y77) and three outputs (Y78, Y79, Y80). The twenty-ninth stage has three inputs (Y78, Y79, Y80) and three outputs (Y81, Y82, Y83). The thirtieth stage has three inputs (Y81, Y82, Y83) and three outputs (Y84, Y85, Y86). The thirty-first stage has three inputs (Y84, Y85, Y86) and three outputs (Y87, Y88, Y89). The thirty-second stage has three inputs (Y87, Y88, Y89) and three outputs (Y90, Y91, Y92). The thirty-third stage has three inputs (Y90, Y91, Y92) and three outputs (Y93, Y94, Y95). The thirty-fourth stage has three inputs (Y93, Y94, Y95) and three outputs (Y96, Y97, Y98). The thirty-fifth stage has three inputs (Y96, Y97, Y98) and three outputs (Y99, Y100, Y101). The thirty-sixth stage has three inputs (Y99, Y100, Y101) and three outputs (Y102, Y103, Y104). The thirty-seventh stage has three inputs (Y102, Y103, Y104) and three outputs (Y105, Y106, Y107). The thirty-eighth stage has three inputs (Y105, Y106, Y107) and three outputs (Y108, Y109, Y110). The thirty-ninth stage has three inputs (Y108, Y109, Y110) and three outputs (Y111, Y112, Y113). The fortieth stage has three inputs (Y111, Y112, Y113) and three outputs (Y114, Y115, Y116). The forty-first stage has three inputs (Y114, Y115, Y116) and three outputs (Y117, Y118, Y119). The forty-second stage has three inputs (Y117, Y118, Y119) and three outputs (Y120, Y121, Y122). The forty-third stage has three inputs (Y120, Y121, Y122) and three outputs (Y123, Y124, Y125). The forty-fourth stage has three inputs (Y123, Y124, Y125) and three outputs (Y126, Y127, Y128). The forty-fifth stage has three inputs (Y126, Y127, Y128) and three outputs (Y129, Y130, Y131). The forty-sixth stage has three inputs (Y129, Y130, Y131) and three outputs (Y132, Y133, Y134). The forty-seventh stage has three inputs (Y132, Y133, Y134) and three outputs (Y135, Y136, Y137). The forty-eighth stage has three inputs (Y135, Y136, Y137) and three outputs (Y138, Y139, Y140). The forty-ninth stage has three inputs (Y138, Y139, Y140) and three outputs (Y141, Y142, Y143). The fiftieth stage has three inputs (Y141, Y142, Y143) and three outputs (Y144, Y145, Y146). The fifty-first stage has three inputs (Y144, Y145, Y146) and three outputs (Y147, Y148, Y149). The fifty-second stage has three inputs (Y147, Y148, Y149) and three outputs (Y150, Y151, Y152). The fifty-third stage has three inputs (Y150, Y151, Y152) and three outputs (Y153, Y154, Y155). The fifty-fourth stage has three inputs (Y153, Y154, Y155) and three outputs (Y156, Y157, Y158). The fifty-fifth stage has three inputs (Y156, Y157, Y158) and three outputs (Y159, Y160, Y161). The fifty-sixth stage has three inputs (Y159, Y160, Y161) and three outputs (Y162, Y163, Y164). The fifty-seventh stage has three inputs (Y162, Y163, Y164) and three outputs (Y165, Y166, Y167). The fifty-eighth stage has three inputs (Y165, Y166, Y167) and three outputs (Y168, Y169, Y170). The fifty-ninth stage has three inputs (Y168, Y169, Y170) and three outputs (Y171, Y172, Y173). The sixtieth stage has three inputs (Y171, Y172, Y173) and three outputs (Y174, Y175, Y176). The sixty-first stage has three inputs (Y174, Y175, Y176) and three outputs (Y177, Y178, Y179). The sixty-second stage has three inputs (Y177, Y178, Y179) and three outputs (Y180, Y181, Y182). The sixty-third stage has three inputs (Y180, Y181, Y182) and three outputs (Y183, Y184, Y185). The sixty-fourth stage has three inputs (Y183, Y184, Y185) and three outputs (Y186, Y187, Y188). The sixty-fifth stage has three inputs (Y186, Y187, Y188) and three outputs (Y189, Y190, Y191). The sixty-sixth stage has three inputs (Y189, Y190, Y191) and three outputs (Y192, Y193, Y194). The sixty-seventh stage has three inputs (Y192, Y193, Y194) and three outputs (Y195, Y196, Y197). The sixty-eighth stage has three inputs (Y195, Y196, Y197) and three outputs (Y198, Y199, Y200). The sixty-ninth stage has three inputs (Y198, Y199, Y200) and three outputs (Y201, Y202, Y203). The seventieth stage has three inputs (Y201, Y202, Y203) and three outputs (Y204, Y205, Y206). The seventy-first stage has three inputs (Y204, Y205, Y206) and three outputs (Y207, Y208, Y209). The seventy-second stage has three inputs (Y207, Y208, Y209) and three outputs (Y210, Y211, Y212). The seventy-third stage has three inputs (Y210, Y211, Y212) and three outputs (Y213, Y214, Y215). The seventy-fourth stage has three inputs (Y213, Y214, Y215) and three outputs (Y216, Y217, Y218). The seventy-fifth stage has three inputs (Y216, Y217, Y218) and three outputs (Y219, Y220, Y221). The seventy-sixth stage has three inputs (Y219, Y220, Y221) and three outputs (Y222, Y223, Y224). The seventy-seventh stage has three inputs (Y222, Y223, Y224) and three outputs (Y225, Y226, Y227). The seventy-eighth stage has three inputs (Y225, Y226, Y227) and three outputs (Y228, Y229, Y230). The seventy-ninth stage has three inputs (Y228, Y229, Y230) and three outputs (Y231, Y232, Y233). The eightieth stage has three inputs (Y231, Y232, Y233) and three outputs (Y234, Y235, Y236). The eighty-first stage has three inputs (Y234, Y235, Y236) and three outputs (Y237, Y238, Y239). The eighty-second stage has three inputs (Y237, Y238, Y239) and three outputs (Y240, Y241, Y242). The eighty-third stage has three inputs (Y240, Y241, Y242) and three outputs (Y243, Y244, Y245). The eighty-fourth stage has three inputs (Y243, Y244, Y245) and three outputs (Y246, Y247, Y248). The eighty-fifth stage has three inputs (Y246, Y247, Y248) and three outputs (Y249, Y250, Y251). The eighty-sixth stage has three inputs (Y249, Y250, Y251) and three outputs (Y252, Y253, Y254). The eighty-seventh stage has three inputs (Y252, Y253, Y254) and three outputs (Y255, Y256, Y257). The eighty-eighth stage has three inputs (Y255, Y256, Y257) and three outputs (Y258, Y259, Y260). The eighty-ninth stage has three inputs (Y258, Y259, Y260) and three outputs (Y261, Y262, Y263). The ninetieth stage has three inputs (Y261, Y262, Y263) and three outputs (Y264, Y265, Y266). The ninety-first stage has three inputs (Y264, Y265, Y266) and three outputs (Y267, Y268, Y269). The ninety-second stage has three inputs (Y267, Y268, Y269) and three outputs (Y270, Y271, Y272). The ninety-third stage has three inputs (Y270, Y271, Y272) and three outputs (Y273, Y274, Y275). The ninety-fourth stage has three inputs (Y273, Y274, Y275) and three outputs (Y276, Y277, Y278). The ninety-fifth stage has three inputs (Y276, Y277, Y278) and three outputs (Y279, Y280, Y281). The ninety-sixth stage has three inputs (Y279, Y280, Y281) and three outputs (Y282, Y283, Y284). The ninety-seventh stage has three inputs (Y282, Y283, Y284) and three outputs (Y285, Y286, Y287). The ninety-eighth stage has three inputs (Y285, Y286, Y287) and three outputs (Y288, Y289, Y290). The ninety-ninth stage has three inputs (Y288,

3

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recommended operating conditions (see Note 3)

		SN54HCT138			SN74HCT138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$			2			V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$			0.8			V
V_I	Input voltage	0			V_{CC}			V
V_O	Output voltage	0			V_{CC}			V
$\Delta t/\Delta v$	Input transition rise/fall time	500			500			ns
T_A	Operating free-air temperature	-55			125			°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT138		SN74HCT138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}\text{ or }V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	4.5 V	4.4	4.499		4.4		4.4		V
		$I_{OH} = -4\text{ mA}$		3.98	4.3		3.7		3.84		
V_{OL}	$V_I = V_{IH}\text{ or }V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	4.5 V		0.001	0.1		0.1		0.1	V
		$I_{OL} = 4\text{ mA}$			0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}\text{ or }0$		5.5 V	± 0.1	± 100		± 1000		± 1000		nA
I_{CC}	$V_I = V_{CC}\text{ or }0, I_O = 0$		5.5 V			8	160		80		μA
$\Delta I_{CC}^\dagger$	One input at 0.5 V or 2.4 V, Other inputs at 0 or V_{CC}		5.5 V		1.4	2.4	3		2.9		mA
C_i			4.5 V to 5.5 V		3	10	10		10		pF

[†] This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC} .

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT138		SN74HCT138		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A, B, or C	Any Y	4.5 V		23	36		54		45	ns
			5.5 V		17	32		49		34	
	Enable	Any Y	4.5 V		22	33		50		42	
			5.5 V		18	30		45		38	
t_t		Y	4.5 V		12	15		22		19	ns
			5.5 V		11	14		20		17	

operating characteristics, $T_A = 25^\circ\text{C}$

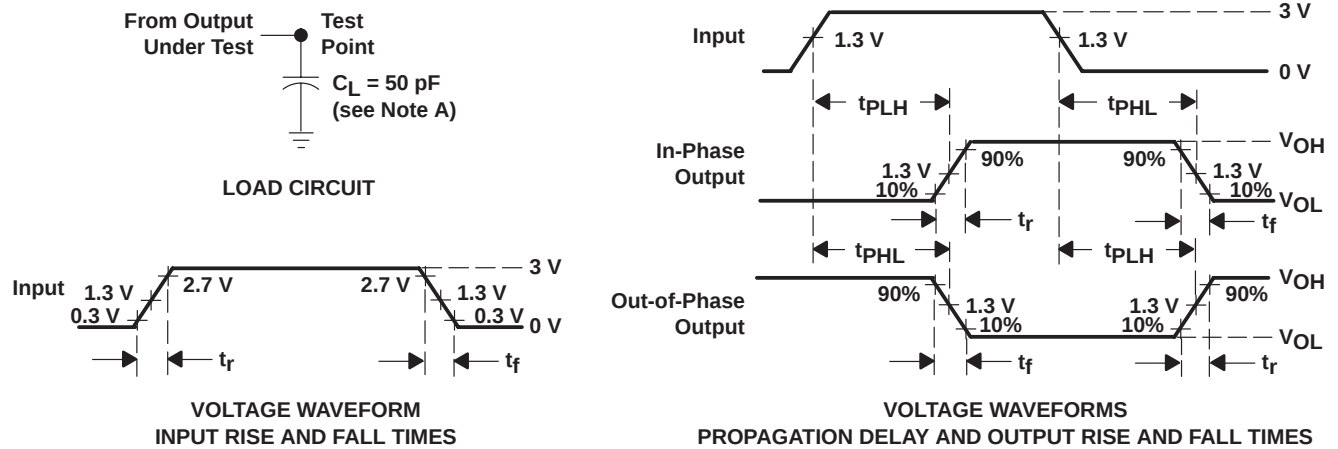
PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load	85	pF



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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. The outputs are measured one at a time with one input transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
85504012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	85504012A SNJ54HCT 138FK	Samples
8550401EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8550401EA SNJ54HCT138J	Samples
8550401FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8550401FA SNJ54HCT138W	Samples
JM38510/65852BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65852BEA	Samples
M38510/65852BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 65852BEA	Samples
SN54HCT138J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HCT138J	Samples
SN74HCT138D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT138	Samples
SN74HCT138DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT138	Samples
SN74HCT138DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT138	Samples
SN74HCT138DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	HCT138	Samples
SN74HCT138DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT138	Samples
SN74HCT138DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT138	Samples
SN74HCT138DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT138	Samples
SN74HCT138N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT138N	Samples
SN74HCT138N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	-40 to 85		
SN74HCT138NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HCT138N	Samples
SN74HCT138NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT138	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCT138NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT138	Samples
SN74HCT138PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT138	Samples
SN74HCT138PWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85		
SN74HCT138PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT138	Samples
SN74HCT138PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT138	Samples
SN74HCT138PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT138	Samples
SN74HCT138PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HT138	Samples
SNJ54HCT138FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	85504012A SNJ54HCT 138FK	Samples
SNJ54HCT138J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8550401EA SNJ54HCT138J	Samples
SNJ54HCT138W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54HCT138, SN74HCT138 :

- Catalog: [SN74HCT138](#)
- Military: [SN54HCT138](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCT138DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HCT138DR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74HCT138DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HCT138PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCT138PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



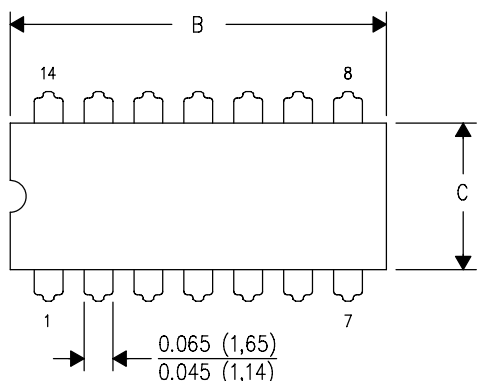
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCT138DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74HCT138DR	SOIC	D	16	2500	364.0	364.0	27.0
SN74HCT138DRG4	SOIC	D	16	2500	333.2	345.9	28.6
SN74HCT138PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74HCT138PWT	TSSOP	PW	16	250	367.0	367.0	35.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

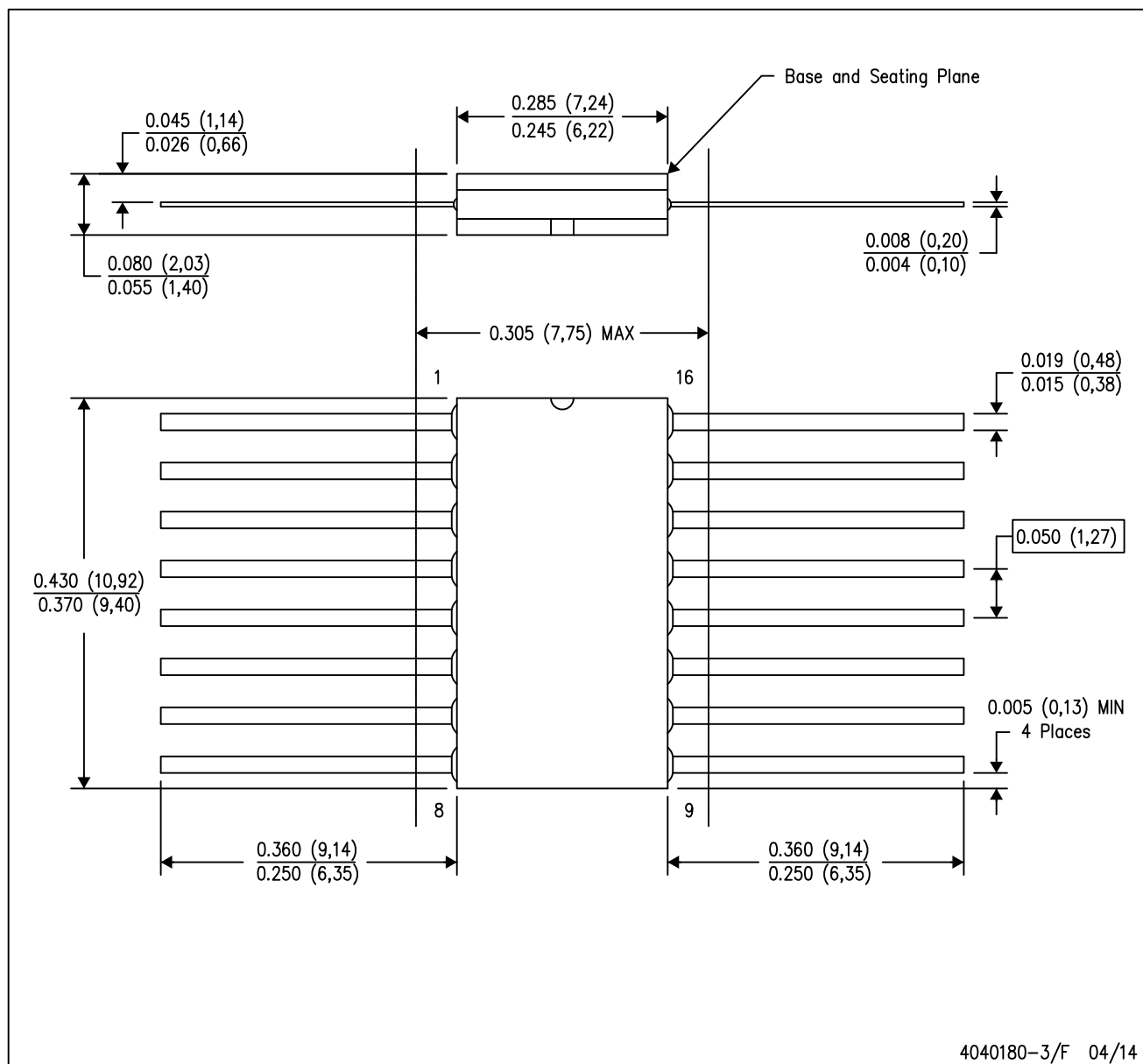


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

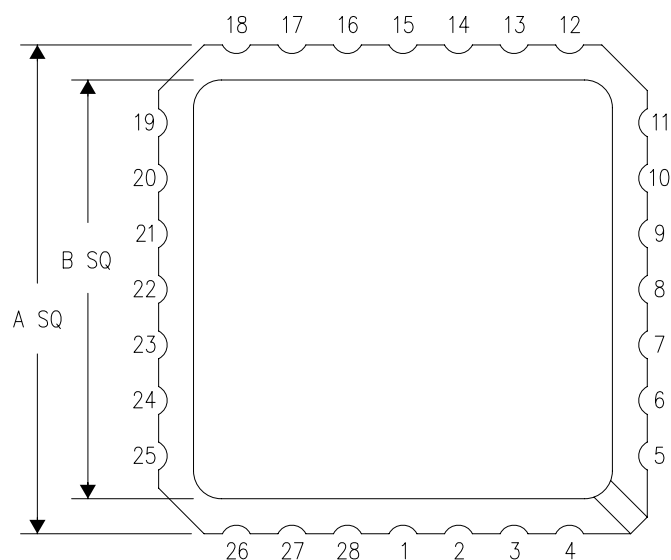


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP2-F16

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



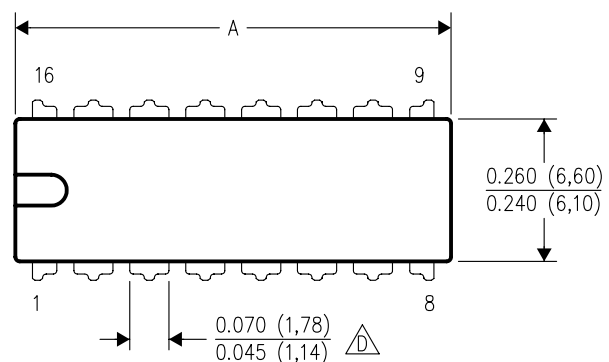
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

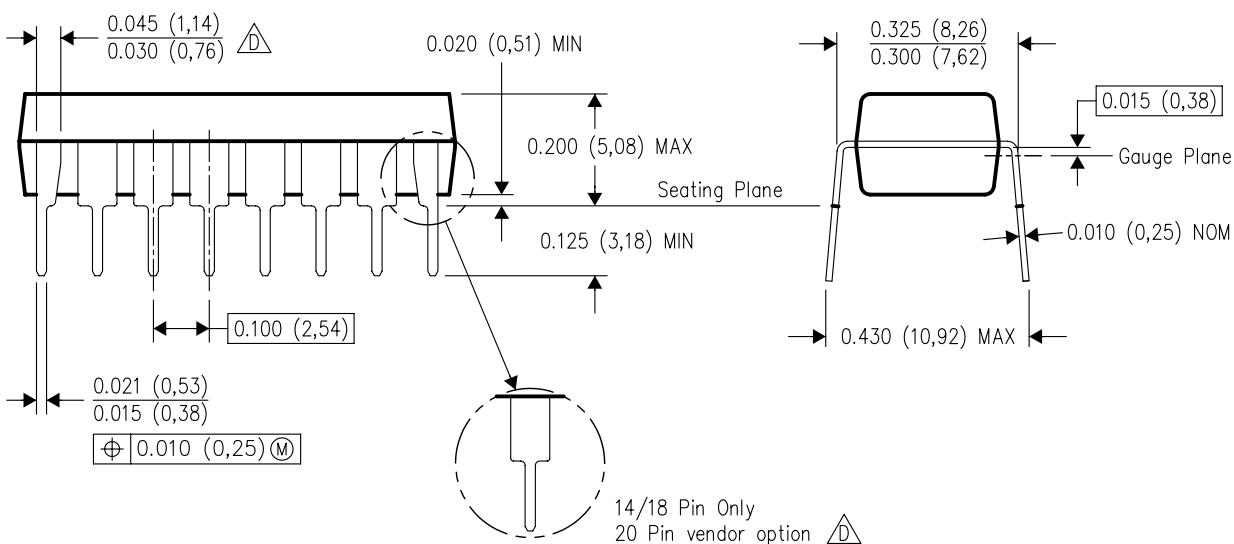
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

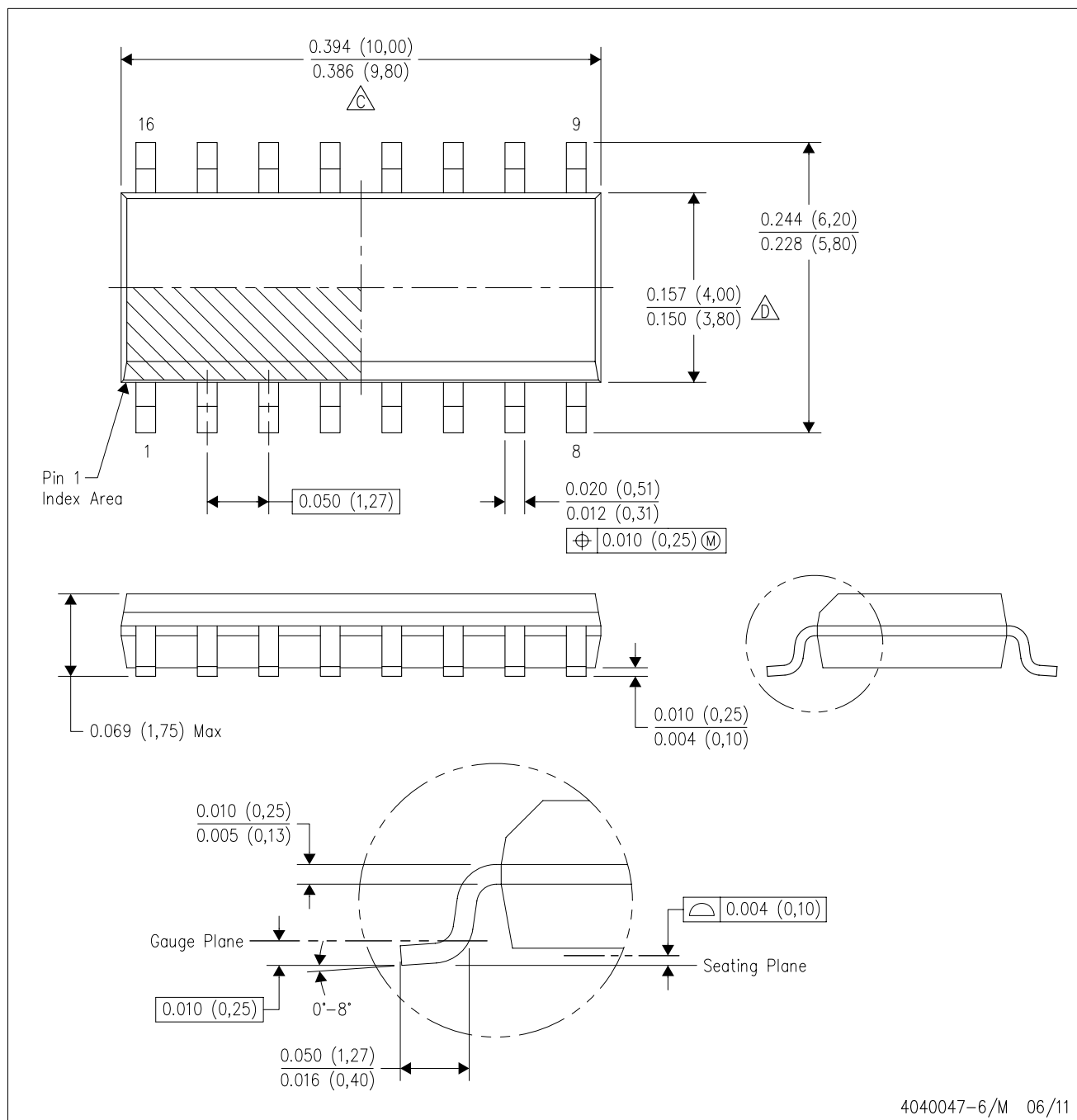


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



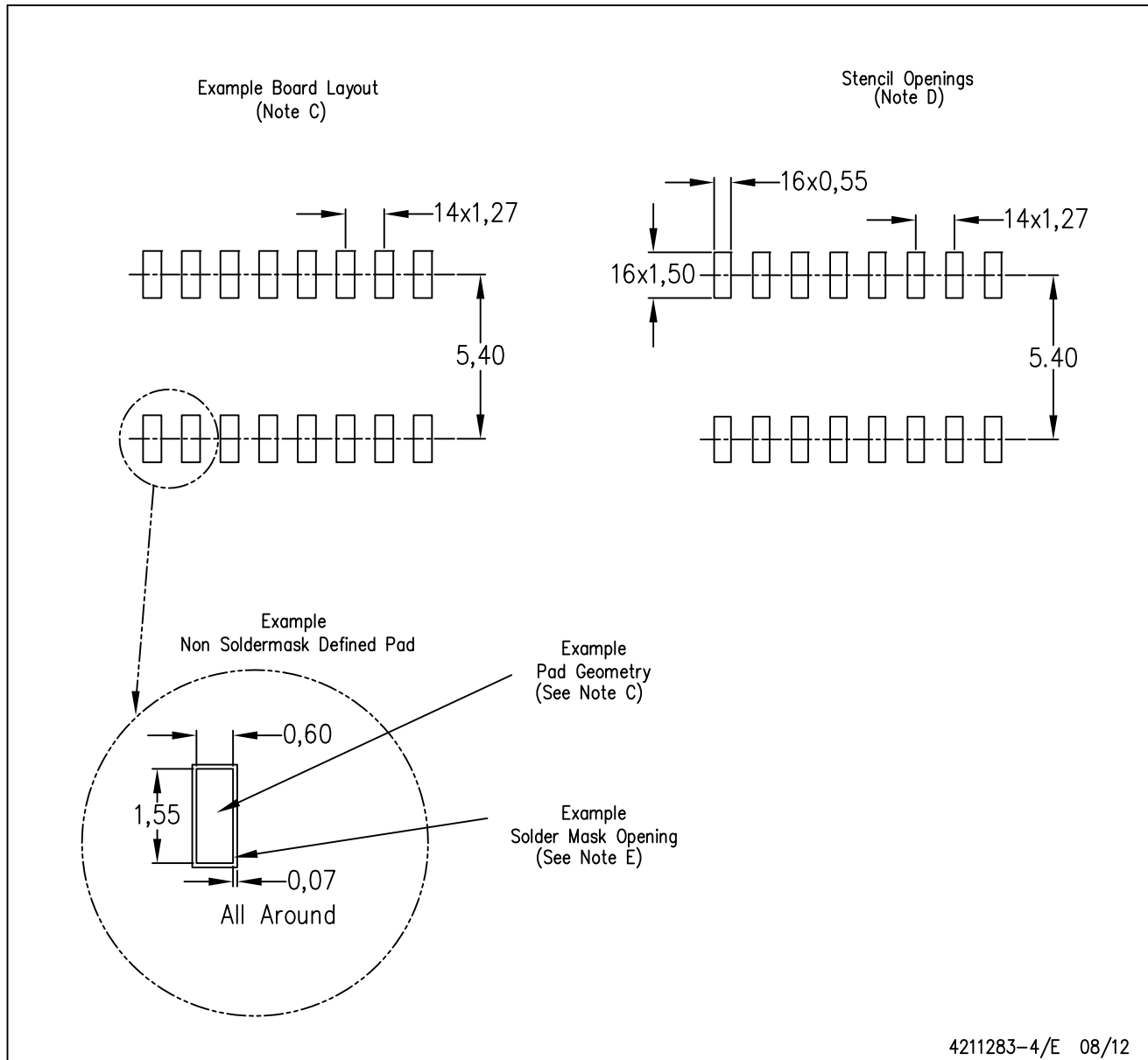
4040047-6/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

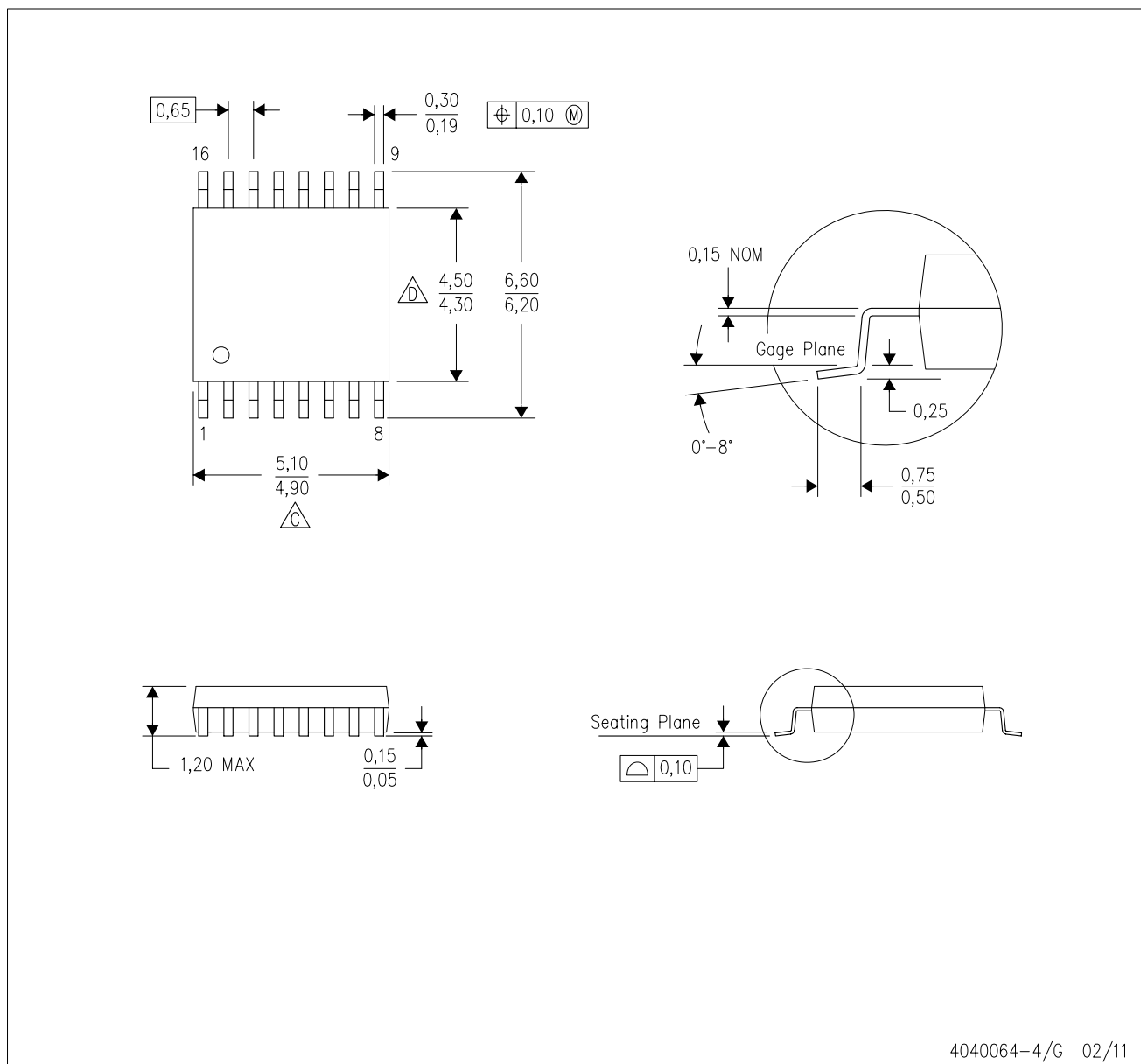
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

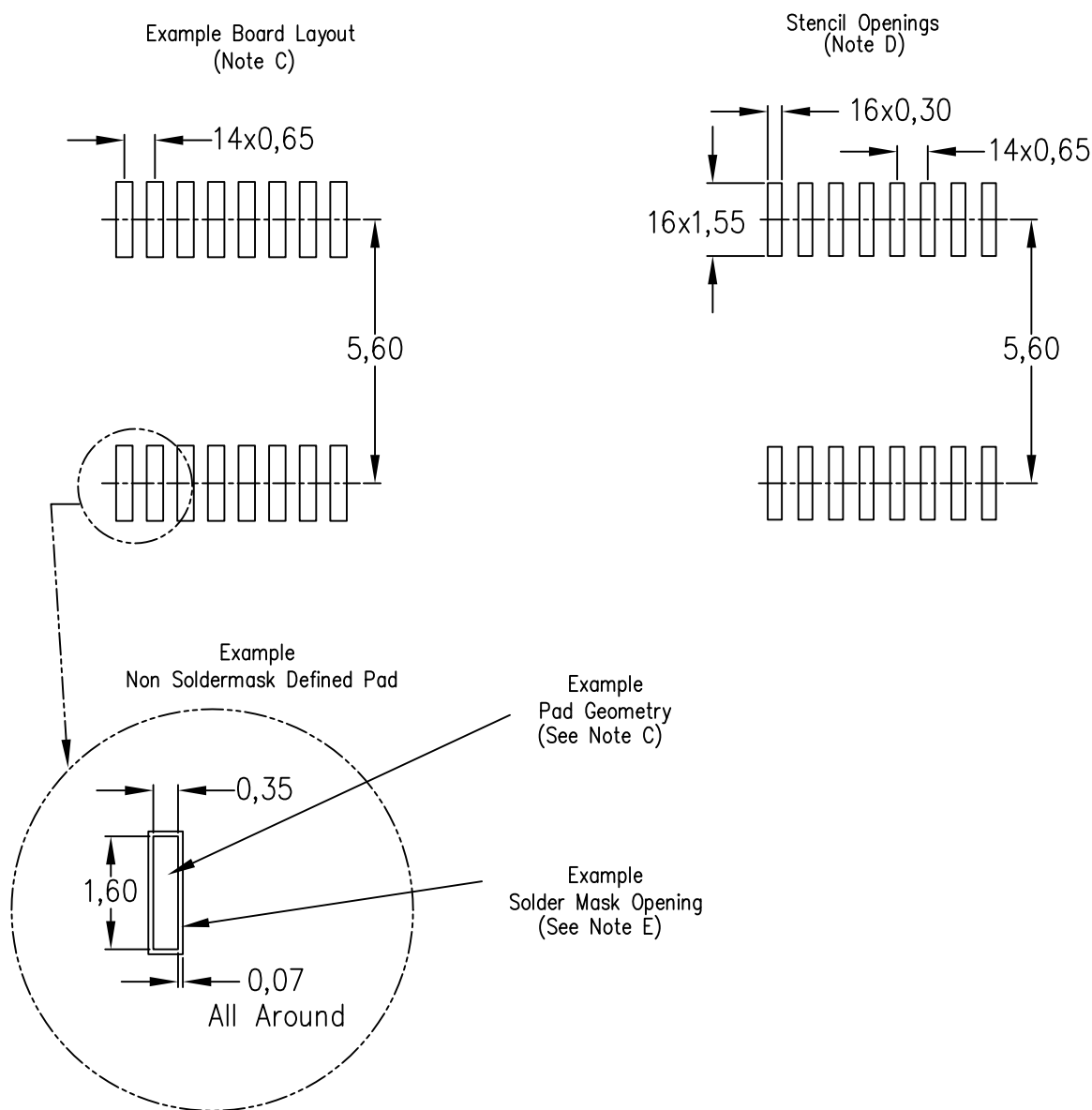
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

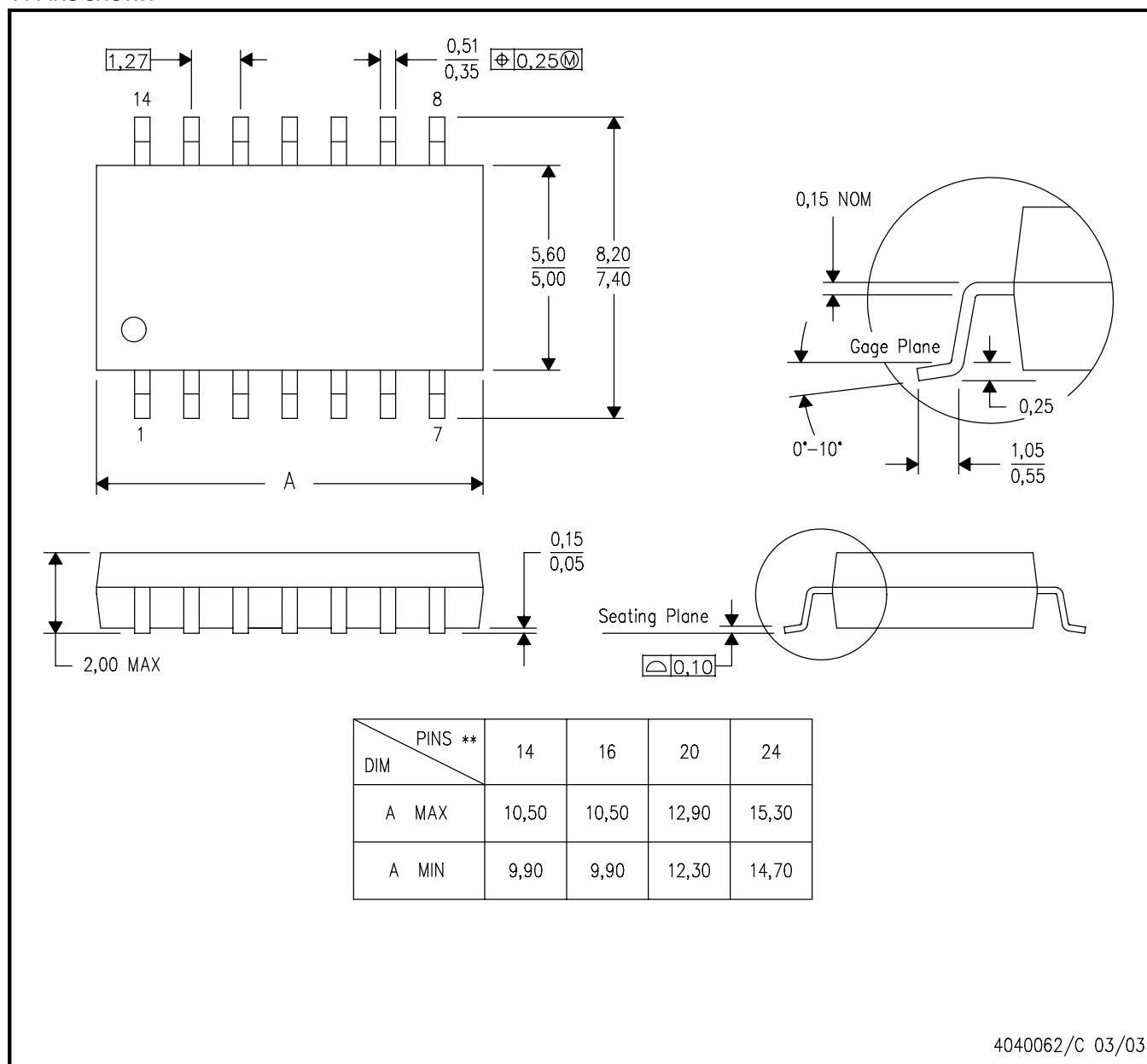
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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