Dual octal buffer/line driver; 3-state 74ALVC16244

FEATURES

- **Wide supply voltage range of 1.2 V to 3.6 V**
- **In accordance with JEDEC standard no.8-1A**
- **CMOS low power consumption**
- **Multibyte™ flow-through standard pin-out architecture**
- **Low inductance multiple power and ground pins for minimum noise and ground bounce**
- **Direct interface with TTL levels**
- **5 V to 3.3 V level shifting**
- **Output drive capability 50 Ω transmission lines @ 85 °C**

DESCRIPTION

The 74ALVC16244 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74ALVC16244 is a 16-bit non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs $1\overline{OE}$ and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high impedance OFF-state. The "16244" is identical to the "16240" but has non-inverting outputs.

FUNCTION TABLE

INPUTS		OUTPUT
$n\overline{OE}$	nA_n	nY_n
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF V_{CC} = 3.3 V	2.1	ns
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	pF

Notes to the quick reference data

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74ALVC16244DL	48	SSOP	plastic	SSOP48/SOT370

PINNING

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	'1' output enable input (active LOW)
2, 3, 5, 6	$1Y_0$ to $1Y_3$	'1Y' data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	ground (0 V)
7, 18, 31, 42	V_{CC}	positive supply voltage
8, 9, 11, 12	$2Y_0$ to $2Y_3$	'2Y' data outputs
13, 14, 16, 17	$3Y_0$ to $3Y_3$	'3Y' data outputs
19, 20, 22, 23	$4Y_0$ to $4Y_3$	'4Y' data outputs
24	$4\overline{OE}$	'4' output enable input (active LOW)
25	$3\overline{OE}$	'3' output enable input (active LOW)
30, 29, 27, 26	$4A_0$ to $4A_3$	'4A' data inputs
36, 35, 33, 32	$3A_0$ to $3A_3$	'3A' data inputs
41, 40, 38, 37	$2A_0$ to $2A_3$	'2A' data inputs
47, 46, 44, 43	$1A_0$ to $1A_3$	'1A' data inputs
48	$2\overline{OE}$	'2' output enable input (active LOW)

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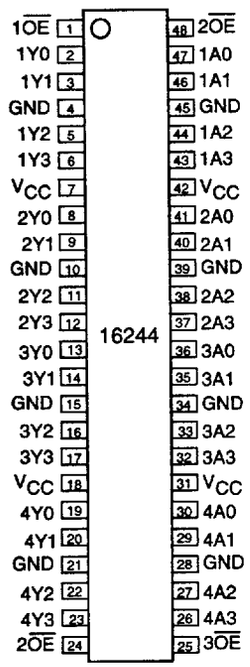


Fig.1 Pin configuration.

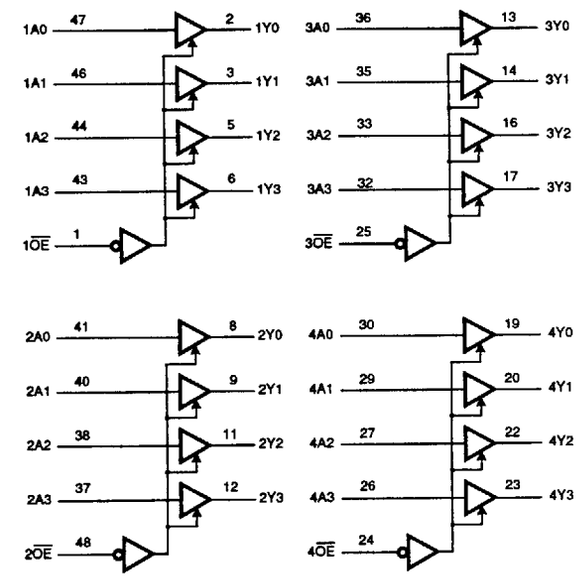


Fig.2 Logic symbol.

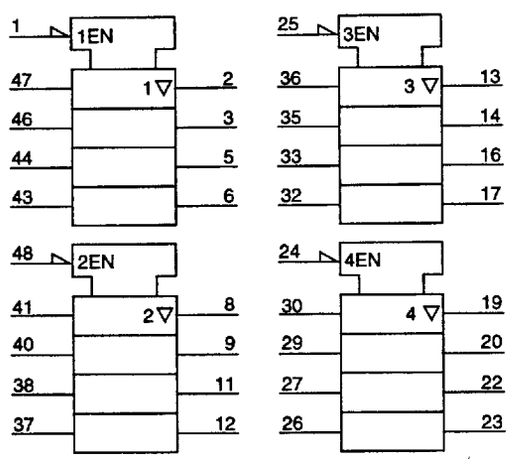


Fig.3 IEC logic symbol.

DC CHARACTERISTICS FOR 74ALVC244

For the DC characteristics see chapter "ALVC family characteristics", section "Family specifications".
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74ALVC244

GND = 0 V; $t_r = t_f$ = 2.5 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) -40 to +85			UNIT	TEST CONDITIONS	
		MIN.	TYP.	MAX.		V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay	–	–	16.0	ns	1.2	Fig. 4
	$1A_n$ to $1Y_n$;	–	–	4.4		2.7	
	$2A_n$ to $2Y_n$	–	2.1*	4.0		3.0 to 3.6	
t_{PZH}/t_{PZL}	3-state output enable time	–	–	–	ns	1.2	Figs 5, 6
	$1\overline{OE}$ to $1Y_n$;	–	–	4.8		2.7	
	$2\overline{OE}$ to $2Y_n$	–	–	4.4		3.0 to 3.6	
t_{PHZ}/t_{PLZ}	3-state output disable time	–	–	–	ns	1.2	Figs 5, 6
	$1\overline{OE}$ to $1Y_n$;	–	–	4.8		2.7	
	$2\overline{OE}$ to $2Y_n$	–	–	4.4		3.0 to 3.6	

Notes: All typical values are measured at T_{amb} = 25 °C.
* Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS (per section of four bits)

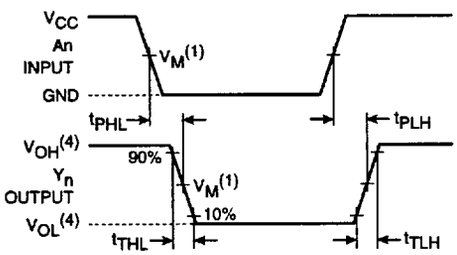


Fig.4 Waveforms showing the input (A_n) to output (Y_n) propagation delays and the output transition times.

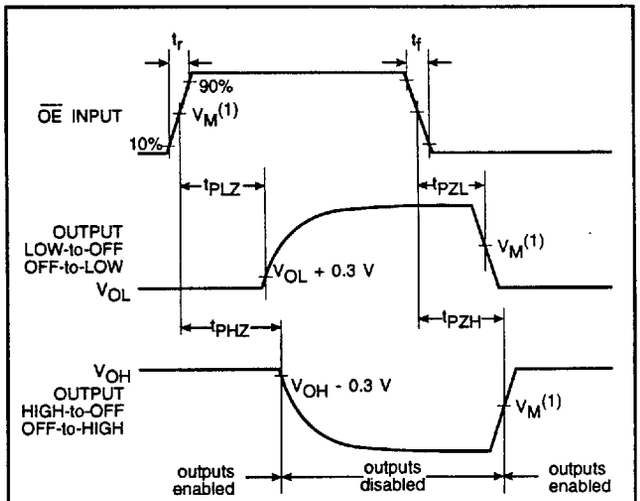
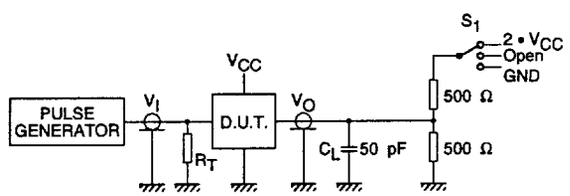


Fig.5 Waveforms showing the 3-state enable and disable times.



Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 • V_{CC}
t_{PHZ}/t_{PZH}	GND

Fig.6 Load circuitry for switching times.

Notes:

(1) $V_M = 0.5 \cdot V_{CC}$ at $V_{CC} < 2.7$ V
$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V

(2) $V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V
$V_X = 0.1 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(3) $V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V
$V_Y = 0.9 \cdot V_{CC}$ at $V_{CC} < 2.7$ V

(4) V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.