LD6815 series

Low-dropout regulators, high PSRR, 150 mA

Rev. 3 — 17 October 2013 Product data sheet

1. Product profile

1.1 General description

The LD6815 series is a small-size Low-DropOut (LDO) regulator family with a high-Power Supply Rejection Ratio (PSRR) of 75 dB. The typical voltage drop is 250 mV at 150 mA current rating. Operating voltages range from 2.3 V to 5.5 V. The devices are available with fixed nominal output voltages $V_{O(nom)}$ between 1.2 V and 3.6 V.

The LD6815 series devices are available in SOT753 (TSOP5) plastic package with a size of 2.9 mm × 1.5 mm × 1.0 mm. All devices are manufactured in monolithic silicon technology.

1.2 Features and benefits

- Overcurrent protection
- Auto discharge or high-ohmic mode for the output state when disabled
- Low quiescent current (0.1 μA) in shutdown mode
- High-level ElectroStatic Discharge (ESD) protection [6 kV Human Body Model (HBM)]
- Industry standard SOT753 (TSOP5) package
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant, free of halogen and antimony (Dark Green compliant)

1.3 Applications

- Smartphones
- Mobile handsets
- Digital still cameras
- Tablet PCs
- Mobile internet devices
- Portable media players

1.4 Quick reference data

- I_{OUT} = 150 mA (max)
- PSRR = 75 dB at 1 kHz
- RMS noise $V_{n(o)(RMS)}$ = 40 μV at 10 Hz to 100 kHz
- $t_{startup(reg)}$ = 150 μs
- V_{IN} = 2.3 V to 5.5 V
- V_{OUT} = 1.2 V to 3.6 V
- Dropout voltage V_{do} = 250 mV at I_{OUT} = 150 mA

2. Pinning information

2.1 Pinning

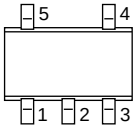

Fig 1. Pin configuration

2.2 Pin description

Table 1. Pin description

Symbol	Pin	Description
IN	1	regulator input voltage
GND	2	supply ground
EN	3	device enable input; active HIGH
n.c.	4	not connected
OUT	5	regulator output voltage

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
LD6815TD	TSOP5	plastic surface-mounted package; 5 leads	SOT753

Further ordering options see Section 3.1 “Ordering options”.

3.1 Ordering options

Further information on output voltage is available on request; see Section 20 “Contact information”. An explanation of high-ohmic and pull-down type is in Section 4 “Block diagram”.

Table 3. Type number extension of high-ohmic output

Type number	Nominal output voltage $V_{O(nom)}$	Type number	Nominal output voltage $V_{O(nom)}$
LD6815TD/12H	1.2 V	LD6815TD/28H	2.8 V
LD6815TD/15H	1.5 V	LD6815TD/29H	2.9 V
LD6815TD/18H	1.8 V	LD6815TD/30H	3.0 V
LD6815TD/21H	2.1 V	LD6815TD/33H	3.3 V
LD6815TD/25H	2.5 V	LD6815TD/36H	3.6 V

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Table 4. Type number extension of pull-down output

Type number	Nominal output voltage $V_{O(nom)}$	Type number	Nominal output voltage $V_{O(nom)}$
LD6815TD/12P	1.2 V	LD6815TD/28P	2.8 V
LD6815TD/15P	1.5 V	LD6815TD/29P	2.9 V
LD6815TD/18P	1.8 V	LD6815TD/30P	3.0 V
LD6815TD/21P	2.1 V	LD6815TD/33P	3.3 V
LD6815TD/25P	2.5 V	LD6815TD/36P	3.6 V

4. Block diagram

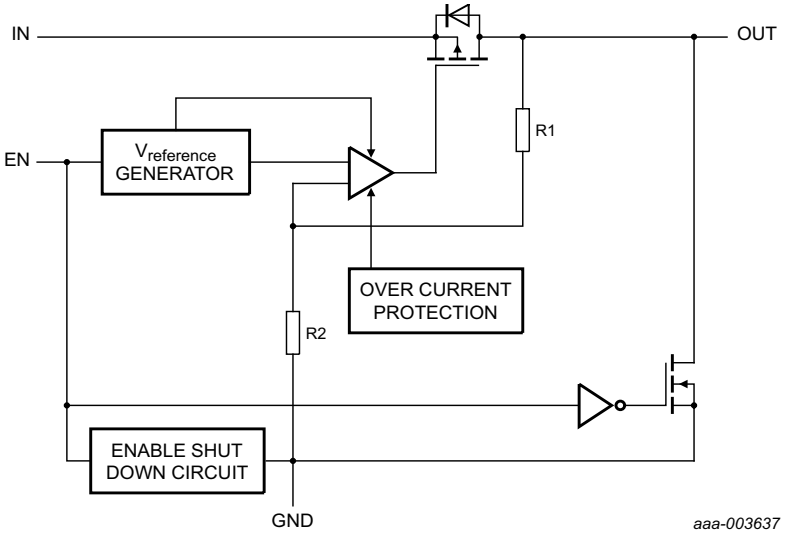

Fig 2. Block diagram of LD6815TD/xxP (auto discharge function)

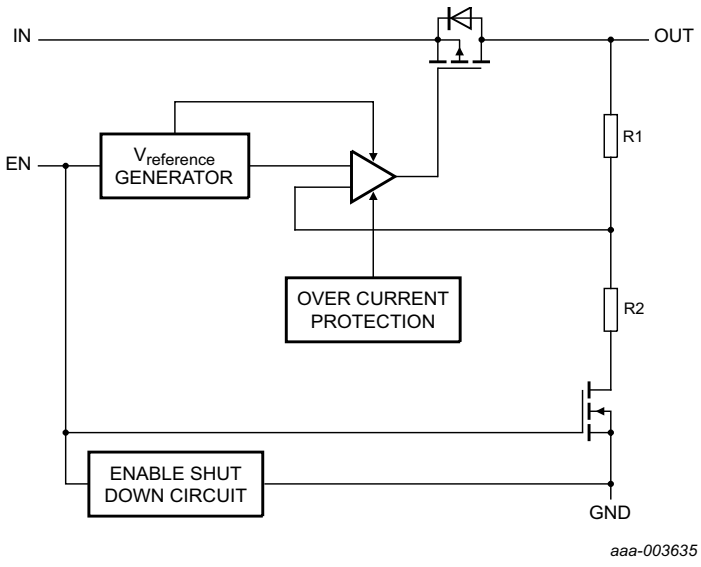

Fig 3. Block diagram of LD6815TD/xxH

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5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{IN}	voltage on pin IN	4 ms transient		–0.5	+6.0	V
V_{EN}	voltage on pin EN	4 ms transient		–0.5	+6.0	V
V_{OUT}	voltage on pin OUT	4 ms transient		–0.5	+6.0	V
P_{tot}	total power dissipation		[1]	-	800	mW
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–40	+125	°C
T_{amb}	ambient temperature			–40	+85	°C
V_{ESD}	electrostatic discharge voltage	human body model	[2]	-	±6	kV
		machine model	[3]	-	±400	V

[1] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 25 °C and the use of a two-layer Printed-Circuit Board (PCB).

[2] According to JESD22-A114 and IEC 61340-3-1.

[3] According to JESD22-A115.

6. Recommended operating conditions

Table 6. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb}	ambient temperature			–40	-	+85	°C
T_j	junction temperature			-	-	125	°C
Pin IN							
V_{IN}	voltage on pin IN			2.3	-	5.5	V
Pin EN							
V_{EN}	voltage on pin EN			0	-	V_{IN}	V
Pin OUT							
V_{OUT}	voltage on pin OUT			–0.5	-	V_{IN} + 0.3	V
$C_{L(ext)}$	external load capacitance		[1]	0.7	1.0	-	µF

[1] See Section 10.1 “Capacitor values”.

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7. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1][2]	125	K/W

[1] The overall $R_{th(j-a)}$ can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$, all pins must have a solid connection to larger Cu layer areas for example to the power and ground layer. In multilayer PCB applications, the second layer is used to create a large heat spreader area directly below the LDO. If this layer is either ground or power, it is connected with several vias to the top layer connecting to the device ground or supply. Avoid the use of solder-stop varnish under the chip.

[2] Use the measurement data given for a rough estimation of the $R_{th(j-a)}$ in your application. The actual $R_{th(j-a)}$ value can vary in applications using different layer stacks and layouts.

8. Characteristics

Table 8. Electrical characteristics

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Output voltage							
V_{do}	dropout voltage	I_{OUT} = 150 mA; $V_{IN} < V_{O(nom)}$	[1]	-	250	-	mV
ΔV_O	output voltage variation	V_{OUT} < 1.8 V; I_{OUT} = 1 mA					
		T_{amb} = +25 °C		−3	±0.5	+3	%
		−40 °C ≤ T_{amb} ≤ +85 °C	[2]	−4	-	+4	%
		$V_{OUT} \geq$ 1.8 V; I_{OUT} = 1 mA					
		T_{amb} = +25 °C		−2	±0.5	+2	%
		−40 °C ≤ T_{amb} ≤ +85 °C	[2]	−3	-	+3	%
Line regulation error							
$\Delta V_O/(V_O \times \Delta V_I)$	relative output voltage variation with input voltage	$V_{IN} = (V_{O(nom)} + 0.5\ V)$ to 5.5 V	[2]	−0.1	-	+0.1	%/V
Load regulation error							
$\Delta V_O/(V_O \times \Delta I_O)$	relative output voltage variation with output current	1 mA ≤ I_{OUT} ≤ 150 mA	[2]	-	0.005	0.02	%/mA
Output current							
I_{OUT}	current on pin OUT			-	-	150	mA
I_{OM}	peak output current	$V_{IN} = (V_{O(nom)} + 0.5\ V)$ to 5.5 V					
		$V_{O(nom)} \geq$ 1.8 V; $V_{OUT} = 0.95 \times V_{O(nom)}$	[2]	200	-	-	mA
		$V_{O(nom)}$ < 1.8 V; $V_{OUT} = 0.9 \times V_{O(nom)}$	[2]	200	-	-	mA
I_{sc}	short-circuit current	pin OUT		-	300	-	mA
Regulator quiescent current							
I_q	quiescent current	V_{EN} = 1.1 V; I_{OUT} = 0 mA		-	35	-	µA
		V_{EN} = 1.1 V; I_{OUT} = 150 mA; $V_{IN} = V_{O(nom)} + 0.5$ V	[2]	-	150	-	µA
		$V_{EN} \leq$ 0.4 V		-	0.1	1	µA

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Table 8. Electrical characteristics *…continued*

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Ripple rejection and output noise							
PSRR	power supply rejection ratio	$V_{IN} = V_{O(nom)} + 1.0$ V; I_{OUT} = 50 mA; f_{ripple} = 1 kHz	[2]	-	75	-	dB
$V_{n(o)(RMS)}$	RMS output noise voltage	f_{ripple} = 10 Hz to 100 kHz; $C_{L(ext)}$ = 1 µF	[2]	-	40	-	µV
Enable input and timing							
V_{IL}	LOW-level input voltage	pin EN		0	-	0.4	V
V_{IH}	HIGH-level input voltage	pin EN		1.1	-	5.5	V
$t_{startup(reg)}$	regulator start-up time	V_{IN} = 5.5 V; $V_{OUT} = 0.95 \times V_{O(nom)}$; I_{OUT} = 150 mA; $C_{L(ext)}$ = 1 µF	[2]	-	150	-	µs
LD6815TD/xxP; auto discharge function							
$t_{sd(reg)}$	regulator shutdown time	V_{IN} = 5.5 V; $V_{OUT} = 0.05 \times V_{O(nom)}$; $C_{L(ext)}$ = 1 µF	[2]	-	300	-	µs
R_{pd}	pull-down resistance		[2]	-	100	-	Ω

[1] $V_{O(nom)}$ = nominal output voltage (device specific).

[2] Parameter is checked, verified and guaranteed by design.

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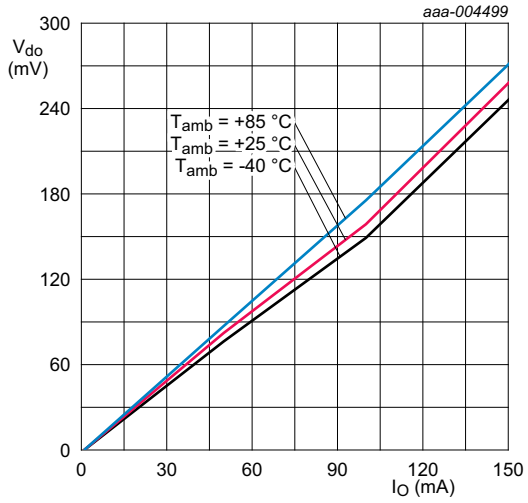
9. Dynamic behavior

9.1 Dropout voltage

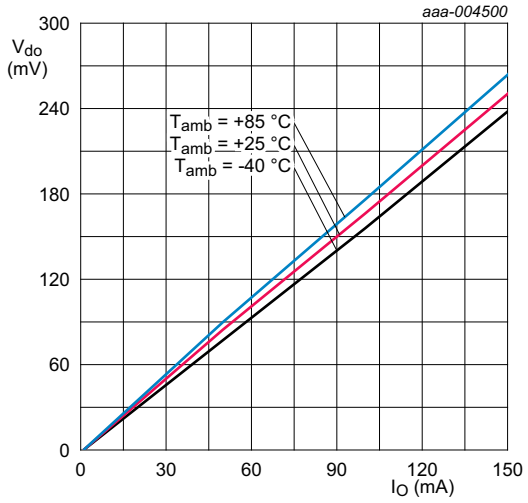
The dropout voltage is defined as the smallest input to output voltage difference at a specified load current when the regulator operates within its linear region. This means that the input voltage is below the nominal output voltage value and the pass transistor works as a plain resistor.

A small dropout voltage guarantees lower power consumption and efficiency maximization.



$V_{IN} = V_{O(nom)} - 0.15\ V = 2.65\ V$;
$C_{L(ext)} = 1\ \mu F$; $C_{ext(IN)} = 1\ \mu F$

Fig 4. LD6815TD/28x: Dropout voltage as a function of output current



$V_{IN} = V_{O(nom)} - 0.15\ V = 3.45\ V$;
$C_{L(ext)} = 1\ \mu F$; $C_{ext(IN)} = 1\ \mu F$

Fig 5. LD6815TD/36x: Dropout voltage as a function of output current

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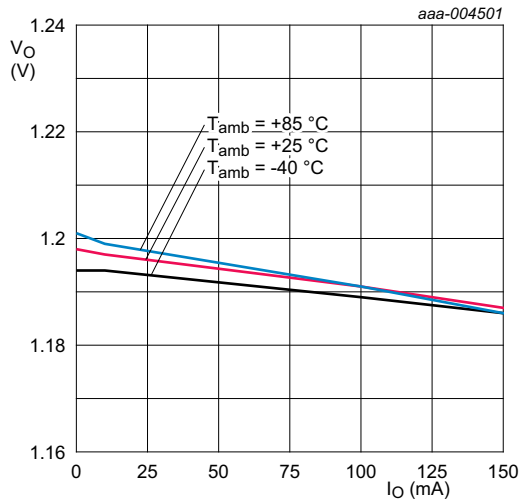
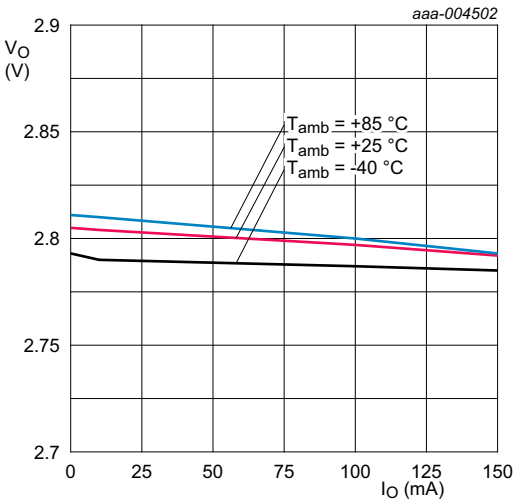
9.2 Output voltage variation (accuracy)

The LD6815 series guarantees high accuracy of the nominal output voltage.



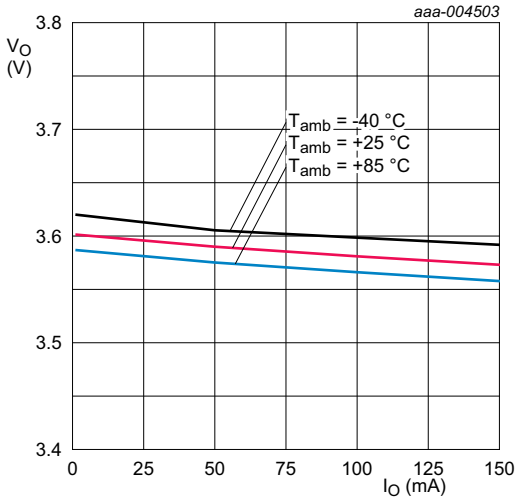
V_{IN} = 2.2 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 6. LD6815TD/12x: Output voltage as a function of output current



V_{IN} = 4.0 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 7. LD6815TD/28x: Output voltage as a function of output current



V_{IN} = 5.5 V; $C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 8. LD6815TD/36x: Output voltage as a function of output current

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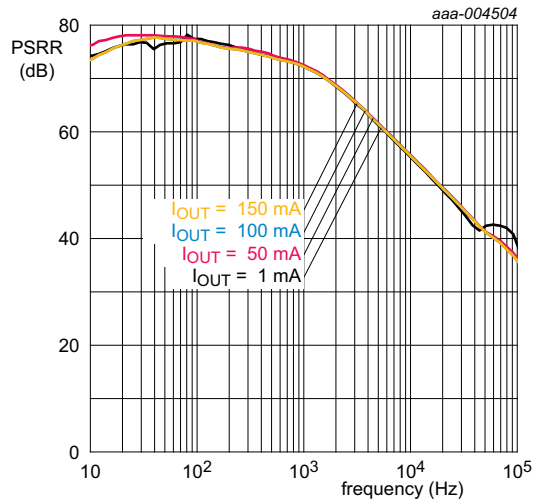
9.3 Power Supply Rejection Ratio (PSRR)

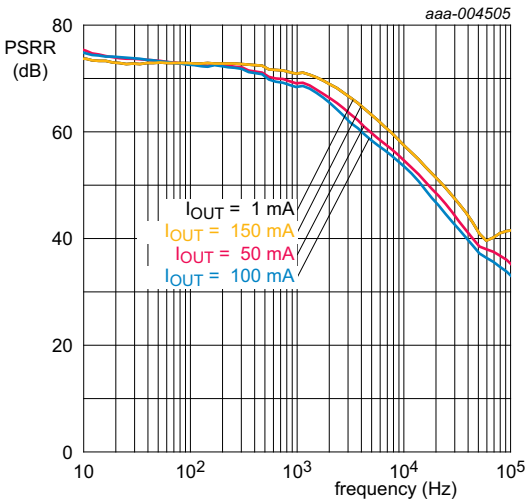
PSRR stands for the capability of the regulator to suppress unwanted signals on the input voltage like noise or ripples.

$$PSRR[dB] = (-20)log\frac{V_{OUT(ripple)}}{V_{IN(ripple)}}$$ for all frequencies



$C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 9. PSRR for LD6815TD/18x



$C_{L(ext)}$ = 1 µF; $C_{ext(IN)}$ = 1 µF

Fig 10. PSRR for LD6815TD/25x

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10. Application information

10.1 Capacitor values

The LD6815 series requires external capacitors at the output to guarantee a stable regulator behavior. Do not under-run the specified minimum Equivalent Series Resistance (ESR). The absolute value of the total capacitance attached to the output pin OUT influences the shutdown time ($t_{sd(reg)}$) of the LD6815 series. Also an input capacitor is recommended to keep the input voltage stable.

Table 9. External load capacitor

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$C_{ext(IN)}$	external capacitance on pin IN		[1]	0.7	1.0		µF
$C_{L(ext)}$	external load capacitance		[1]	0.7	1.0	-	µF
ESR	equivalent series resistance			5	-	500	mΩ

[1] The minimum value of capacitance for stability and correct operation is 0.7 µF. The specified capacitor tolerance is ±30 % (over the temperature and operating range). The recommended capacitor type is X7R to meet the full temperature specification of −40 °C to +125 °C.

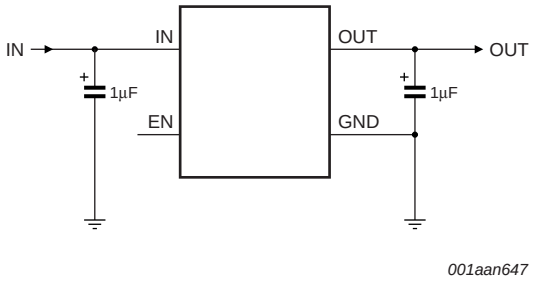

Fig 11. Application diagram

11. Test information

11.1 Quality information

This product has been qualified in accordance with *NX1-00023 NXP Semiconductors Quality and Reliability Specification* and is suitable for use in consumer applications.

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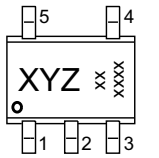
12. Marking



transparent top view

aaa-004520

Circle (bottom left) = marking of pin 1

XYZ = version; for marking code corresponding to type number see Table 10 and Table 11

All other characters = lot ID information

Fig 12. Marking SOT753

Table 10. Marking of high-ohmic output

Type number	Nominal output voltage $V_{O(nom)}$	Marking code	Type number	Nominal output voltage $V_{O(nom)}$	Marking code
LD6815TD/12H	1.2 V	AC3	LD6815TD/28H	2.8 V	AC7
LD6815TD/15H	1.5 V	AC4	LD6815TD/29H	2.9 V	AC8
LD6815TD/18H	1.8 V	AC5	LD6815TD/30H	3.0 V	AC9
LD6815TD/21H	2.1 V	AE4	LD6815TD/33H	3.3 V	AD1
LD6815TD/25H	2.5 V	AC6	LD6815TD/36H	3.6 V	AD2

Table 11. Marking of pull-down output

Type number	Nominal output voltage $V_{O(nom)}$	Marking code	Type number	Nominal output voltage $V_{O(nom)}$	Marking code
LD6815TD/12P	1.2 V	AD3	LD6815TD/28P	2.8 V	AD7
LD6815TD/15P	1.5 V	AD4	LD6815TD/29P	2.9 V	AD8
LD6815TD/18P	1.8 V	AD5	LD6815TD/30P	3.0 V	AD9
LD6815TD/21P	2.1 V	AE3	LD6815TD/33P	3.3 V	AE1
LD6815TD/25P	2.5 V	AD6	LD6815TD/36P	3.6 V	AE2

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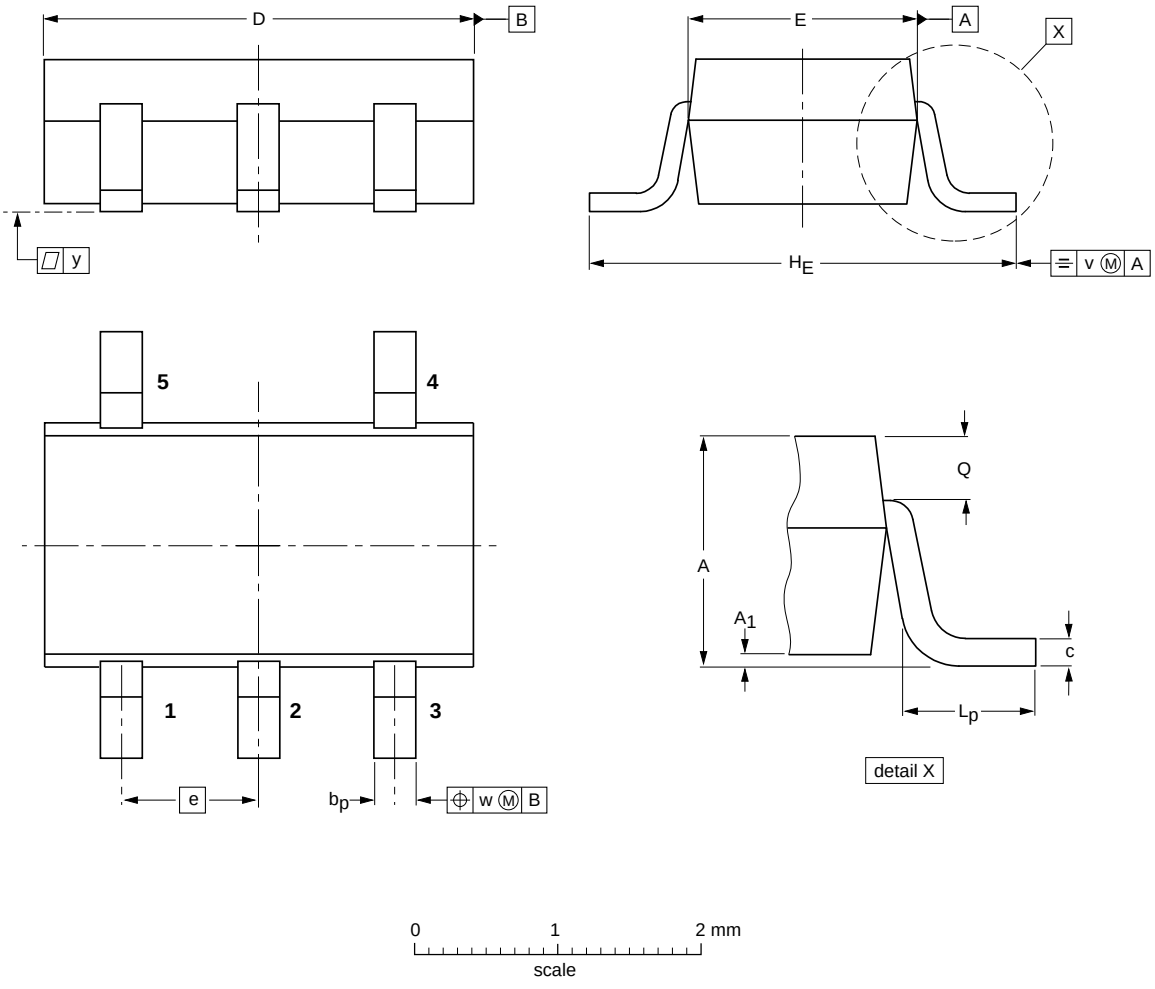
13. Package outline

Plastic surface-mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig 13. Package outline SOT753 (TSOP5)

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14. Packing information

14.1 Packing methods

Table 12. Packing methods

Type number	Package	Description	Orientation [1]	12NC ending	Packing quantity
LD6815TD	SOT753	4 mm pitch, 8 mm tape and reel	Q3	125	3000

[1] For further information about orientation, see Section 14.2.

14.2 Carrier tape information

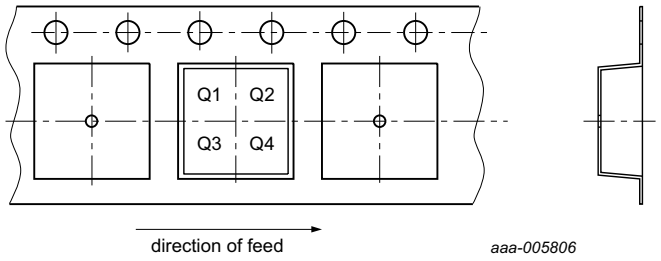

Fig 14. Carrier tape

Table 13. Orientations

Orientation	Meaning	Pin 1 location
Q1	quadrant 1	upper left
Q2	quadrant 2	upper right
Q3	quadrant 3	lower left
Q4	quadrant 4	lower right

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15. Soldering

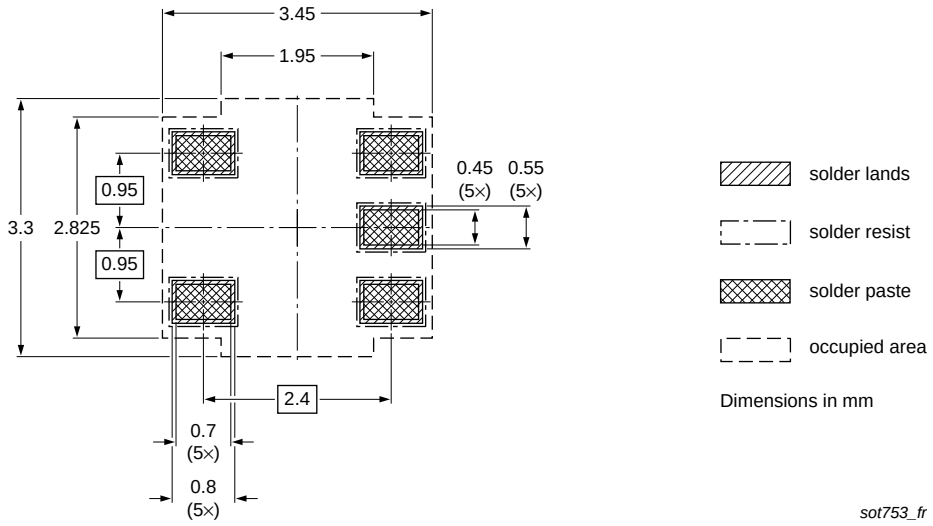

Fig 15. Soldering footprint SOT753 (TSOP5)

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

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The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14 and 15

Table 14. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

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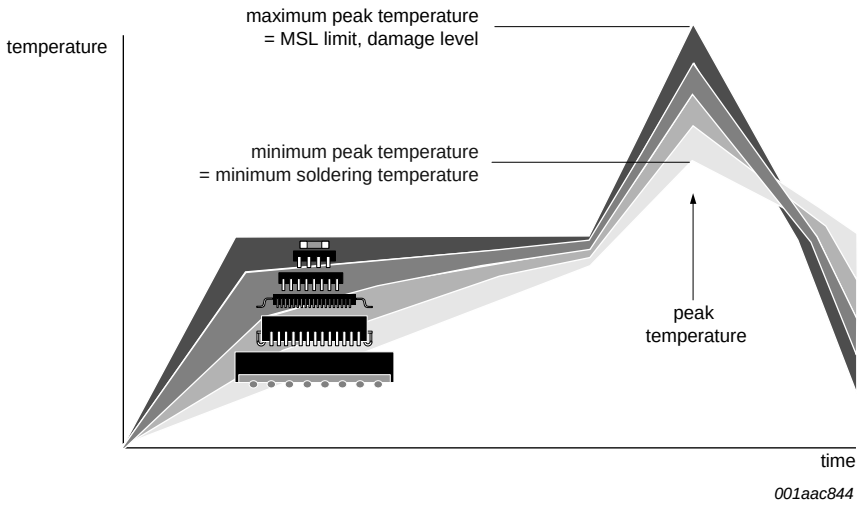
Table 15. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.



MSL: Moisture Sensitivity Level

Fig 16. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. References

[1] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[2] **IEC 61340-3-1 —** Methods for simulation of electrostatic effects - Human Body Model (HBM) electrostatic discharge test waveforms

[3] **JESD22-A114 —** ElectroStatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[4] **JESD22-A115 —** ElectroStatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[5] **NX1-00023 —** NXP Semiconductors Quality and Reliability Specification

[6] **AN10365 —** Surface mount reflow soldering description

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18. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LD6815_SER v.3	20131017	Product data sheet	-	LD6815_SER v.2
Modifications:	• Section 1 “Product profile”: redesigned and updated			
LD6815_SER v.2	20121214	Product data sheet	-	LD6815_SER v.1
LD6815_SER v.1	20120807	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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