



-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

MAX5921/MAX5939

General Description

The MAX5921/MAX5939 hot-swap controllers allow a circuit card to be safely hot plugged into a live backplane. The MAX5921/MAX5939 operate from -20V to -80V and are well suited for -48V power systems. These devices are pin compatible with both the LT1640 and LT4250 and provide improved features over these devices.

The MAX5921/MAX5939 provide a controlled turn-on to circuit cards preventing damage to board connectors, board components, and preventing glitches on the power-supply rail. The MAX5921/MAX5939 provide undervoltage, overvoltage, and overcurrent protection. These devices ensure that the input voltage is stable and within tolerance before applying power to the load.

Both the MAX5921 and MAX5939 protect a system against overcurrent and short-circuit conditions by turning off the external MOSFET in the event of a fault condition. The MAX5921/MAX5939 protect against input voltage steps by limiting the load current to a safe level without turning off power to the load.

The device features an open-drain power-good status output, PWRGD or PWRGD for enabling downstream converters (see *Selector Guide*). A built-in thermal shutdown feature is also included to protect the external MOSFET in case of overheating. The MAX5939 features a latched fault output. The MAX5921 contains built-in autoretry circuitry after a fault condition.

The MAX5921/MAX5939 are available in an 8-pin SO package and operate in the extended -40°C to +85°C temperature range.

Applications

Telecom Line Cards
Network Switches/Routers
Central-Office Line Cards
Server Line Cards
Base-Station Line Cards

Typical Operating Circuit and Selector Guide appear at end of data sheet.

Features

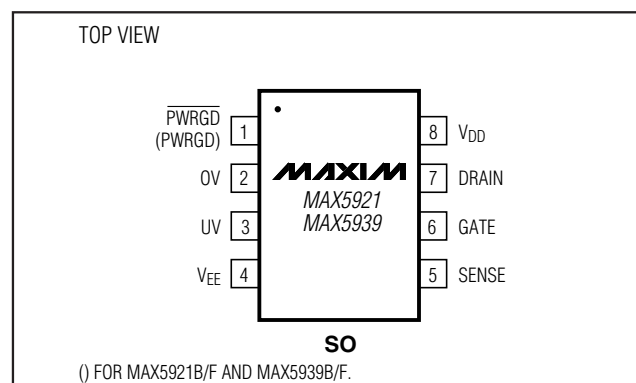
- ◆ Allows Safe Board Insertion and Removal from a Live -48V Backplane
- ◆ Pin-Compatible with LT1640 and LT4250
- ◆ Circuit Breaker Immunity to Input Voltage Steps and Current Spikes
- ◆ 450mA GATE Pulldown Current During Short-Circuit Condition
- ◆ Exponential GATE Pulldown Current
- ◆ Withstands -100V Input Transients with No External Components
- ◆ Programmable Inrush and Short-Circuit Current Limits
- ◆ Operates from -20V to -80V
- ◆ Programmable Overvoltage Protection
- ◆ Programmable Undervoltage Lockout with Built-In Glitch Filter
- ◆ Overcurrent Fault Integrator
- ◆ Powers Up into a Shorted Load
- ◆ Power-Good Control Output
- ◆ Thermal Shutdown Protects External MOSFET

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5921AESA	-40°C to +85°C	8 SO
MAX5921BESA	-40°C to +85°C	8 SO

Ordering Information continued at end of data sheet.

Pin Configuration



-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

ABSOLUTE MAXIMUM RATINGS

All Voltages Are Referenced to VEE, Unless Otherwise Noted
 Supply Voltage (VDD - VEE) -0.3V to +100V
 DRAIN, PWRGD, PWRGD -0.3V to +100V
 PWRGD to DRAIN -0.3V to +95V
 PWRGD to VDD -95V to +85V
 SENSE (Internally Clamped) -0.3V to +1.0V
 GATE (Internally Clamped) -0.3V to +18V
 UV and OV -0.3V to +60V
 Current into SENSE +40mA

Current into GATE +300mA
 Current into Any Other Pin +20mA
 Continuous Power Dissipation (TA = +70°C)
 8-Pin SO (derate 5.9mW/°C above +70°C) 471mW
 Operating Temperature Range -40°C to +85°C
 Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (soldering, 10s) +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VEE = 0V, VDD = 48V, TA = -40°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C, unless otherwise noted.) (Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Operating Input Voltage Range	VDD		20		80	V
Supply Current	IDD	Current into VDD with UV = 3V, OV, DRAIN, SENSE = VEE, GATE = floating		0.7	2	mA
GATE DRIVER AND CLAMPING CIRCUITS						
Gate Pullup Current	IPU	GATE drive on, VGATE = VEE	-30	-45	-60	μA
Gate Pulldown Current	IPD	VSENSE - VEE = 100mV, VGATE = 2V (Note 2)	24	50	70	mA
External Gate Drive	ΔVGATE	VGATE - VEE, steady state, 20V ≤ VDD ≤ 80V	10	13.5	18	V
GATE to VEE Clamp Voltage	VGSCCLMP	VGATE - VEE, IGS = 30mA	15	16.4	18	V
CIRCUIT BREAKER						
Current-Limit Trip Voltage	VCL	VCL = VSENSE - VEE	40	50	60	mV
SENSE Input Current	ISENSE	VSENSE = 50mV	-1	-0.2	0	μA
UNDERVOLTAGE LOCKOUT						
Supply Internal Undervoltage Lockout Voltage High	VUVLOH	VDD increasing	13.8	15.4	17.0	V
Supply Internal Undervoltage Lockout Voltage Low	VUVLOL	VDD decreasing	11.8	13.4	15.0	V
UV INPUT						
UV High Threshold	VUVH	UV voltage increasing	1.240	1.255	1.270	V
UV Low Threshold	VUVL	UV voltage decreasing	1.105	1.125	1.145	V
UV Hysteresis	VUVHY			130		mV
UV Input Current	IINUV	UV = VEE	-0.5		0	μA
OV INPUT						
OV High Threshold	VOVH	OV voltage rising	1.235	1.255	1.275	V
OV Low Threshold	VOVL	OV voltage decreasing	1.189	1.205	1.221	V
OV Voltage Reference Hysteresis	VOVHY			50		mV
OV Input Current	IINOV	OV = VEE	-0.5		0	μA

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = 0V, V_{DD} = 48V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
PWRGD OUTPUT SIGNAL (REFERENCED TO DRAIN)								
DRAIN Input Current	I _{DRAIN}	V _{DRAIN} = 48V		10	80	250	μA	
DRAIN Threshold for PWRGD	V _{DL}	V _{DRAIN} - V _{EE} threshold for power-good condition, DRAIN decreasing		1.1	1.7	2.0	V	
GATE High Threshold	V _{GH}	ΔV _{GATE} - V _{GATE} , decreasing		1.0	1.6	2.0	V	
PWRGD, $\overline{\text{PWRGD}}$ Output Leakage	I _{OH}	V $\overline{\text{PWRGD}}$ = 80V, V _{DRAIN} = 48V		10			μA	
		V $\overline{\text{PWRGD}}$ = 80V, V _{DRAIN} = 0V		10				
PWRGD Low Voltage (V $\overline{\text{PWRGD}}$ - V _{EE})	V _{OL}	V _{DRAIN} - V _{EE} < V _{DL} , I _{SINK} = 5mA (A, E versions)		0.11			0.4	V
PWRGD Low Voltage (V $\overline{\text{PWRGD}}$ - V _{DRAIN})	V _{OL}	V _{DRAIN} = 5V, I _{SINK} = 5mA (B, F versions)		0.11			0.4	V
OVERTEMPERATURE PROTECTION								
Overtemperature Threshold	T _{OT(TH)}	Junction temperature, temperature rising		135			°C	
Overtemperature Hysteresis	T _{HYS}	See <i>Thermal Shutdown</i> section		20			°C	
AC PARAMETERS								
OV High to GATE Low	t _{PHLOV}	Figures 1a, 2		0.5			μs	
UV Low to GATE Low	t _{PHLUV}	Figures 1a, 3		0.4			μs	
OV Low to GATE High	t _{PLHOV}	Figures 1a, 2		3.3			μs	
UV High to GATE High	t _{PLHUV}	Figures 1a, 3		8.4			ms	
SENSE High to GATE Low	t _{PHLSENSE}	Figures 1a, 4a		1			μs	
Current Limit to GATE Low	t _{PHLCL}	Time from continuous current limit to GATE shutdown (see <i>Overcurrent Fault Integrator</i> section), Figures 1b, 4b	A, B versions	0.35	0.5	0.65	ms	
			E, F versions	1.4	2.0	2.6		
DRAIN Low to $\overline{\text{PWRGD}}$ Low	t _{PHLDL}	Figures 1a, 5a; A and E versions		8.2			ms	
DRAIN Low to (PWRGD - DRAIN) High		Figures 1a, 5a; B and F versions		8.2				
GATE High to $\overline{\text{PWRGD}}$ Low	t _{PHLGH}	Figures 1a, 5b; A and E versions		8.2			ms	
GATE High to (PWRGD - DRAIN) High		Figures 1a, 5b; B and F versions		8.2				
TURN-OFF								
Latch-Off Period	t _{OFF}	(Note 3)	A, B, E, F versions	128 x t _{PHLCL}			ms	

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to V_{EE}, unless otherwise specified.

Note 2: Gate pulldown current after the current limit to GATE low (t_{PHLCL}) time has elapsed.

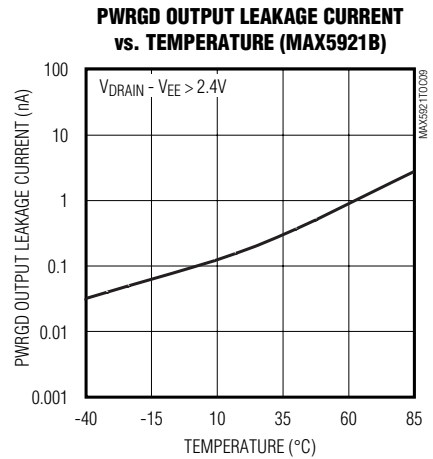
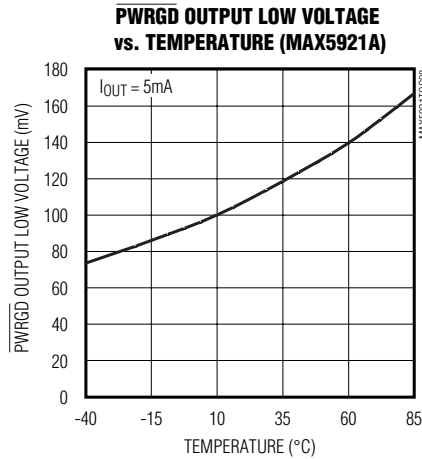
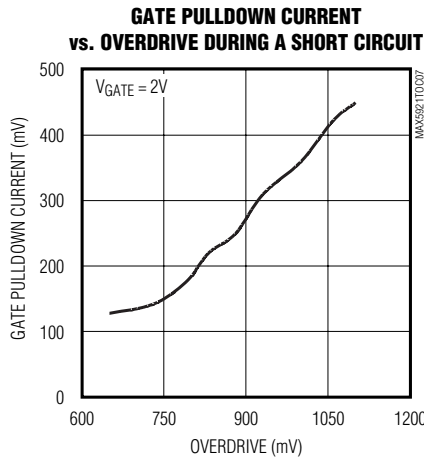
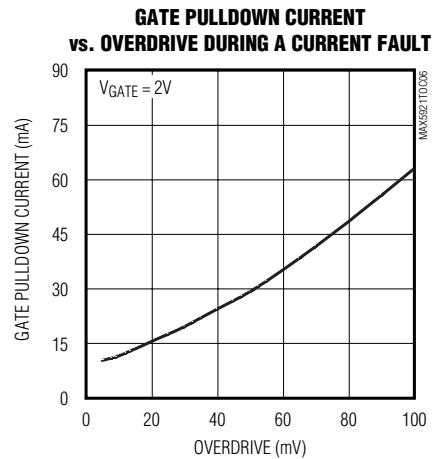
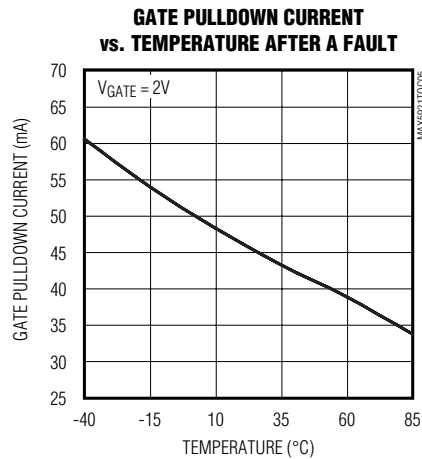
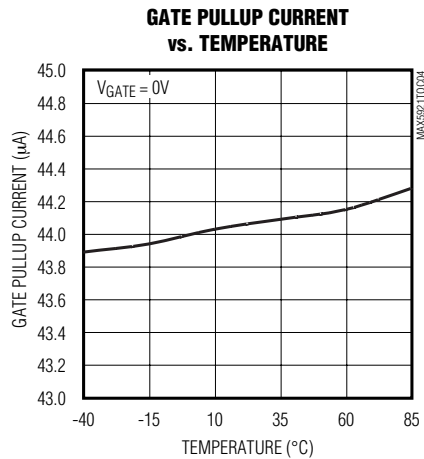
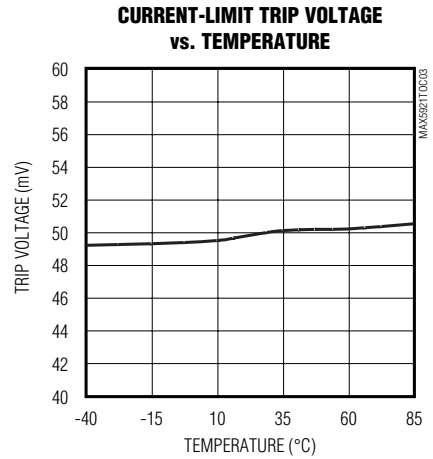
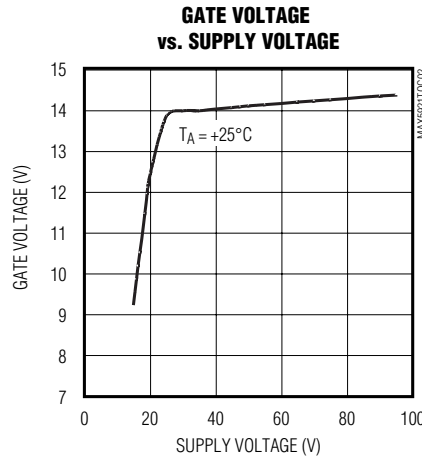
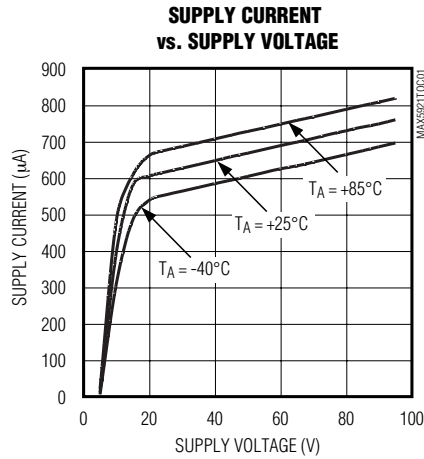
Note 3: Minimum duration of GATE pulldown following a circuit breaker fault. The MAX5921_ automatically restarts after a circuit breaker fault. The MAX5939_ is latched off and can be reset by toggling UV low. The GATE pulldown does not release until t_{OFF} has elapsed.

Note 4: The min/max limits are 100% production tested at +25°C and +85°C and guaranteed by design at -40°C.

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

Typical Operating Characteristics

($V_{DD} = +48V$, $V_{EE} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)



-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

MAX5921/MAX5939

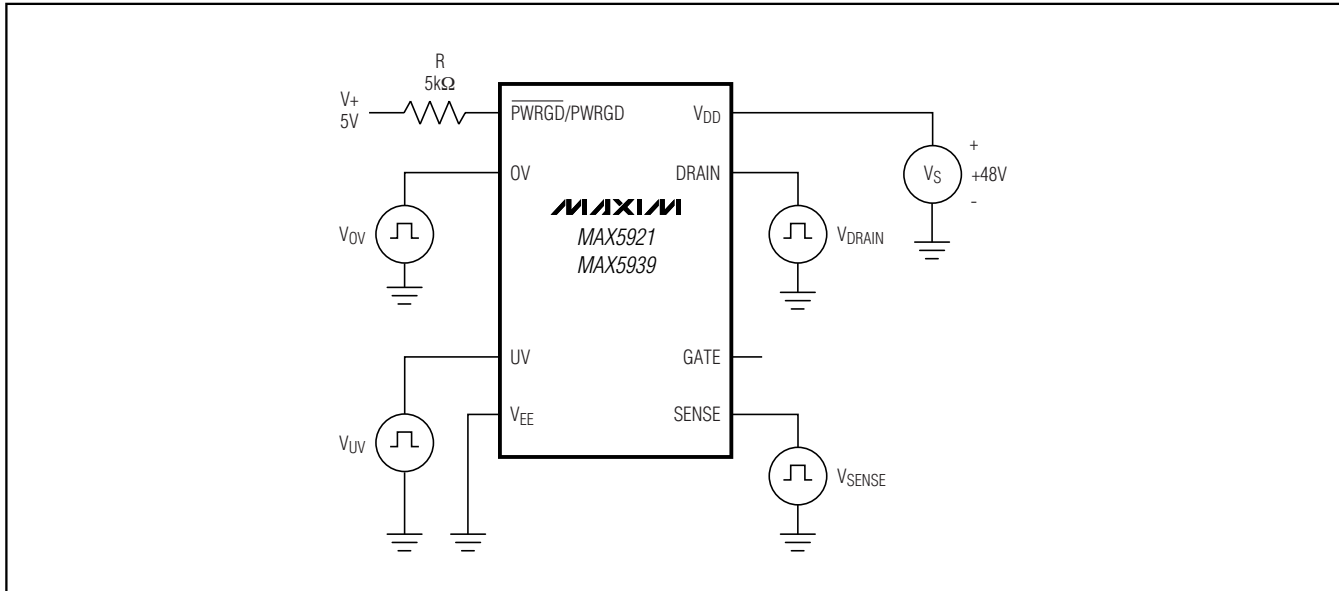


Figure 1a. Test Circuit 1

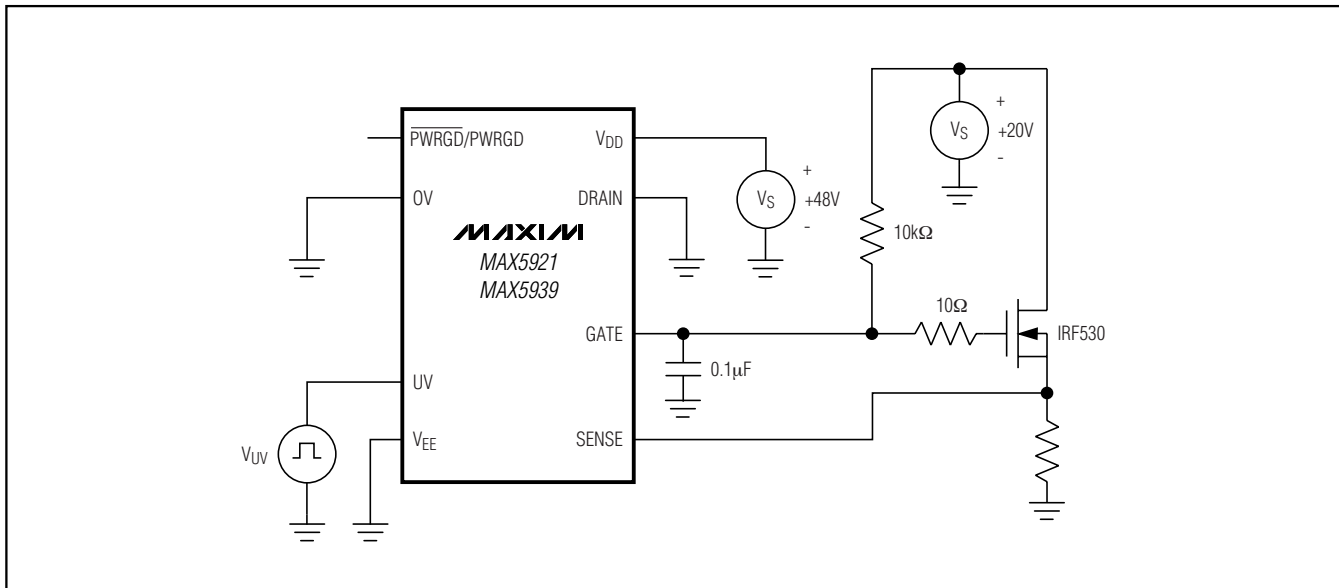


Figure 1b. Test Circuit 2

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

Timing Diagrams

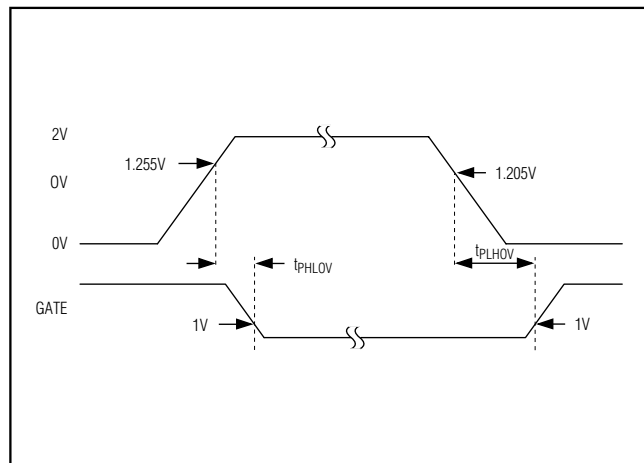


Figure 2. OV to GATE Timing

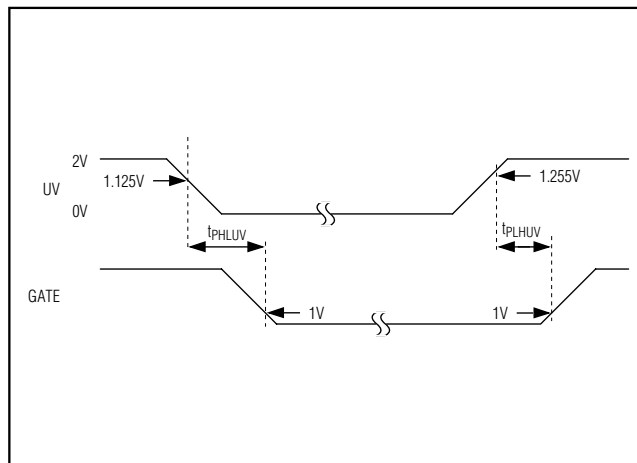


Figure 3. UV to GATE Timing

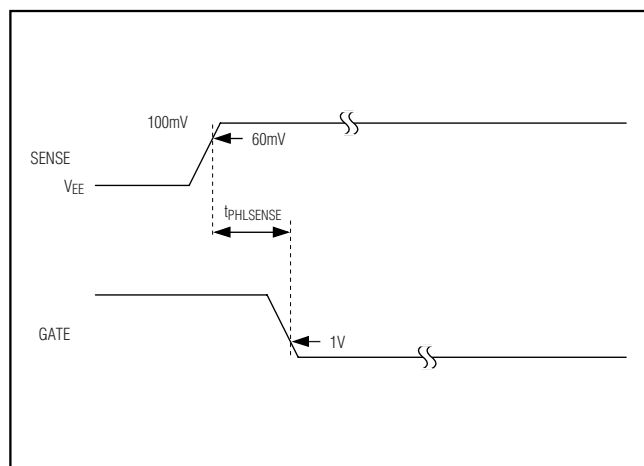


Figure 4a. SENSE to GATE Timing

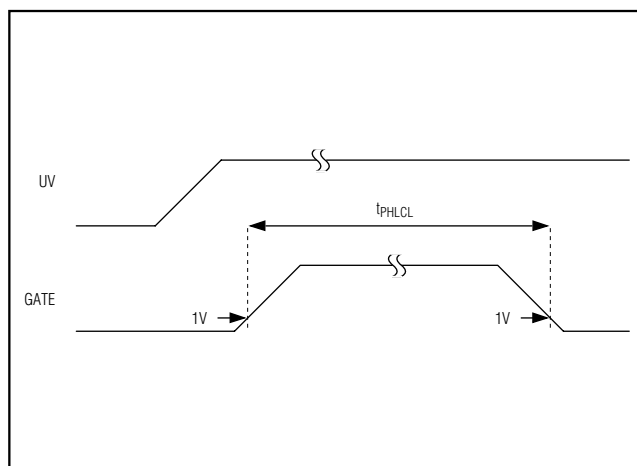


Figure 4b. Active Current-Limit Threshold

MAX5921/MAX5939

The diagram shows two timing scenarios for the PWRGD and DRAIN signals. In the top scenario, the DRAIN signal is at 1.4V and the PWRGD signal is at V_{EE}. When PWRGD transitions from high to low, DRAIN transitions from 1.4V to V_{EE}. The time interval between the falling edge of PWRGD and the falling edge of DRAIN is labeled t_{PHLDL} . In the bottom scenario, the DRAIN signal is at 1.4V and the PWRGD signal is at V_{EE}. When PWRGD transitions from low to high, DRAIN transitions from 1.4V to V_{EE}. The time interval between the rising edge of PWRGD and the rising edge of DRAIN is labeled t_{PHLDL} . The voltage levels are indicated as 1.4V, V_{EE}, and 1V.

The diagram illustrates the timing requirements for the PWRGD pin. It shows two test conditions for the propagation delay t_{PHLGH} from a high gate signal to the PWRGD pin falling to 1V.

- Top Condition:** The gate signal $GATE$ transitions from 0V to 1.4V. The PWRGD signal transitions from V_{DD} to 1V. The delay t_{PHLGH} is measured from the rising edge of $GATE$ to the falling edge of PWRGD.
- Bottom Condition:** The gate signal $GATE$ transitions from 0V to 1.4V. The PWRGD signal transitions from V_{DD} to 1V. The delay t_{PHLGH} is measured from the rising edge of $GATE$ to the falling edge of PWRGD. The condition $V_{DCEN} - V_{DRAIN} = 0V$ is specified.

The schematic diagram illustrates the internal architecture of the MAX5921/MAX5939 precision centred level shifter. Key components and their connections include:

- VDD and REFERENCE GENERATOR:** Provides a stable V_{DD} supply and a reference voltage REF to the comparators and logic.
- UVLO (Under-Voltage Lockout):** Monitors the V_{DD} supply to ensure proper operation.
- LOGIC:** Coordinates the internal operations, including the output driver and gate driver.
- Comparators:** Two comparators are used. One compares the UV input against REF , and the other compares the OV input against REF . Their outputs are connected to the $UVLO$ and $LOGIC$ blocks.
- 50mV Reference:** A precision 50mV reference voltage is provided for the comparators.
- GATE DRIVER:** Controls the gate of the MOSFETs, ensuring they switch properly.
- OUTPUT DRIVER:** Provides the final centred square wave output, which is also available as $PWRGD$ and $\overline{PWRGD}$.
- MOSFETs:** Two MOSFETs are used for signal inversion and level shifting. The first MOSFET's gate is driven by the $GATE DRIVER$ and its source is connected to V_{EE} . The second MOSFET's gate is driven by the $GATE DRIVER$ and its source is connected to V_{EE} . The drain of the first MOSFET is connected to the $DRAIN$ input, and the drain of the second MOSFET is connected to the $DRAIN$ input.
- Inputs and Outputs:** The circuit has inputs for UV , OV , REF , $50mV$, V_{EE} , $SENSE$, $GATE$, and $DRAIN$. The output is a centred square wave, with $PWRGD$ and $\overline{PWRGD}$ signals also available.

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

Pin Description

PIN		NAME	FUNCTION
MAX5921A/ MAX5921E MAX5939A/ MAX5939E	MAX5921B/ MAX5921F MAX5939B/ MAX5939F		
1	—	$\overline{\text{PWRGD}}$	Power-Good Signal Output. $\overline{\text{PWRGD}}$ is an active-low open-drain status output referenced to V_{EE} . $\overline{\text{PWRGD}}$ latches low when $V_{\text{DRAIN}} - V_{EE} \leq V_{\text{DL}}$ and $V_{\text{GATE}} > \Delta V_{\text{GATE}}$ indicating a power-good condition. $\overline{\text{PWRGD}}$ is open drain otherwise.
—	1	PWRGD	Power-Good Signal Output. PWRGD is an active-high open-drain status output referenced to DRAIN. PWRGD latches in a high-impedance state when $V_{\text{DRAIN}} - V_{EE} \leq V_{\text{DL}}$ and $V_{\text{GATE}} > \Delta V_{\text{GATE}} - V_{\text{GH}}$ indicating a power-good condition. PWRGD is pulled low to DRAIN otherwise.
2	2	OV	Overvoltage Detection Input. OV is referenced to V_{EE} . When OV is pulled above V_{OVH} voltage, GATE pulls low. GATE remains low until the OV voltage reduces to $V_{\text{OVH}} - V_{\text{OVHY}}$.
3	3	UV	Undervoltage Detection Input. UV is referenced to V_{EE} . When UV is pulled above V_{UVH} voltage, the GATE is enabled. When UV is pulled below V_{UVL} , GATE pulls low. UV is also used to reset the circuit breaker after a fault condition. To reset the circuit breaker, pull UV below V_{UVL} . The reset command can be issued immediately after a fault condition; however, the device will not restart until a t_{OFF} delay time has elapsed after the fault condition is removed.
4	4	V_{EE}	Negative Power-Supply Input. Connect to the negative power-supply rail.
5	5	SENSE	Current-Sense Input. Connect to the external sense resistor and the source of the external MOSFET. The voltage drop across the external sense resistor is monitored to detect overcurrent or short-circuit fault conditions. Connect SENSE to V_{EE} to disable the current-limiting feature.
6	6	GATE	Gate Drive Output. Connect to the gate of the external N-channel MOSFET.
7	7	DRAIN	Output Voltage Sense Input. Connect to the output voltage node (drain of external N-channel MOSFET). Place the MAX5921/MAX5939 such that DRAIN is close to the drain of the external MOSFET for the best thermal protection.
8	8	V_{DD}	Positive Power-Supply Input. This is the power ground in the negative supply voltage system. Connect to the higher potential of the power-supply inputs.

Detailed Description

The MAX5921/MAX5939 integrated hot-swap controllers for -48V power systems allow circuit boards to be safely hot plugged into a live backplane without causing a glitch on the power-supply rail. When circuit boards are inserted into a live backplane, the bypass capacitors at the input of the board's power module or switching power supply can draw large inrush currents as they charge. Uncontrolled inrush currents can cause glitches on the system power supply and damage components on the board.

The MAX5921/MAX5939 provide a controlled turn-on to circuit cards preventing damage to connectors, board components, and prevent glitches on the power-supply rail. Both the MAX5921/MAX5939 provide undervoltage, overvoltage, and overcurrent protection. The MAX5921/MAX5939 ensure that the input voltage is stable and within tolerance before applying power to the load. The device also provides protection against input voltage steps by limiting the load current to a safe level without turning off power to the load.

MAX5921/MAX5939

9

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

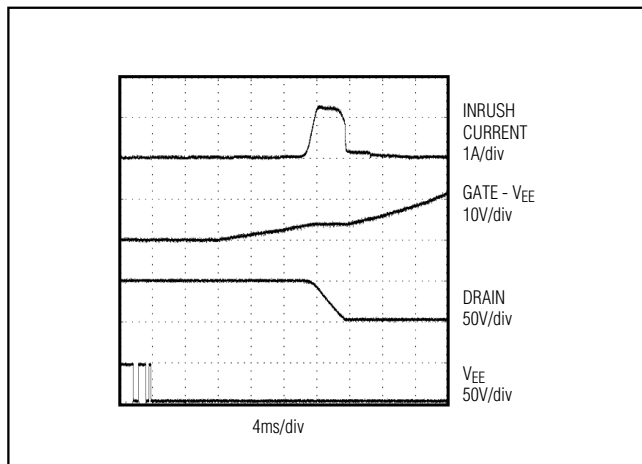


Figure 6b. Inrush Control Waveforms

If the voltage between VEE and SENSE reaches the current-limit trip voltage (V_{CL}), the MAX5921/MAX5939 pull down the GATE and regulate the current through the external MOSFET such that $V_{SENSE} - V_{EE} \leq V_{CL}$. If the current drawn by the load drops below V_{CL} / R_{SENSE} limit, the GATE voltage rises again. However, if the load current is at the regulation limit of V_{CL} / R_{SENSE} for a period of t_{PHLCL} , the electronic circuit breaker trips, causing the MAX5921/MAX5939 to turn off the external MOSFET.

After an overcurrent fault condition, the MAX5921 automatically restarts after t_{OFF} has elapsed. The MAX5939 circuit breaker is reset by toggling UV or by cycling power. Unless power is cycled to the MAX5939, the device waits until t_{OFF} has elapsed before turning on the gate of the external FET.

Load-Current Regulation

The MAX5921/MAX5939 accomplish load-current regulation by pulling current from GATE whenever $V_{SENSE} - V_{EE} > V_{CL}$. This decreases the gate-to-source voltage of the external MOSFET, thereby reducing the load current. When $V_{SENSE} - V_{EE} < V_{CL}$, the MAX5921/MAX5939 pulls GATE high by a $45\mu A$ (I_{PU}) current.

Exponential Current Regulation

The MAX5921/MAX5939 provide an exponential pull-down current to turn off the external FET in response to overcurrent conditions. The GATE pulldown current increases (see *Typical Operating Characteristics*) in response to $V_{SENSE} - V_{EE}$ potentials greater than 50mV (V_{CL}).

Load Current Regulation (Short-Circuit Condition)

The MAX5921/MAX5939 devices also include a very fast high-current pulldown source connected to GATE (see *Typical Operating Characteristics*). The high-current pulldown activates if V_{SENSE} exceeds V_{EE} by 650mV (typ) during a catastrophic overcurrent or short-circuit fault condition. The high-current pulldown circuit sinks as much as 450mA from GATE to turn off the external MOSFET.

Immunity to Input Voltage Steps

The MAX5921/MAX5939 guard against input voltage steps on the input supply. A rapid increase in the input supply voltage ($V_{DD} - V_{EE}$ increasing) causes a current step equal to $I = C_L \times \Delta V_{IN} / \Delta t$, proportional to the input voltage slew rate ($\Delta V_{IN} / \Delta t$). If the load current exceeds V_{CL} / R_{SENSE} during an input voltage step, the MAX5921/MAX5939 current limit activates, pulling down the gate voltage and limiting the load current to V_{CL} / R_{SENSE} . The DRAIN voltage (V_{DRAIN}) then slews at a slower rate than the input voltage. As the drain voltage starts to slew down, the drain-to-gate feedback capacitor C_2 pushes back on the gate, reducing the gate-to-source voltage (V_{GS}) and the current through the external MOSFET. Once the input supply reaches its final value, the DRAIN slew rate (and therefore the inrush current) is limited by the capacitor C_2 just as it is limited in the startup condition (see the *Power-Supply Ramping* section). To ensure correct operation, R_{SENSE} must be chosen to provide a current limit larger than the sum of the load current and the dynamic current into the load capacitance in the slewing mode.

If the load current plus the capacitive charging current is below the current limit, the circuit breaker does not trip.

Undervoltage and Overvoltage Protection

Use UV and OV to detect undervoltage and overvoltage conditions. UV and OV internally connect to analog comparators with 130mV (UV) and 50mV (OV) of hysteresis. When the UV voltage falls below its threshold or the OV voltage rises above its threshold, GATE pulls low. GATE is held low until UV goes high and OV is low, indicating that the input supply voltage is within specification. The MAX5921/MAX5939 includes an internal lockout (UVLO) that keeps the external MOSFET off until the input supply voltage exceeds 15.4V, regardless of the UV input.

UV is also used to reset the circuit breaker after a fault condition has occurred. Pull UV below V_{UVL} to reset the circuit breaker.

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

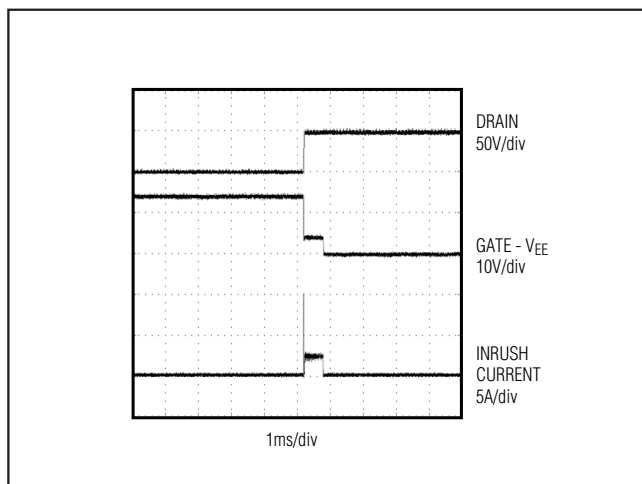


Figure 7. Short-Circuit Protection Waveform

Figure 10 shows how to program the undervoltage and overvoltage trip thresholds using three resistors. With $R4 = 549k\Omega$, $R5 = 6.49k\Omega$, and $R6 = 10k\Omega$, the undervoltage threshold is set to 38.5V (with a 43V release from undervoltage), and the overvoltage is set to 71V. The resistor-divider also increases the hysteresis and overvoltage lockout to 4.5V and 2.8V at the input supply, respectively.

PWRGD/PWRGD Output

Use the $\overline{\text{PWRGD}}$ (PWRGD) output to enable a power module after hot insertion. Use the MAX59__A (PWRGD) to enable modules with an active-low enable input (Figure 12), or use the MAX59__B (PWRGD) to enable modules with an active-high enable input (Figure 11).

The PWRGD signal is referenced to the DRAIN terminal, which is the negative supply of the power module. The $\overline{\text{PWRGD}}$ signal is referenced to V_{EE} .

When the DRAIN voltage of the MAX5921A (see *Selector Guide* for complete selection) or MAX5939A is high with respect to V_{EE} or the GATE voltage is low from an undervoltage condition, then the internal pull-down MOSFET Q2 is off. The PWRGD output goes into a high-impedance state (Figure 13). PWRGD is pulled high by the module's internal pullup current source, turning the module off. When the DRAIN voltage drops below V_{DL} and the GATE voltage is greater than $\Delta V_{GATE} - V_{GH}$, Q2 turns on and PWRGD pulls low, enabling the module.

The $\overline{\text{PWRGD}}$ signal can also be used to turn on an LED

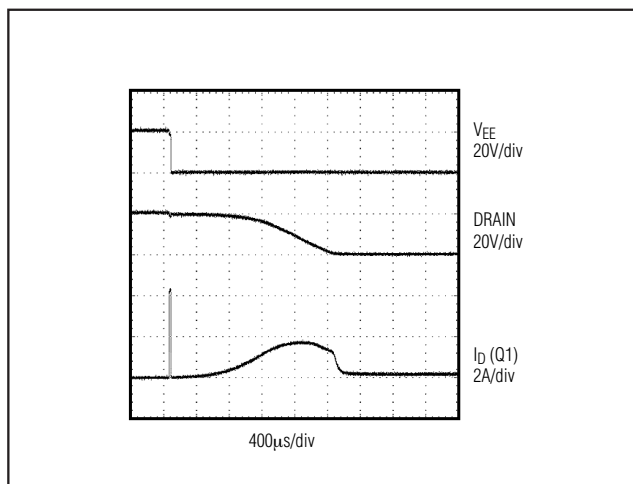


Figure 8. Voltage Step-On Input Supply

or optoisolator to indicate that the power is good (Figure 13) (see the *Component Selection Procedure* section).

When the DRAIN voltage drops below V_{DL} and the GATE voltage is greater than $\Delta V_{GATE} - V_{GH}$, MOSFET Q3 turns on, shorting I_1 to V_{EE} and turning Q2 off. The pullup current in the module pulls the PWRGD high, enabling the module.

When the DRAIN voltage of the MAX5921B/MAX5939B (see *Selector Guide* for complete selection) is high with respect to V_{EE} (Figure 12) or the GATE voltage is low due to an undervoltage condition, the internal MOSFET Q3 is turned off so that I_1 and the internal MOSFET Q2 clamp PWRGD to the DRAIN turning off the module.

Once the PWRGD and $\overline{\text{PWRGD}}$ outputs are active, the MAX5921/MAX5939 output does not toggle due to an overvoltage (OV) fault.

GATE Voltage Regulation

GATE goes high when the following startup conditions are met: UV is high, OV is low, the supply voltage is above V_{UVLOH} , and $(V_{SENSE} - V_{EE})$ is less than 50mV. The gate is pulled up with a 45μA current source and is regulated at 13.5V above V_{EE} . The MAX5921/MAX5939 include an internal clamp that ensures the GATE voltage of the external MOSFET never exceeds 18V. During a fast-rising V_{DD} , an additional dynamic clamp keeps the GATE and SENSE potentials as close as possible to prevent the FET from accidentally turning on. When a fault condition is detected, GATE is pulled low (see the *Load Current Regulation* section).

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

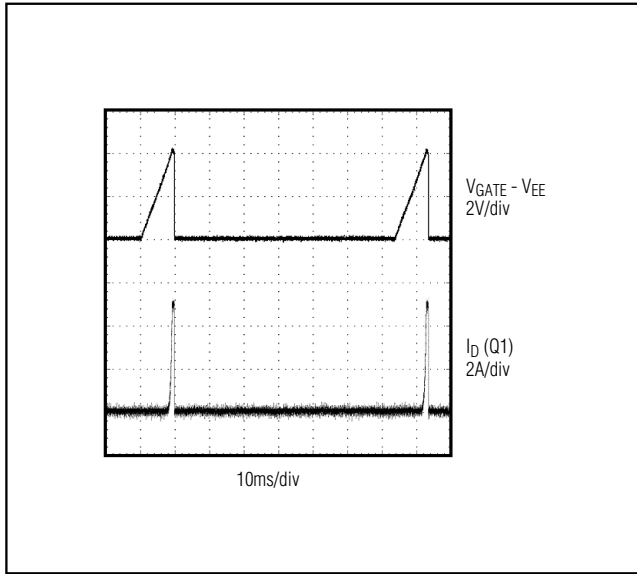


Figure 9. Automatic Restart After a Short Circuit

Overcurrent Fault Integrator

The MAX5921/MAX5939 feature an overcurrent fault integrator. When an overcurrent condition is detected, an internal digital counter is incremented. The clock period for the digital counter is 32μs for the 500μs maximum current-limit duration version and 128μs for 2ms maximum current-limit duration devices. An overcurrent of less than 32μs is interpreted as an overcurrent of 32μs. When the counter reaches 500μs (the maximum current-limit duration) for the MAX5921/MAX5939A, an overcurrent fault is generated. If the overcurrent fault does not last 500μs, then the counter begins decrementing at a rate 128 (maximum current-limit duty cycle) times slower than the counter was incrementing. Repeated overcurrent conditions generate a fault if the duty cycle of the overcurrent condition duty ratio is greater than the maximum current-limit duty cycle (see Figure 14).

Thermal Shutdown

The MAX5921/MAX5939 include internal die-temperature monitoring. When the die temperature reaches the thermal-shutdown threshold, T_{OT} , the MAX5921/MAX5939 pull GATE low and turn off the external MOSFET. If a good thermal path is provided between the MOSFET and the MAX5921/MAX5939, the device offers thermal protection for the external MOSFET. Placing the

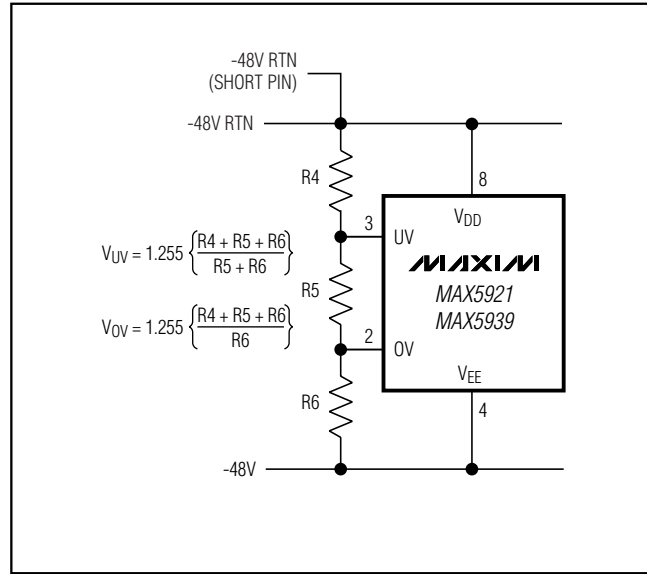


Figure 10. Undervoltage and Overvoltage Sensing

MAX5921/MAX5939 near the drain of the external MOSFET offers the best thermal protection because most of the power is dissipated in its drain.

After a thermal shutdown fault has occurred, the MAX5921_ turns the external FET off for a minimum time of t_{OFF} , allowing the MOSFET to cool down. The MAX5921_ device restarts after the temperature drops 20°C below the thermal-shutdown threshold.

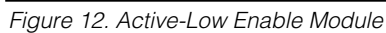
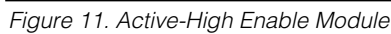
The MAX5939_ latches off after a thermal shutdown fault. The MAX5939_ can be restarted by toggling UV low or cycling power. However, the device keeps the external FET off for a minimum time of t_{OFF} when toggling UV.

Applications Information

Sense Resistor

The circuit-breaker current-limit threshold is set to 50mV (typ). Select a sense resistor that causes a drop equal to or above the current-limit threshold at a current level above the maximum normal operating current. Typically, set the overload current to 1.5 to 2.0 times the nominal load current plus the dynamic load-capacitance charging current during startup. Choose the sense resistor power rating to be greater than $(V_{CL})^2 / R_{SENSE}$.

MAX5921/MAX5939



-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

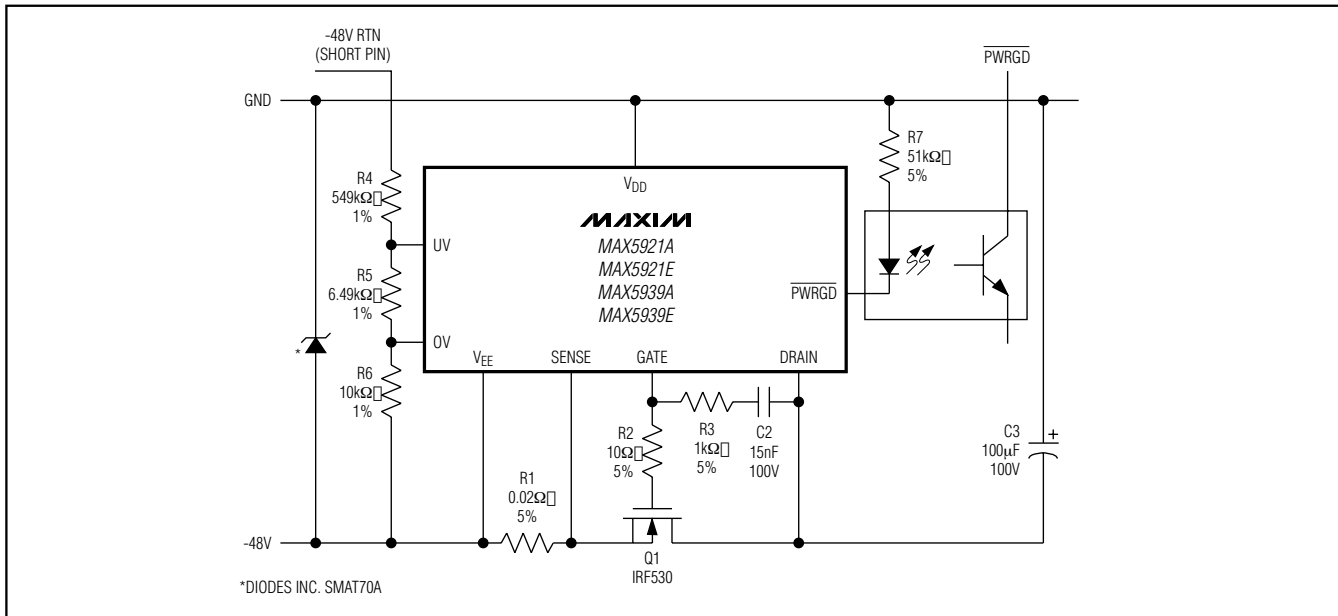


Figure 13. Using $\overline{PWRGD}$ to Drive an Optoisolator

Component Selection Procedure:

- Determine load capacitance:
 $C_L = C_2 + C_3 + \text{module input capacitance}$
- Determine load current, I_{LOAD} .
- Select circuit-breaker current, for example:
 $I_{CB} = 2 \times I_{LOAD}$

$$R_{\text{SENSE}} = \frac{50\text{mV}}{I_{\text{CB}}}$$

Realize that I_{CB} varies $\pm 20\%$ due to trip-voltage tolerance.

- Set allowable inrush current:

$$I_{INRUSH} \leq 0.8 \times \frac{40mV}{R_{SENSE}} - I_{LOAD} \text{ or } I_{INRUSH} + I_{LOAD} \leq 0.8 \times I_{CB(MIN)}$$

- Determine value of C2:

$$C2 = \frac{45\mu A \times C_L}{I_{INRUSH}}$$

- Calculate value of C1:

$$C1 = (C2 + C_{gd}) \times \left(\frac{V_{IN(MAX)} - V_{GS(TH)}}{V_{GS(TH)}} \right)$$

- Determine value of R3:

$$R3 = \frac{150\mu s}{C2}$$

- Set $R_2 = 10\Omega$.
- If an optocoupler is utilized as in Figure 14, determine the LED series resistor:

$$R7 = \frac{V_{IN(NOMINAL)} - 2V}{3 \leq I_{LED} \leq 5mA}$$

Although the suggested optocoupler is not specified for operation below 5mA, its performance is adequate for 36V temporary low-line voltage where LED current would then be $\approx 2.2\text{mA}$ to 3.7mA . If R7 is set as high as $51\text{k}\Omega$, optocoupler operation should be verified over the expected temperature and input voltage range to ensure suitable operation when LED current $\approx 0.9\text{mA}$ for 48V input and $\approx 0.7\text{mA}$ for 36V input.

If input transients are expected to momentarily raise the input voltage to >100V, select an input transient-voltage-suppression diode (TVS) to limit maximum voltage on the MAX5921/MAX5939 to less than 100V. A suitable device is the Diodes Inc. SMAT70A telecom-specific TVS.

Select Q1 to meet supply voltage, load current, efficiency, and Q1 package power-dissipation requirements:

$$BV_{DSS} \geq 100V$$

$$I_{D(ON)} \geq 3 \times I_{LOAD}$$

DPAK, D²PAK, or TO-220AB

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

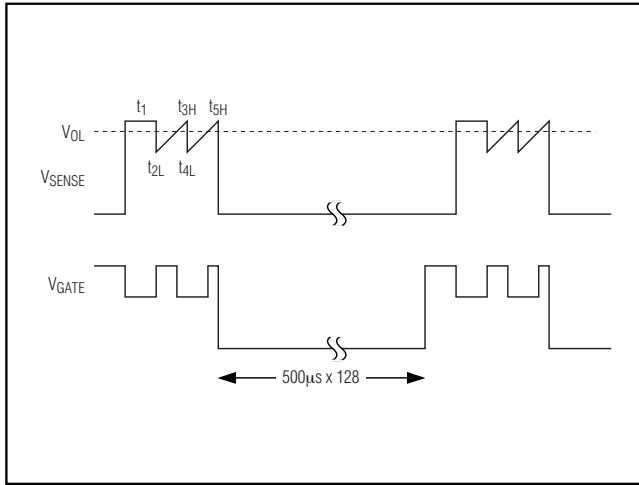


Figure 14. MAX5921A Overcurrent Fault Example

The lowest practical $R_{DS(ON)}$, within budget constraints and with values from $14m\Omega$ to $540m\Omega$, are available at 100V breakdown.

Ensure that the temperature rise of Q1 junction is not excessive at normal load current for the package selected. Ensure that I_{CB} current during voltage transients does not exceed allowable transient-safe operating-area limitations. This is determined from the SOA and transient-thermal-resistance curves in the Q1 manufacturer's data sheet.

Example 1:

$I_{LOAD} = 2.5A$, efficiency = 98%, then $V_{DS} = 0.96V$ is acceptable, or $R_{DS(ON)} \leq 384m\Omega$ at operating temperature is acceptable. An IRL520NS 100V NMOS with $R_{DS(ON)} \leq 180m\Omega$ and $I_{D(ON)} = 10A$ is available in D²PAK. (A Vishay Siliconix SUD40N10-25 100V NMOS with $R_{DS(ON)} \leq 25m\Omega$ and $I_{D(ON)} = 40A$ is available in DPAK but may be more costly because of a larger die size).

Using the IRL520NS, $V_{DS} \leq 0.625V$ even at $+80^{\circ}C$ so efficiency $\geq 98.6\%$ at $80^{\circ}C$. $P_D \leq 1.56W$ and junction temperature rise above case temperature would be $5^{\circ}C$ due to the package $\theta_{JC} = 3.1^{\circ}C/W$ thermal resistance. Of course, using the SUD40N10-25 will yield an efficiency greater than 99.8% to compensate for the increased cost.

If I_{CB} is set to twice I_{LOAD} , or 5A, V_{DS} momentarily doubles to $\leq 1.25V$. If $C_{OUT} = 4000\mu F$, transient-line input voltage is $\Delta 36V$, the 5A charging-current pulse is:

$$t = \frac{4000\mu F \times 1.25V}{5A} = 1ms$$

Entering the data sheet transient-thermal-resistance curves at 1ms provides a $\theta_{JC} = 0.9^{\circ}C/W$. $P_D = 6.25W$, so $\Delta t_{JC} = 5.6^{\circ}C$. Clearly, this is not a problem.

Example 2:

$I_{LOAD} = 10A$, efficiency = 98%, allowing $V_{DS} = 0.96V$ but $R_{DS(ON)} \leq 96m\Omega$. An IRF530 in a D²PAK exhibits $R_{DS(ON)} \leq 90m\Omega$ at $+25^{\circ}C$ and $\leq 135m\Omega$ at $+80^{\circ}C$. Power dissipation is 9.6W at $+25^{\circ}C$ or 14.4W at $+80^{\circ}C$. Junction-to-case thermal resistance is $1.9^{\circ}C/W$, so the junction temperature rise would be approximately $5^{\circ}C$ above the $+25^{\circ}C$ case temperature. For higher efficiency, consider IRL540NS with $R_{DS(ON)} \leq 44m\Omega$. This allows $\eta = 99\%$, $P_D \leq 4.4W$, and $T_{JC} = +4^{\circ}C$ ($\theta_{JC} = 1.1^{\circ}C/W$) at $+25^{\circ}C$.

Thermal calculations for the transient condition yield $I_{CB} = 20A$, $V_{DS} = 1.8V$, $t = 0.5ms$, transient $\theta_{JC} = 0.12^{\circ}C/W$, $P_D = 36W$ and $\Delta t_{JC} = 4.3^{\circ}C$.

Layout Guidelines

Good thermal contact between the MAX5921/MAX5939 and the external MOSFET is essential for the thermal-shutdown feature to operate effectively. Place the MAX5921/MAX5939 as close as possible to the drain of the external MOSFET and use wide circuit-board traces for good heat transfer. See Figure 15 for an example of recommended layout for Kelvin-sensing current through a sense resistor on a PC board.

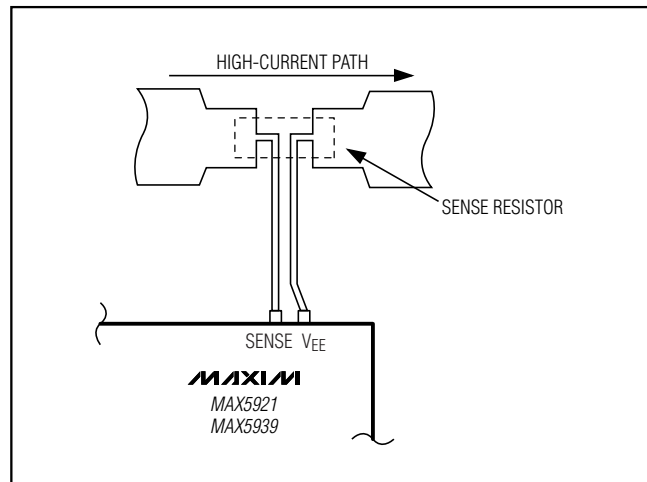


Figure 15. Recommended Layout for Kelvin-Sensing Current Through Sense Resistor

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

Selector Guide

PART	DCEN POLARITY	FAULT MANAGEMENT	MAXIMUM CURRENT-LIMIT DURATION (ms)	MAXIMUM CURRENT-LIMIT DUTY CYCLE
MAX5921AESA	Active-Low $\overline{\text{PWRGD}}$	Autoretry	0.5	1/128
MAX5921BESA	Active-High PWRGD	Autoretry	0.5	1/128
MAX5921EESA	Active-Low $\overline{\text{PWRGD}}$	Autoretry	2	1/128
MAX5921FESA	Active-High PWRGD	Autoretry	2	1/128
MAX5939AESA	Active-Low $\overline{\text{PWRGD}}$	Latched	0.5	1/128
MAX5939BESA	Active-High PWRGD	Latched	0.5	1/128
MAX5939EESA	Active-Low $\overline{\text{PWRGD}}$	Latched	2	1/128
MAX5939FESA	Active-High PWRGD	Latched	2	1/128

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX5921EESA*	-40°C to +85°C	8 SO
MAX5921FESA*	-40°C to +85°C	8 SO
MAX5939 AESA	-40°C to +85°C	8 SO
MAX5939BESA	-40°C to +85°C	8 SO
MAX5939EESA*	-40°C to +85°C	8 SO
MAX5939FESA*	-40°C to +85°C	8 SO

*Future product—contact factory for availability.

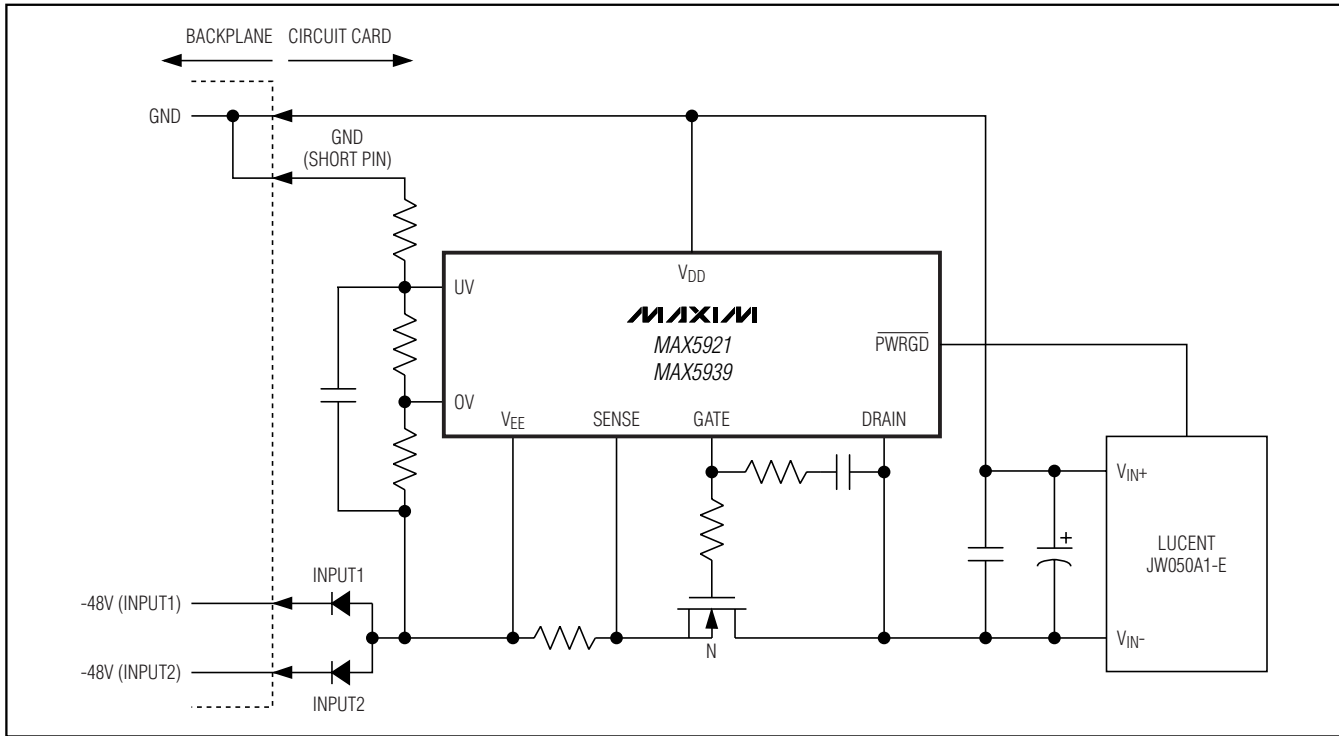
Chip Information

TRANSISTOR COUNT: 2645

PROCESS: BiCMOS

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

Typical Operating Circuit

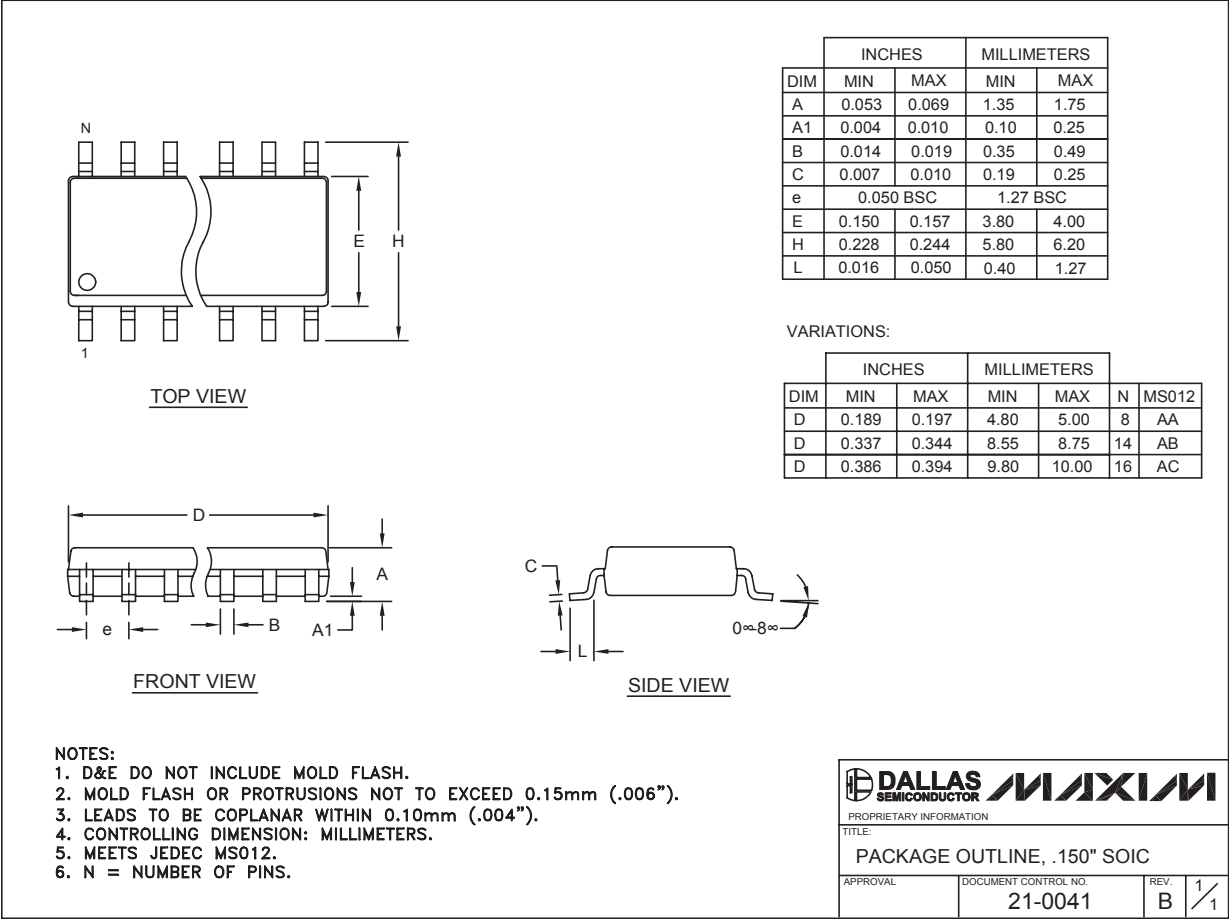


MAX5921/MAX5939

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



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