National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM117-X REV 0A0

Original Creation Date: 09/12/00
Last Update Date: 09/22/00
Last Major Revision Date:

POSITIVE THREE-TERMINAL ADJUSTABLE VOLTAGE REGULATOR

General Description

The LM117 adjustable 3-terminal positive voltage regulator is capable of supplying in excess of 0.5A over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators.

In addition to higher performance than fixed regulators, the LM117 offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, (i.e., avoid short-circuiting the output).

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment pin and output, the LM117 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

Industry Part Number

LM117H

NS Part Numbers

LM117H/883
LM117WG/883

Prime Die

LM117H

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Guaranteed 0.5A output current
- Adjustable output down to 1.2V
- Current limit constant with temperature
- 80 dB ripple rejection
- Output is short-circuit protected

(Absolute Maximum Ratings)

(Note 1)

Power Dissipation (Note 2)	Internally Limited
Input-Output Voltage Differential	+40V, -0.3V
Maximum Junction Temperature	150 C
Storage Temperature Range	-65 C ≤ Ta ≤ +150 C
Lead Temperature (Soldering, 10 seconds)	300 C
Thermal Resistance	
ThetaJA	
Metal Can	
(Still Air)	186 C/W
(500LF/Min Air Flow)	64 C/W
CERAMIC SOIC	
(Still Air)	115 C/W
(500LF/Min Air Flow)	66 C/W
ThetaJC	
Metal Can	21 C/W
CERAMIC SOIC (Note 3, 4)	3.4 C/W
Package Weight (Typical)	
Metal Can	TBD
CERAMIC SOIC	365mg
ESD Tolerance (Note 5)	3000V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum jnnction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: For the CERAMIC SOIC device to function properly, the "Output" and "Output/Sense" pins must be connected on the users printed circuit board.

Note 4: The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using junction-to-ambient, rather than junction-to-case, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out of the package, since the thermal resistance of the leadframe materical is very poor, relatvie to the materical of the package base. The stated junction-to-case thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.

Note 5: Human body model, 1.5K Ohms in series with 100pF.

Recommended Operating Conditions

Operating Temperature Range	-55 C $\leq$ Ta $\leq$ +125 C

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vdiff = Vin - Vout, Il = 8mA

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iadj	Adjustment Pin Current	Vdiff = 3V				100	uA	1
		Vdiff = 3.3V				100	uA	2, 3
		Vdiff = 40V				100	uA	1, 2, 3
Iq	Minimum Load Current	Vdiff = 3V, Vout = 1.7V				5	mA	1
		Vdiff = 3.3V, Vout = 1.7V				5	mA	2, 3
		Vdiff = 40V, Vout = 1.7V				5	mA	1, 2, 3
Vref	Reference Voltage	Vdiff = 3V			1.2	1.3	V	1
		Vdiff = 3.3V			1.2	1.3	V	2, 3
		Vdiff = 40V			1.2	1.3	V	1, 2, 3
Rline	Line Regulation	3V ≤ Vdiff ≤ 40V, Vout = 1.2V			-8.9	8.9	mV	1
		3.3V ≤ Vdiff ≤ 40V, Vout = 1.2V			-22.2	22.2	mV	2, 3
Rload	Load Regulation	Vdiff= 3V, Il = 10mA to 500mA			-15	15	mV	1
		Vdiff= 3.3V, Il = 10mA to 500mA			-15	15	mV	2, 3
		Vdiff= 40V, Il = 10mA to 150mA			-15	15	mV	1
		Vdiff= 40V, Il = 10mA to 100mA			-15	15	mV	2, 3
Delta Iadj	Adjustment Current Change	Vdiff = 3V, Il = 10mA to 500mA			-5	5	uA	1
		Vdiff = 3.3V, Il = 10mA to 500mA			-5	5	uA	2, 3
		Vdiff = 40V, Il = 10mA to 150mA			-5	5	uA	1
		Vdiff = 40V, Il = 10mA to 100mA			-5	5	uA	2, 3
		3V ≤ Vdiff ≤ 40V			-5	5	uA	1
		3.3V ≤ Vdiff ≤ 40V			-5	5	uA	2, 3
Ios	Short Circuit Current	Vdiff = 10V			.45	1.6	A	1
Theta R	Thermal Regulation	TA = 25 C, t = 20mS, Vdiff = 40V, Il = 150mA			-6	6	mV	1
Icl	Current Limit	Vdiff ≤ 15V	1		0.5		A	1, 2, 3
		Vdiff = 40V	1		0.15		A	1

Electrical Characteristics

AC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Rr	Ripple Rejection	Vin =+6.25V, Vout = Vref, f = 120Hz, ei = 1Vrms, Il = 125mA	2		66		dB	4, 5, 6

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vdiff = Vin - Vout, Il = 8mA. "Deltas not required on B-Level product. Deltas required for S-Level product ONLY as specified on Internal Processing Instructions (IPI)."

Iadj	Adjustment Pin Current	Vdiff = 40V			-10	10	uA	1
Vref	Reference Voltage	Vdiff = 3V			-0.01	0.01	V	1

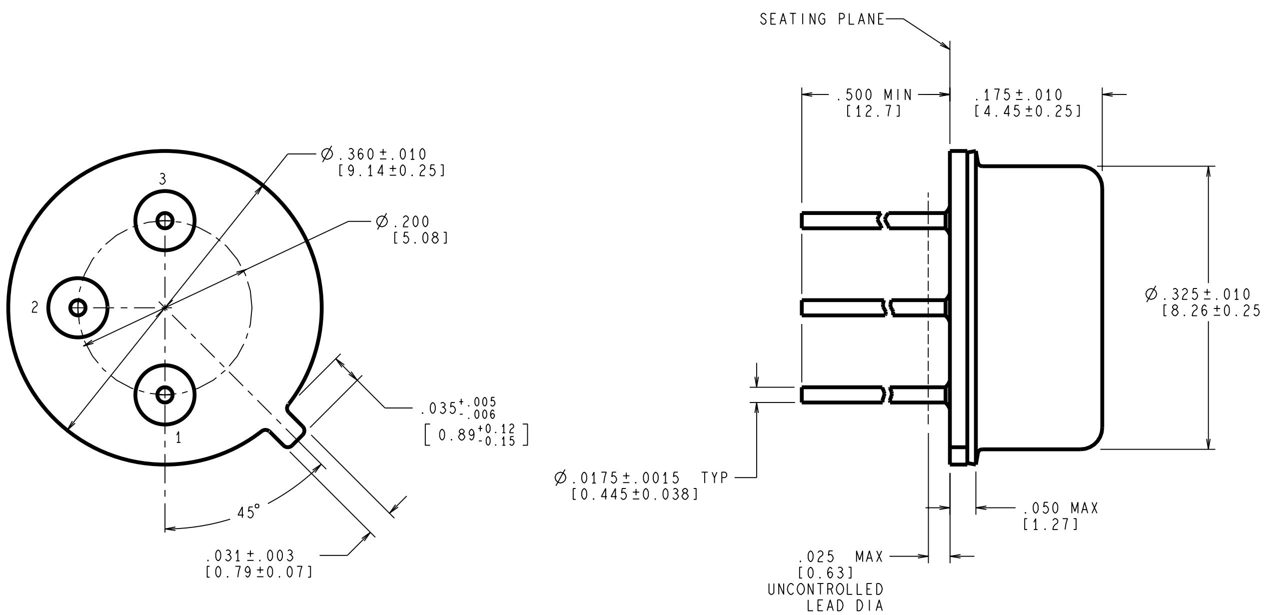
Note 1: Guaranteed parameter not tested
Note 2: Tested at +25 C; guaranteed, but not tested at +125 C and -55 C.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06368HRA1	CERAMIC SOIC (WG), 16 LEAD (B/I CKT)
09784HRB3	METAL CAN (H), TO-39, 3LD, .200 DIA P.C. (B/I CKT)
H03ARD	METAL CAN (H), TO-39, 3LD, .200 DIA P.C. (P/P DWG)
P000174A	METAL CAN (H), TO-39, 3LD, .200 DIA P.C. (PINOUT)
P000385B	CERAMIC SOIC (WG), 16 LEAD (PINOUT)
WG16ARC	CERAMIC SOIC (WG), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
C	REVISE & REDRAW PER NEW STANDARD	10403	05/24/94	TL/GM
D	UPDATE MILAERO STAMP; Ø.325 WAS Ø.326; REVISE TOLERANCES	10798	02/28/95	TL/



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .010 IN/ 0.25 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE, KOVAR.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-39, JEDEC PUBLICATION No. 95.

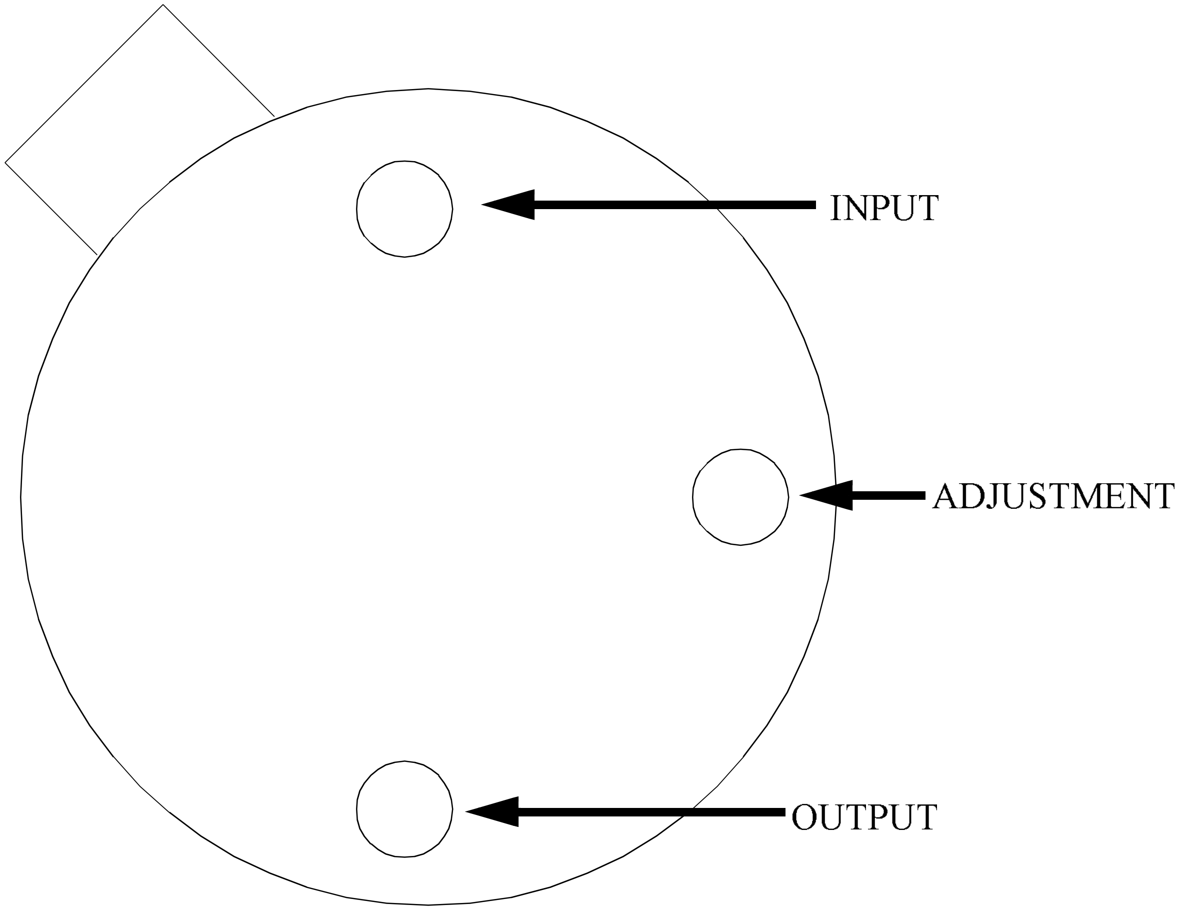
APPROVALS	DATE
DRAWN T. LEQUANG	05/24/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr. Santa Clara, CA 95052-8090

METAL CAN,
TO-39, 3 LEAD,
.200 DIA P.C.

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
INCH [MM]	N/A	C	MKT-H03A	D

DO NOT SCALE DRAWING | SHEET 1 of 1



LM117H, LM117HVH

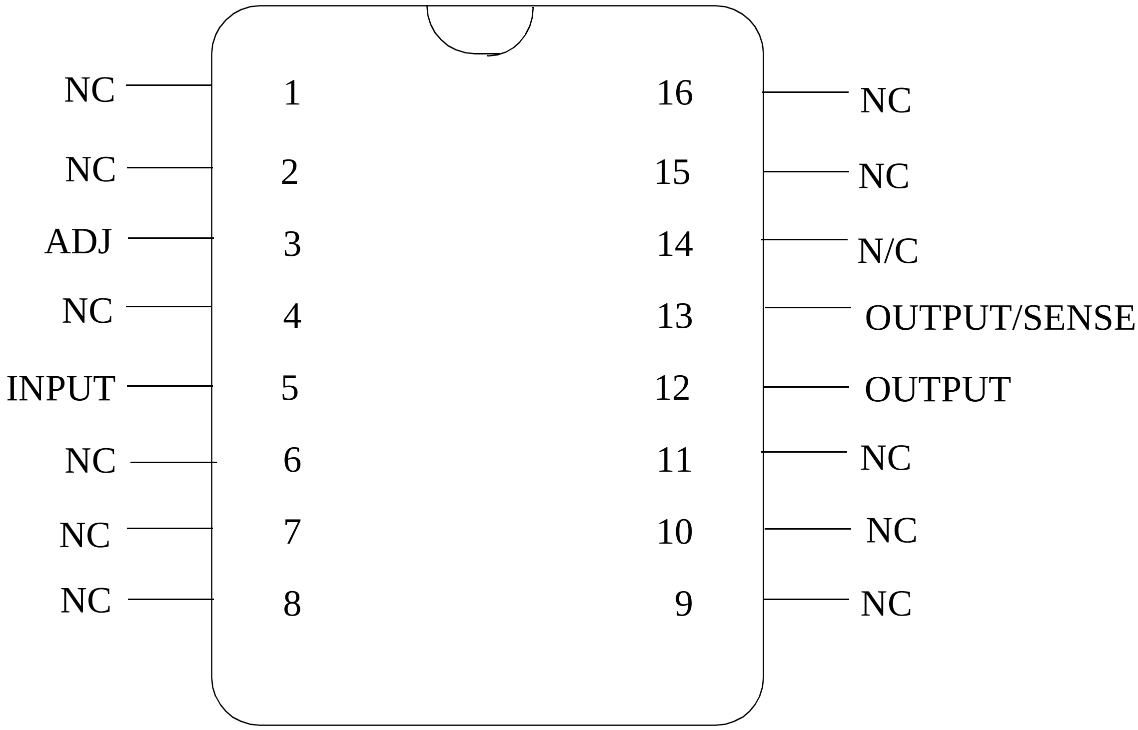
3 - LEAD TO-39

CONNECTION DIAGRAM

BOTTOM VIEW

P000174A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM117WG

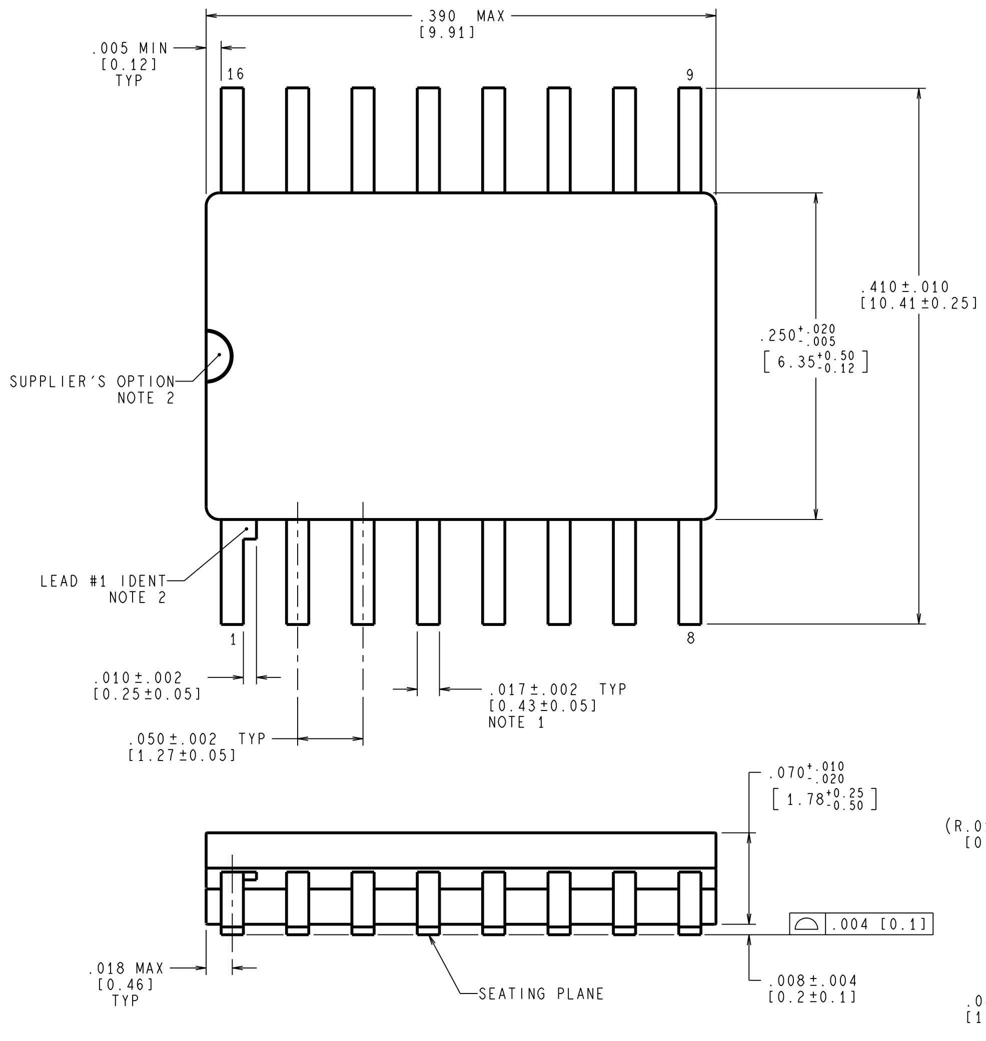
16 - LEAD CERAMIC SOIC

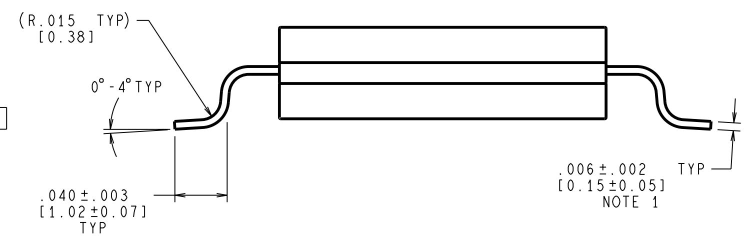
CONNECTION DIAGRAM

TOP VIEW

P000385B

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050





REVISIONS

LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11376	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11443	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11840	10/08/1997	TL/

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK,
16 LEAD,
GULL WING

PROJECTION	SCALE	SIZE	DRAWING NUMBER	REV
INCH [MM]	N/A	C	(SC)MKT-WG16A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003046	09/22/00	Rose Malone	Initial MDS Release: MNLM117-X, Rev. 0A0. Replaced MNLM117-H, Rev. 1A0.