CMOS 4-BIT MICROCONTROLLER

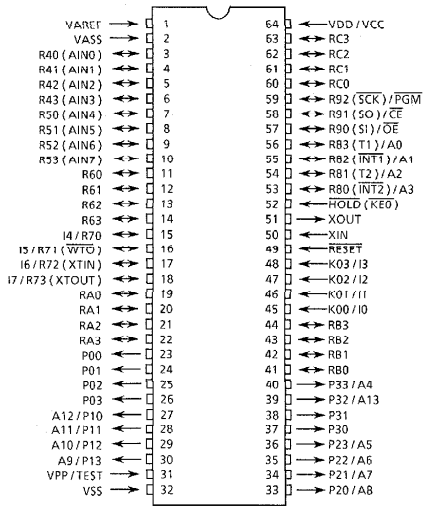
TMP47P1660VN
TMP47P1660VF

The 47P1660V is the system evaluation LSI of 47C1260/1660 with 128K bits one-time PROM. The 47P1660V programs / verifies using an adaptersocket to connect with PROM programmer, as it is in TMM27128AD. In addition, the 47P1660V and the 47C1260/1660 are pin compatible. The 47P1660V operates as the same as the 47C1260/1660 by programming to the internal PROM.

PART No.	ROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P1660VN	OTP	768 × 4-bit	SDIP64-P-750-1.78	BM1130
TMP47P1660VF	16384 × 8-bit		QFP64-P-1420-1.00A	BM1132

PIN ASSIGNMENT (TOP VIEW)

SDIP64-P-750-1.78



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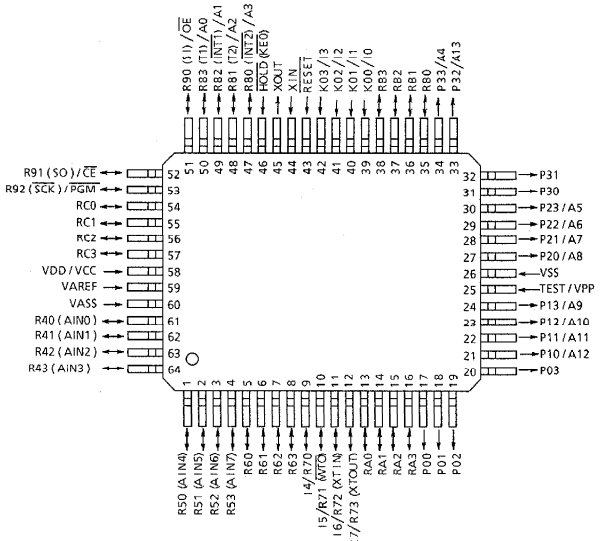

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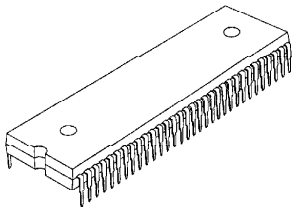

TMP47P1660VN

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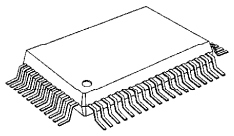


TMP47P1660VF

PIN FUNCTION

The 47P1660V has MCU mode and PROM mode.

(1) MCU mode

The 47C1260/1660 and the 47P1660V are pin compatible (TEST pin for out-going test. Be fixed to low level).

(2) PROM mode

PIN NAME	INPUT / OUTPUT	FUNCTIONS	PIN NAME (MCU mode)
A13	INPUT	Address inputs	P32
A12 - A9			P10 - P13
A8 - A5			P20 - P23
A4			P33
A3 - A0			R80 - R83
I7 - I4	I/O	Data outputs (Inputs)	R73 - R70
I3 - I0			K03 - K00
$\overline{PGM}$	Input	Program control input	R92
$\overline{CE}$		Chip Enable input	R91
$\overline{OE}$		Output Enable input	R90
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
VSS		0V	VSS
P03 - P00	output	Open	
P31 - P30			
RA3 - RA0	I/O		
RB3 - RB0			
RC3 - RC0			
R43 - R40		Be fixed to Low Level	
R53 - R50			
R63 - R60			
$\overline{RESET}$	Input	PROM mode setting pin. Be fixed to low level.	
$\overline{HOLD}$	Input		
XIN	Input	Resonator connecting pin	
XOUT	output		
VAREF	Power supply	Be fixed to low level	
VASS			

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P1660V. The 47P1660V is the same as the 47C1260/1660 except that an OTP is used instead of a built-in mask ROM.

1. OPERATION mode

The 47P1660V has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C1260/1660, except that the TEST/VPP pin does not have built in pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C1660. Data conversion tables must be set in two locations when using the 47P1660V to check 47C1260 operation.

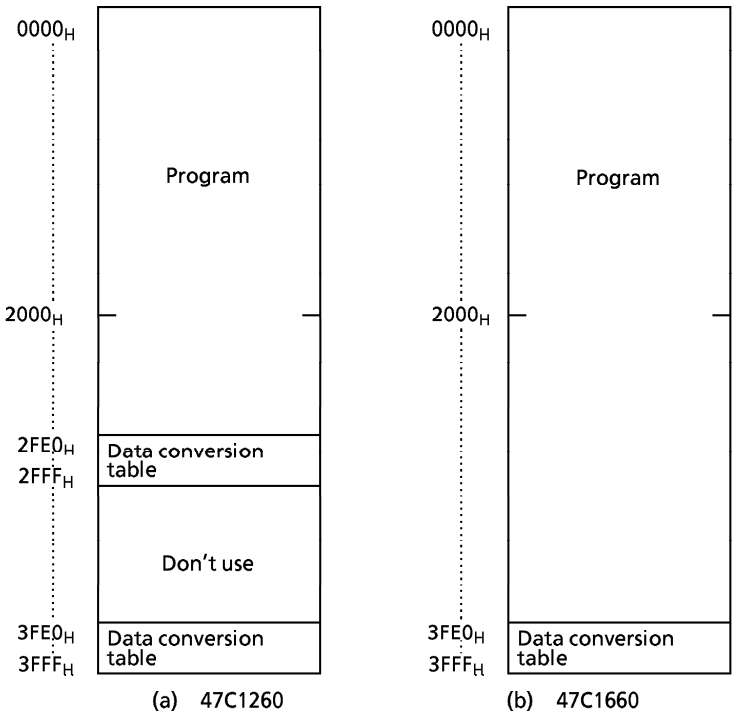


Figure 1-1. Program area

1.1.2 Data Memory

The 47P1660V has 768 × 4-bit of data memory (RAM), 256 × 4-bit (addresses 00_H through FF_H) on each of banks (bank 0, bank 1 and bank 2).

1.1.3 Input/Output Circuitry

(1) Control pins
This is the same as for the 47C1260/1660 except that there is no built-in pull-down resistance for the TEST pin.

(2) I/O Ports
The input/output circuit of the 47P1660V is the same as I/O code IA of the 47C1260/1660.
External resistance, for example, is required when using as evaluator of other I/O codes (IB, IC), (Refer to Figure 1-2)

(a) Equivalent to IO code IB (b) Equivalent to IO code IC

Figure 1-2. I/O code and external circuitry

1.2 PROM mode

The PROM mode is set by setting the $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$ pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM 27128AD.)

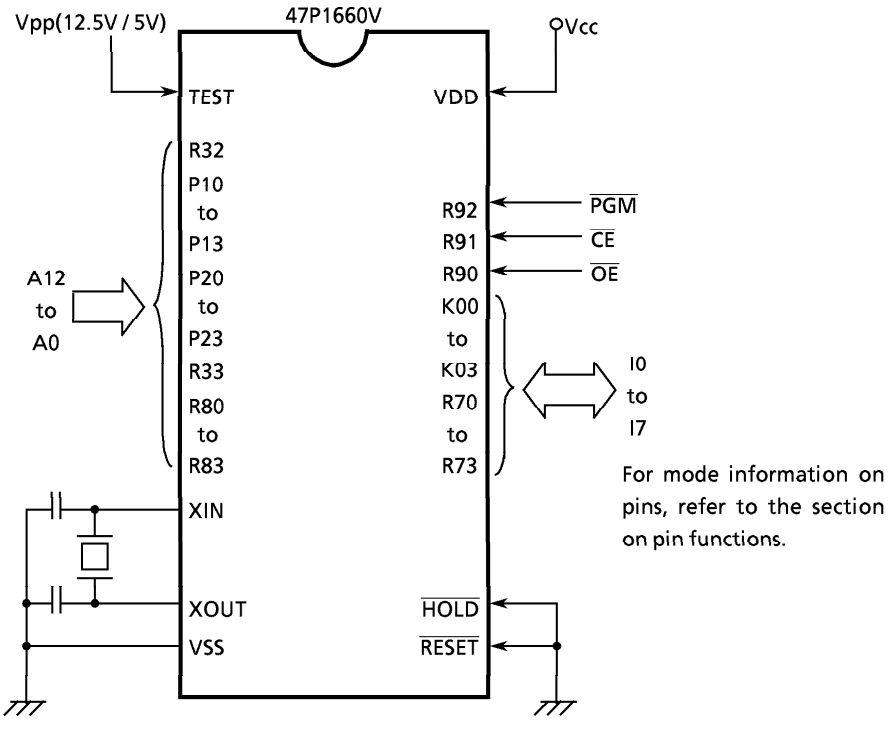


Figure 1-3. Setting for PROM mode

1.2.1 High Speed Programming Mode

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+ 12.5V) is applied to the V_{PP} terminal with V_{CC} = 6V and $\overline{PGM}$ = V_{IH}.

The programming is achieved by applying a single low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC} = V_{PP} = 5V.

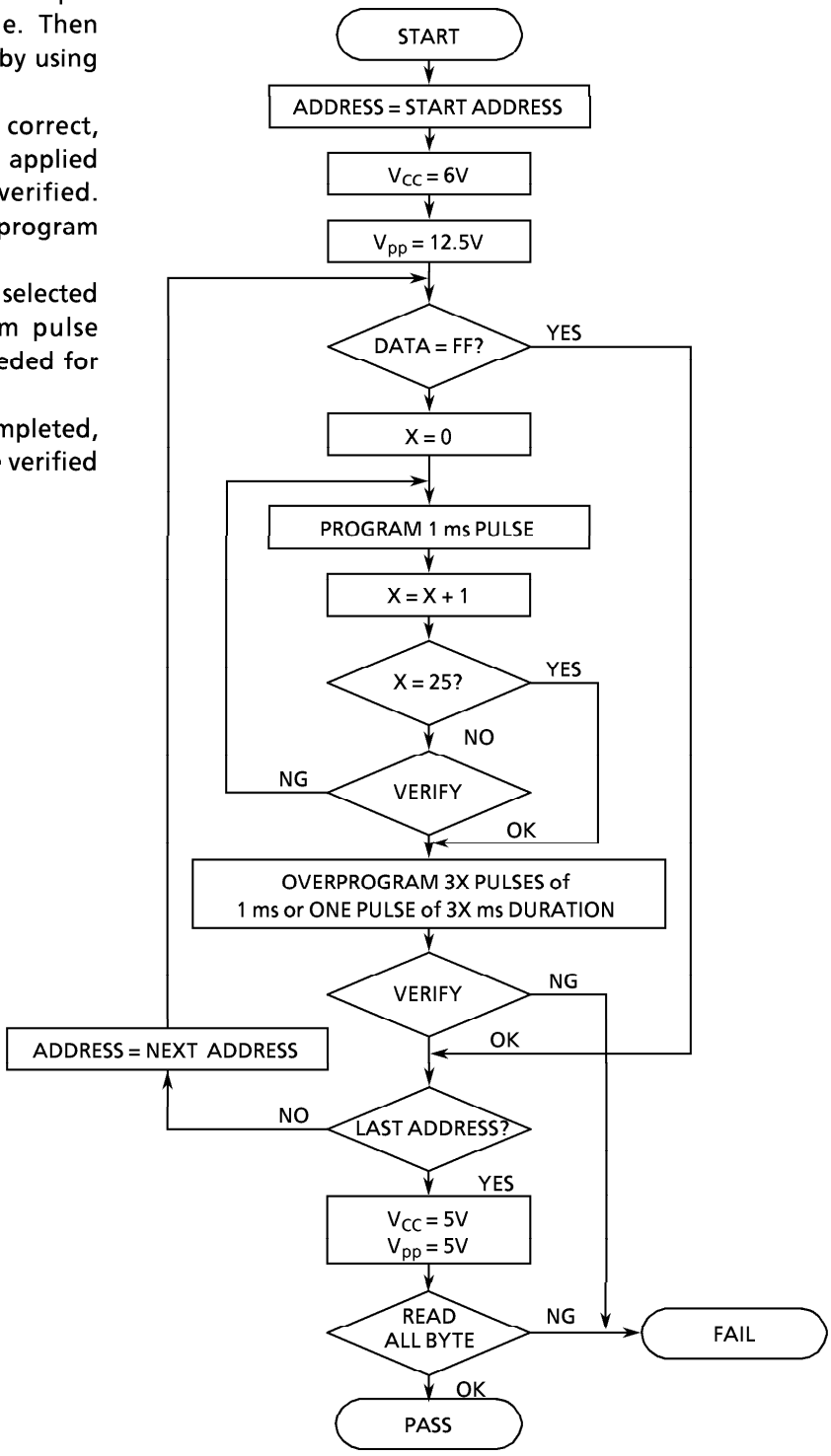


Figure 1-4. Flow Chart

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.3 to 7	V
Program Voltage	V_{PP}	TEST / VPP pin	− 0.3 to 14.0	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Ports R4, R5, R7, push-pull	− 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Ports P1, P2, R6, R8, R9	− 0.3 to 10	
Output (Per 1 pin)	I_{OUT1}	Port R	3.2	mA
	I_{OUT2}	Ports P1, P2	30	
	I_{OUT2}	Ports P0, P3	15	
Output Current (Total)	ΣI_{OUT1}	Ports P0, P1	120	mA
	ΣI_{OUT2}	Ports P2, P3	120	
Power Dissipation	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	℃
Storage Temperature	T_{stg}		− 55 to 125	℃
Operating Temperature	T_{opr}		− 40 to 70	℃

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, Topr = − 40 to 70℃)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	4.5	6.0	V
			in the SLOW mode	2.7		
			in the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc		High-freq.clock	0.4	6.0	MHz
	fs		Low-freq.clock	30	34	kHz

Note. Input Voltage V_{IH3}, V_{IL3} : in the SLOW mode or HOLD mode

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = – 40 to 70℃)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis input		—	0.7	—	V
Input Current	I_{IN1}	port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	ports R (open-drain)					
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Low Level Input Current	I_{IL}	ports R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	—	—	– 2	mA
Output Leakage Current	I_{LO}	ports R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
Output Level High Voltage	V_{OH}	push-pull ports	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	—	—	V
Output Level Low Voltage	V_{OL}	Except XOUT, P ports	V_{DD} = 4.5V, I_{OL} = 1.6mA	—	—	0.4	
Low Level Output Current	I_{OL2}	ports P1, P2	V_{DD} = 4.5V, V_{OL} = 1.0V	—	20	—	mA
	I_{OL3}	ports P0, P3		—	7	—	
Supply Current (in the Nomal mode)	I_{DD}		V_{DD} = 5.5V fc = 4MHz	—	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 5.0V fs = 32.768kHz	—	30	60	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	—	0.5	10	μA

Note 1. *Typ. values show those at T_{opr} = 25℃, V_{DD} = 5V.*

Note 2. *Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.*

Note 3. *I_{DD}, I_{DDH}; V_{IN} = 5.3V / 0.2V*
The voltage applied to the R port is within the valid range.
I_{DDS}; V_{IN} = 2.8V / 0.2V, low frequency clock is only oscillated (connecting XTIN, XTOUT).

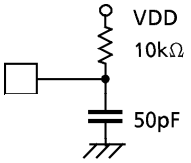
A / D CONVERSION CHARACTERRISTICS (T_{opr} = – 40 to 70℃)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference	V_{AREF}		V_{DD} – 1.5	—	V_{DD}	V
	V_{ASS}		V_{SS}	—	1.5	
Analog Reference Voltage Range	$\triangle V_{AREF}$	$V_{AREF} - V_{ASS}$	2.5	—	—	V
Analog input Voltage	V_{AIN}		V_{ASS}	—	V_{AREF}	V
Analog Supply Current	I_{REF}		—	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 4.5 to 6.0V, V_{SS} = 0.0V V_{AREF} = V_{DD} ± 0.001V V_{ASS} = 0.000V	—	—	± 1	LSB
Zero pornt Error			—	—	± 1	
Full scale Error			—	—	± 1	
Totar Error			—	—	± 2	

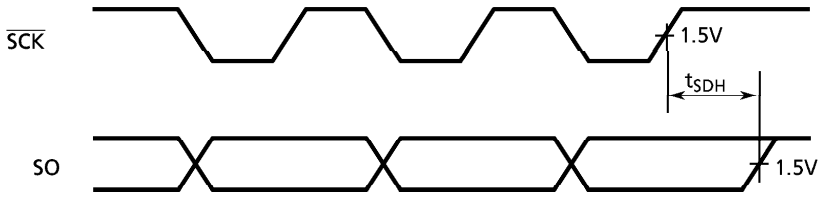
A.C. CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70℃)

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	in the Normal mode	1.33	–	20	μs
		in the SLOW mode	235	–	267	
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low level Clock Pulse Width	t_{WCL}					
A / D Conversion Sampling Time	t_{AIN}	fc = 4MHz	–	2	–	μs
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	–	–	ns

Note. Shift data Hold Time:
External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



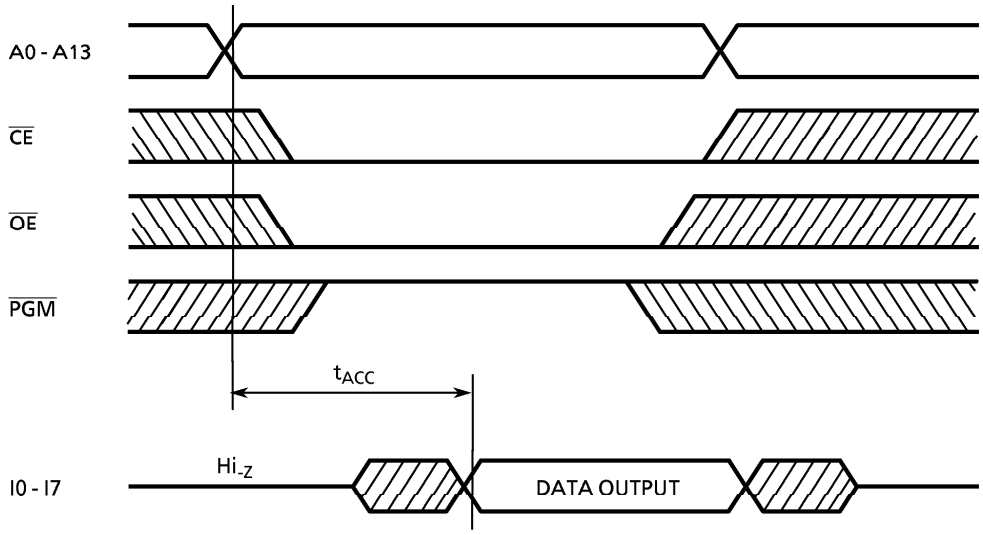
RECOMMENDED OSCILLATING CONDITIONS (V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70℃)

Recommended oscillating conditions of the 47P1660V are equal to the 47C1660's.

DC/AC CHARACTERISTICS (V_{SS} = 0V)

(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25V	0	–	350	ns



(2) High Speed Programming Operation

PARAMETER	SYBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.25	12.50	12.75	V
Programming Pulse Width	t_{PW}	$V_{CC} = 6.0 \pm 0.25V$	0.95	1.0	1.05	ms