



3.3V CMOS 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16721

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP, and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels (0.4 μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16721:

- High Output Drivers: $\pm 24\text{mA}$
- Suitable for heavy loads

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

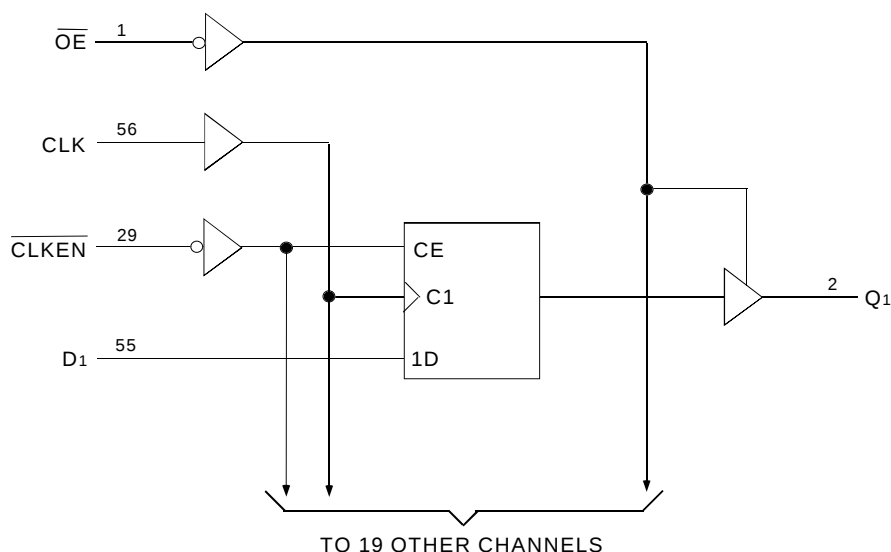
This 20-bit flip-flop is built using advanced dual metal CMOS technology. The 20 flip-flops of the ALVCH16721 are edge-triggered D-type flip-flops with qualified clock storage. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs if the clock-enable (CLKEN) input is low. If CLKEN is high, no data is stored.

A buffered output-enable ($\overline{\text{OE}}$) input places the 20 outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components. $\overline{\text{OE}}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

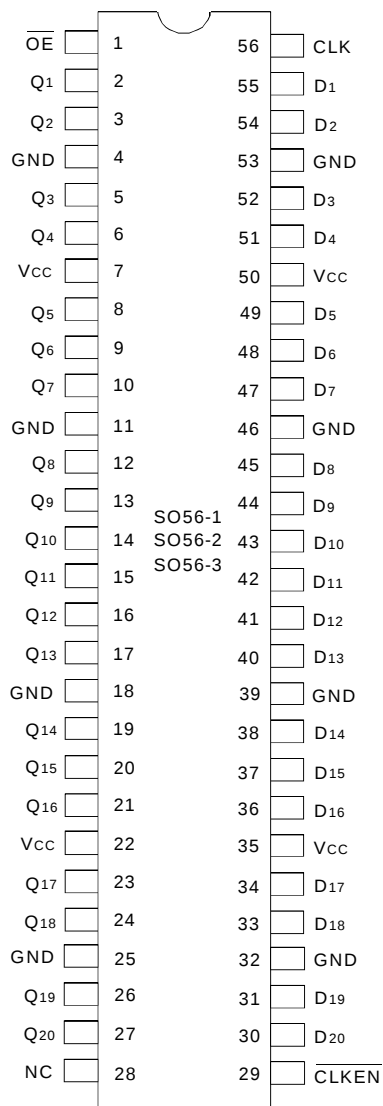
The ALVCH16721 has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16721 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistor.

Functional Block Diagram



PIN CONFIGURATION



SSOP/TSSOP/TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	3-State Output Enable Input (Active LOW)
Dx	Data Inputs ⁽¹⁾
Qx	3-State Outputs
CLK	Clock Input
$\overline{CLKEN}$	Clock Enable Input (Active LOW)
NC	No Internal Connection

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATING ⁽¹⁾

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	– 0.5 to V _{CC} + 0.5	V
TSTG	Storage Temperature	– 65 to + 150	°C
I _{OUT}	DC Output Current	– 50 to + 50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > V _{CC}	± 50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	– 50	mA
I _{CC} I _{SS}	Continuous Current through each V _{CC} or GND	±100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

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NOTE:

- As applicable to the device type.

FUNCTION TABLE (each flip-flop) ⁽¹⁾

Inputs				Output
$\overline{OE}$	$\overline{CLKEN}$	CLK	Dx	Qx
L	H	X	X	Q ₀
L	L	↑	H	H
L	L	↑	L	L
L	L	L or H	X	Q ₀
H	X	X	X	Z

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
Q₀ = Indicates the previous state

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH}	Input HIGH Current	V _{CC} = 3.6V	V _I = V _{CC}	—	—	± 5	μA
I _{IL}	Input LOW Current	V _{CC} = 3.6V	V _I = GND	—	—	± 5	
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = V _{CC}	—	—	± 10	μA
			V _O = GND	—	—	± 10	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = – 18mA		—	– 0.7	– 1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCL} I _{CCH} I _{CCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V V _{IN} = GND or V _{CC}		—	0.1	40	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} – 0.6V, other inputs at V _{CC} or GND		—	—	750	μA

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NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 3.0V	V _I = 2.0V	– 75	—	—	μA
			V _I = 0.8V	75	—	—	
I _{BHH} I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	– 45	—	—	μA
			V _I = 0.7V	45	—	—	
I _{BHHO} I _{BHLO}	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	± 500	μA

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NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = – 0.1mA	V _{CC} – 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = – 6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = – 12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3.0V		2.4	—	
		V _{CC} = 3.0V	I _{OH} = – 24mA	2	—	
VOL	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.55	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to + 85°C.

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OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V _{CC} = 2.5V ± 0.2V	V _{CC} = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C _L = 0pF, f = 10MHz	55	59	pF
CPD	Power Dissipation Capacitance Outputs disabled		46	49	pF

SWITCHING CHARACTERISTICS ⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		150	—	150	—	150	—	MHz
t _{PLH} t _{PHL}	Propagation Delay CLK to Q _x	1	5.6	1	5.1	1	4.3	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{\text{OE}}$ to Q _x	1	6.1	1	5.8	1	4.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{\text{OE}}$ to Q _x	1	5.5	1	4.7	1	4.4	ns
t _{SU}	Setup Time, data before CLK $\uparrow$	4	—	3.6	—	3.1	—	ns
t _{SU}	Setup Time $\overline{\text{CLKEN}}$ before CLK $\uparrow$	3.4	—	3.1	—	2.7	—	ns
t _H	Hold Time, data after CLK $\uparrow$	0	—	0	—	0	—	ns
t _H	Hold Time, $\overline{\text{CLKEN}}$ after CLK $\uparrow$	0	—	0	—	0	—	ns
t _W	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t _{sk(o)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

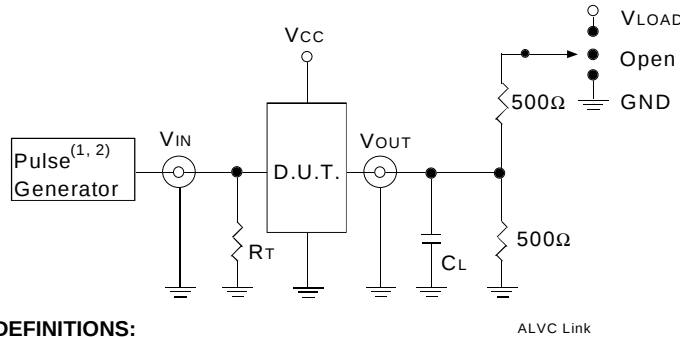
TEST CIRCUITS AND WAVEFORMS:

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

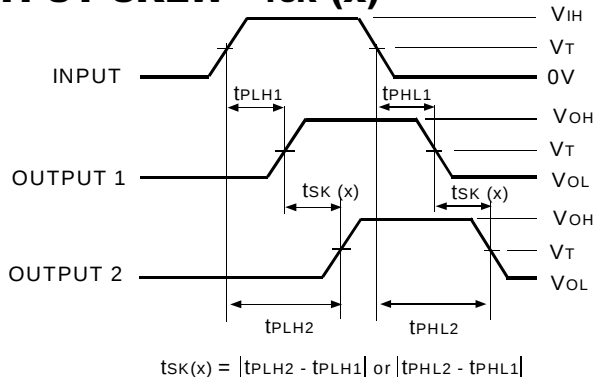
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)

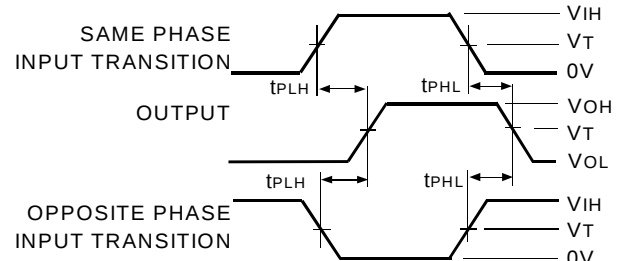


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NOTES:

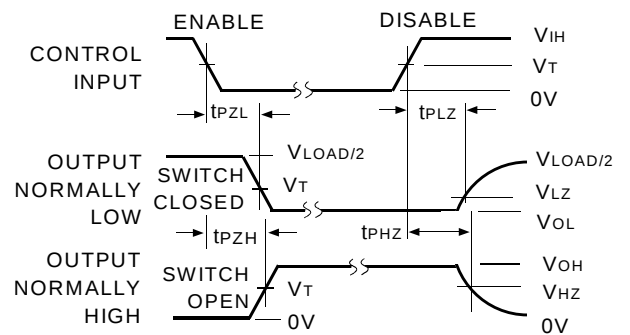
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

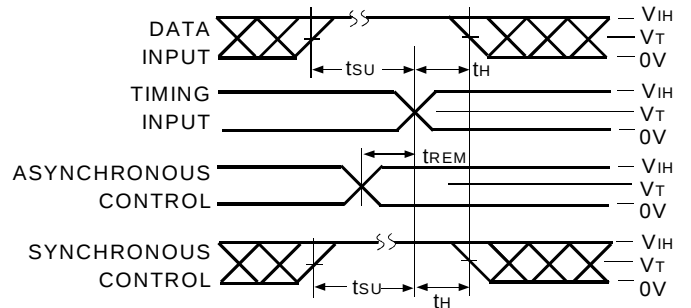


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NOTE:

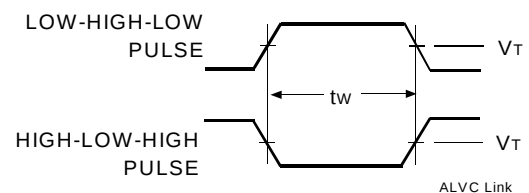
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	ALVC	X	XXX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
						721	20-Bit Flip-Flop with 3-State Outputs
						16	Double-Density with Resistors, $\pm 24\text{mA}$
						H	Bus-Hold
						74	-40°C to $+85^{\circ}\text{C}$



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