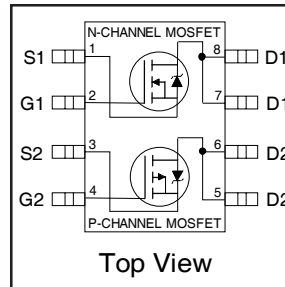


IRF7509PbF

HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Dual N and P Channel MOSFET
- Very Small SOIC Package
- Low Profile (<1.1mm)
- Available in Tape & Reel
- Fast Switching
- Lead-Free

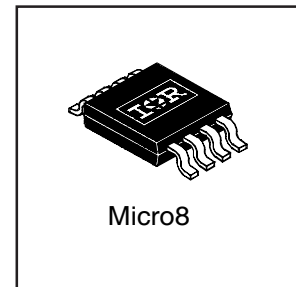


	N-Ch	P-Ch
V_{DS}	30V	-30V
$R_{DS(on)}$	0.11 Ω	0.20 Ω

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The new Micro8 package, with half the footprint area of the standard SO-8, provides the smallest footprint available in an SOIC outline. This makes the Micro8 an ideal device for applications where printed circuit board space is at a premium. The low profile (<1.1mm) of the Micro8 will allow it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.



Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	30	-30	V
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, V_{GS}	2.7	-2.0	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, V_{GS}	2.1	-1.6	A
I_{DM}	Pulsed Drain Current ^①	21	-16	A
$P_D @ T_A = 25^\circ\text{C}$	Maximum Power Dissipation ^④	1.25		W
$P_D @ T_A = 70^\circ\text{C}$	Maximum Power Dissipation ^④	0.8		W
	Linear Derating Factor	10		mW/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
V_{GSM}	Gate-to-Source Voltage Single Pulse $t_p < 10\mu\text{s}$	30		V
dv/dt	Peak Diode Recovery dv/dt ^②	5.0		V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C
	Soldering Temperature, for 10 seconds	240 (1.6mm from case)		

Thermal Resistance

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ^④	100	°C/W

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
		P-Ch	-30	—	—		$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.059	—	$V/^\circ\text{C}$	Reference to 25°C , $I_D = 1\text{mA}$
		P-Ch	—	-0.039	—		Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	0.09	0.110	Ω	$V_{GS} = 10V, I_D = 1.7A$ ④
			—	0.14	0.175		$V_{GS} = 4.5V, I_D = 0.85A$ ④
		P-Ch	—	0.17	0.20		$V_{GS} = -10V, I_D = -1.2A$ ④
			—	0.30	0.40		$V_{GS} = -4.5V, I_D = -0.6A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		P-Ch	-1.0	—	—		$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	N-Ch	1.9	—	—	S	$V_{DS} = 10V, I_D = 0.85A$ ④
		P-Ch	0.92	—	—		$V_{DS} = -10V, I_D = -0.6A$ ④
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		P-Ch	—	—	-1.0		$V_{DS} = -24V, V_{GS} = 0V$
		N-Ch	—	—	25		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
		P-Ch	—	—	-25		$V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	± 100		$V_{GS} = \pm 20V$
Q_g	Total Gate Charge	N-Ch	—	7.8	12		N-Channel $I_D = 1.7A, V_{DS} = 24V, V_{GS} = 10V$ ④
		P-Ch	—	7.5	11		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	1.2	1.8	nC	P-Channel $I_D = -1.2A, V_{DS} = -24V, V_{GS} = -10V$ ④
		P-Ch	—	1.3	1.9		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	2.5	3.8		N-Channel $V_{DD} = 15V, I_D = 1.7A, R_G = 6.1\Omega,$ $R_D = 8.7\Omega$ ④
		P-Ch	—	2.5	3.7		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	4.7	—		P-Channel $V_{DD} = -15V, I_D = -1.2A, R_G = 6.2\Omega,$ $R_D = 12\Omega$ ④
		P-Ch	—	9.7	—		
t_r	Rise Time	N-Ch	—	10	—	ns	N-Channel $V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$ ③
		P-Ch	—	12	—		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	12	—		P-Channel $V_{GS} = 0V, V_{DS} = -25V, f = 1.0\text{MHz}$ ③
		P-Ch	—	19	—		
t_f	Fall Time	N-Ch	—	5.3	—		N-Channel $T_J = 25^\circ\text{C}, I_F = 1.7A, di/dt = 100A/\mu s$ ③
		P-Ch	—	9.3	—		
C_{iss}	Input Capacitance	N-Ch	—	210	—	pF	P-Channel $T_J = 25^\circ\text{C}, I_F = -1.2A, di/dt = -100A/\mu s$ ③
		P-Ch	—	180	—		
C_{oss}	Output Capacitance	N-Ch	—	80	—		
		P-Ch	—	87	—		
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	32	—		
		P-Ch	—	42	—		

Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	1.25	A	
		P-Ch	—	—	-1.25		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	21		
		P-Ch	—	—	-16		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 1.7A, V_{GS} = 0V$ ③
		P-Ch	—	—	-1.2		$T_J = 25^\circ\text{C}, I_S = -1.8A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	N-Ch	—	40	60	ns	
		P-Ch	—	30	45		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	48	72	nC	
		P-Ch	—	37	55		

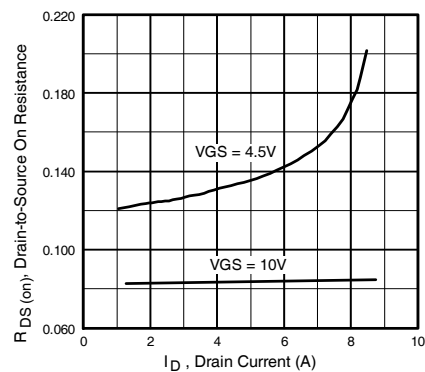
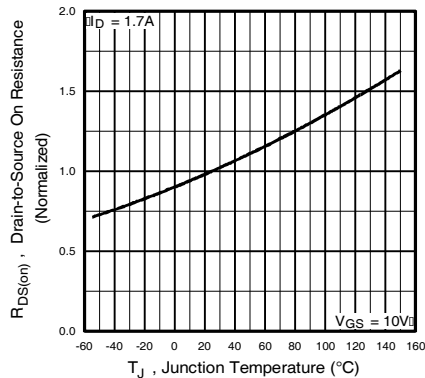
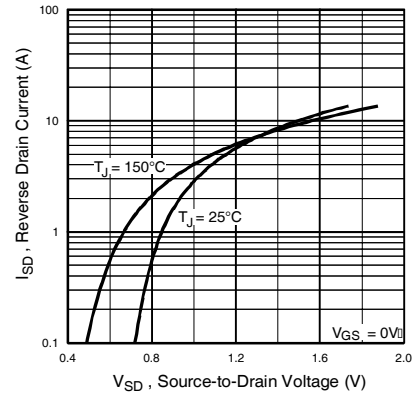
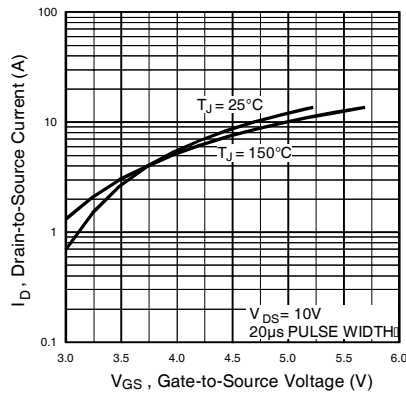
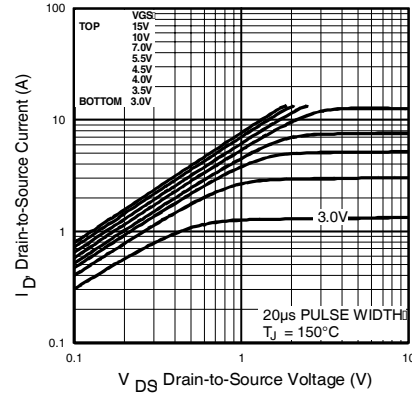
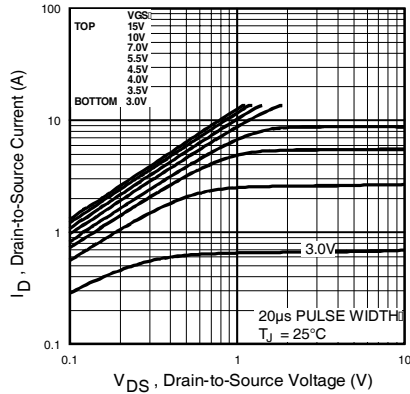
Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 21)

③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

② N-Channel $I_{SD} \leq 1.7A, di/dt \leq 120A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
P-Channel $I_{SD} \leq -1.2A, di/dt \leq 160A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

④ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.



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N - Channel

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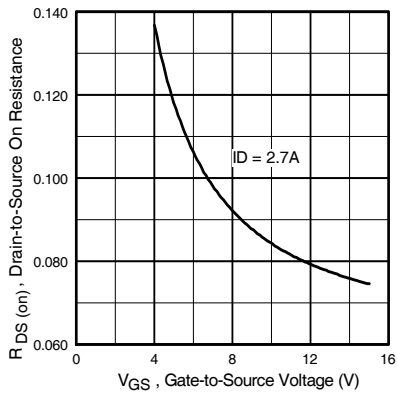


Fig 7. Typical On-Resistance Vs. Gate Voltage

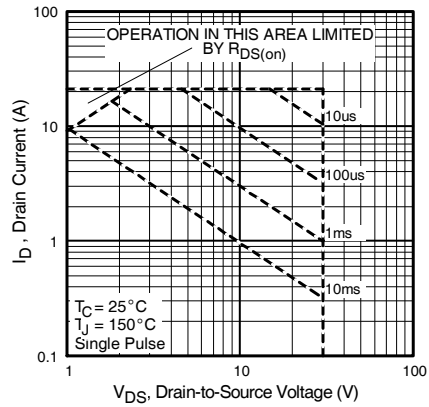


Fig 8. Maximum Safe Operating Area

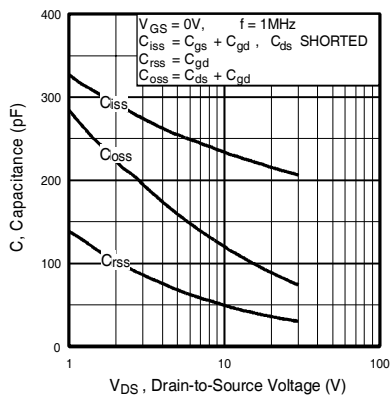


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

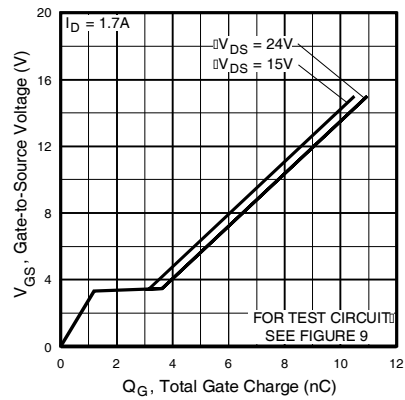


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

P - Channel

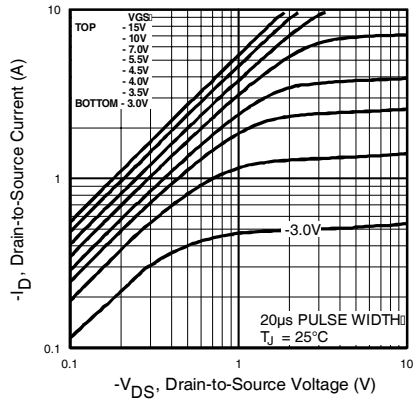


Fig 11. Typical Output Characteristics

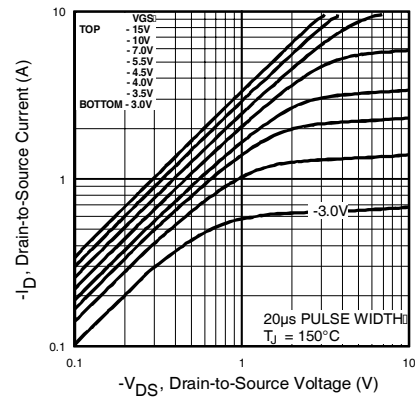


Fig 12. Typical Output Characteristics

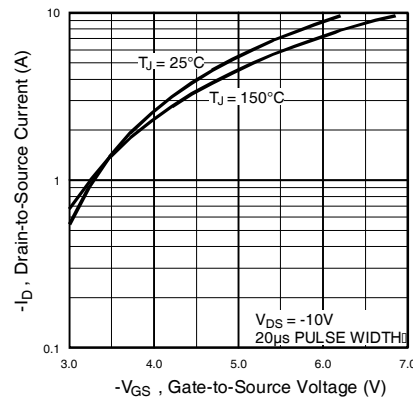


Fig 13. Typical Transfer Characteristics

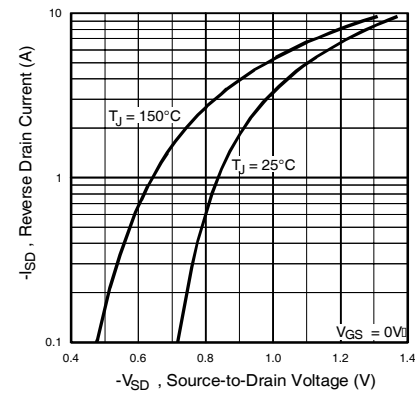


Fig 14. Typical Source-Drain Diode Forward Voltage

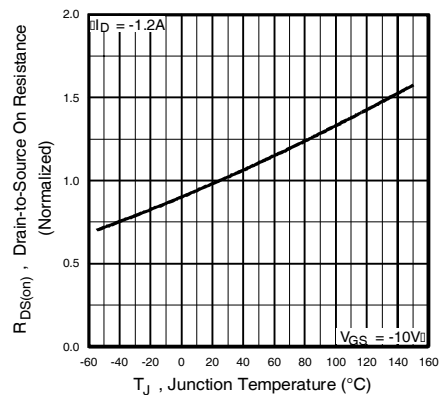


Fig 15. Normalized On-Resistance Vs. Temperature

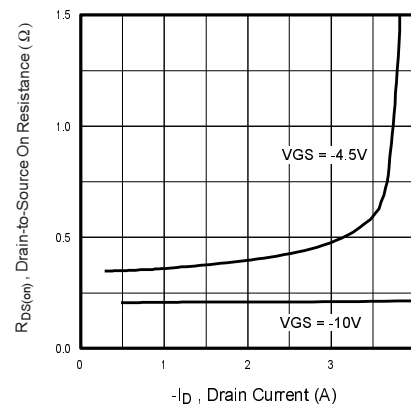


Fig 16. Typical On-Resistance Vs. Drain Current

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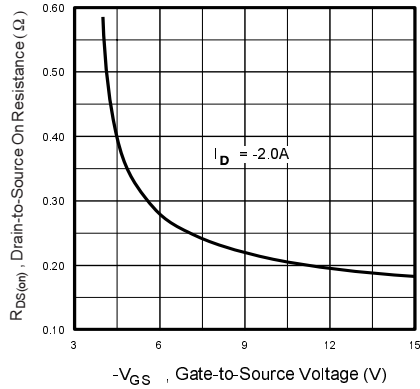


Fig 17. Typical On-Resistance Vs. Gate Voltage

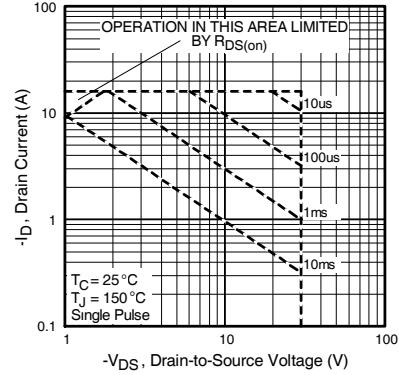


Fig 18. Maximum Safe Operating Area

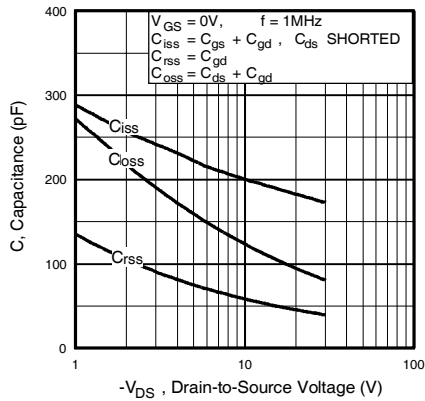


Fig 19. Typical Capacitance Vs. Drain-to-Source Voltage

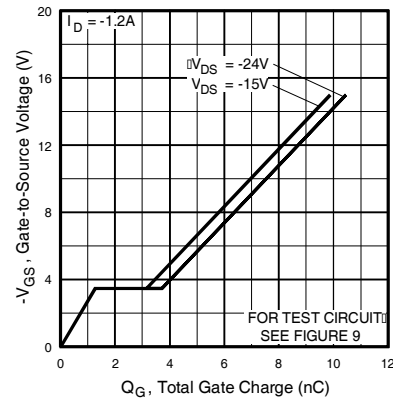


Fig 20. Typical Gate Charge Vs. Gate-to-Source Voltage

N-P - Channel

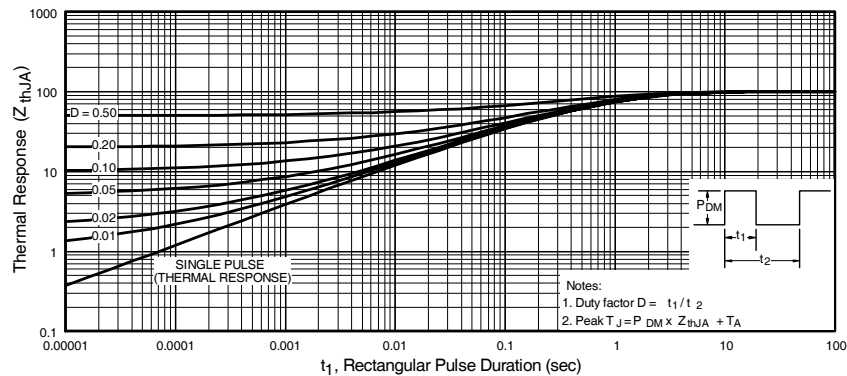
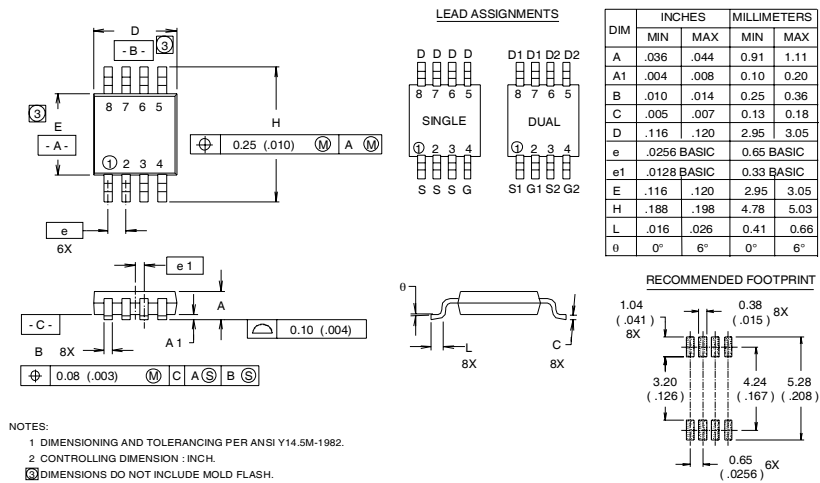


Fig 21. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

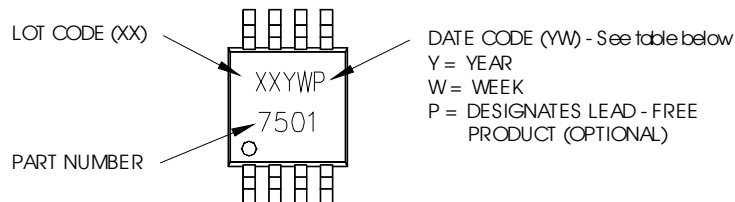
Micro8 Package Outline

Dimensions are shown in millimeters (inches)



Micro8 Part Marking Information

EXAMPLE: THIS IS AN IRF7501



WW = (1-26) IF PRECEDED BY LAST DIGIT OF CALENDAR YEAR

YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
2004	4	04	D
2005	5		
2006	6		
2007	7		
2008	8		
2009	9		
2010	0	24	X
		25	Y
		26	Z

WW = (27-52) IF PRECEDED BY A LETTER

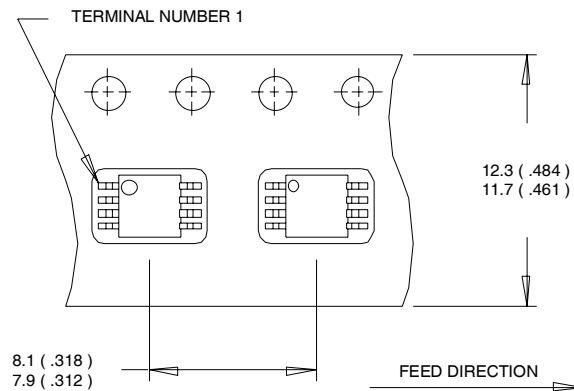
YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
2004	D	30	D
2005	E		
2006	F		
2007	G		
2008	H		
2009	J		
2010	K	50	X
		51	Y
		52	Z

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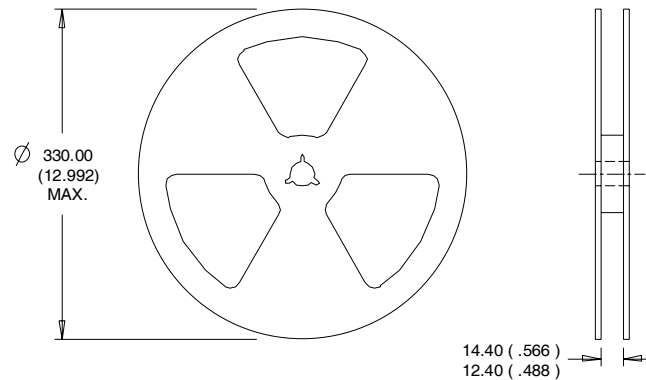
Micro8 Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. CONTROLLING DIMENSION : MILLIMETER.



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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