HIGH-BANDWIDTH DUAL SPDT DIFFERENTIAL SIGNAL SWITCH WITH INPUT LOGIC TRANSLATION

Check for Samples: TS3DS26227

FEATURES

- High-Bandwidth Data Paths – Up to 800 MHz
- Specified Break-Before-Make Switching
- Control Inputs Reference to V_{IO}
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 2.3-V to 3.6-V Power Supply (V_+)
- 1.65-V to 1.95-V Logic Supply (V_{IO})
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 4000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
  - 200-V Machine Model (A115-A)

APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Low-Voltage Differential Signal Routing
- Mobile Industry Processor Interface (MIPI) Signal Routing

YZT PACKAGE (BOTTOM VIEW)

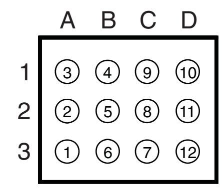


Table 1. TERMINAL ASSIGNMENTS

	A	B	C	D
1	IN1	NO1	COM1	NC1
2	V_{IO}	GND	GND	V_+
3	IN2	NO2	COM2	NC2

DESCRIPTION/ORDERING INFORMATION

The TS3DS26227 is a dual single-pole double-throw (SPDT) analog switch that is designed to operate from 2.3 V to 3.6 V. The device offers high-bandwidth data paths, and a break-before-make feature to prevent signal distortion during the transferring of a signal from one path to another. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable applications.

The TS3DS26227 has a separate logic supply pin (V_{IO}) that operates from 1.65 V to 1.95 V. V_{IO} powers the control circuitry, which allows the TS3DS26227 to be controlled by 1.8-V signals.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZT (Pb-free)	Tape and reel	TS3DS26227YZTR	

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) YZT: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

Table 2. SUMMARY OF CHARACTERISTICS(1)

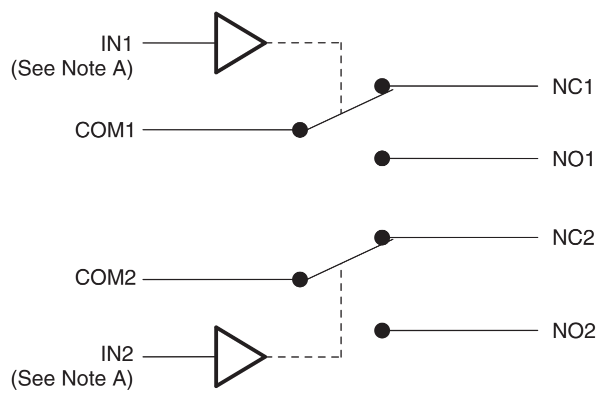
Configuration	Dual 2:1 Multiplexer/Demultiplexer (2 × SPDT)
Number of channels	2
ON-state resistance (r_{on})	5 Ω max
ON-state resistance match (Δr_{on})	0.1 Ω max
ON-state resistance flatness [$r_{on(flat)}$]	3 Ω max
Turn-on/turn-off time (t_{ON}/t_{OFF})	9 ns/4 ns
Break-before-make time (t_{BBM})	8 ns
Charge injection (Q_C)	5.5 pC
Bandwidth (BW)	800 MHz
OFF isolation (O_{ISO})	–40 dB
Crosstalk (X_{TALK})	–39 dB
Leakage current [$I_{NO(OFF)}/I_{NC(OFF)}$]	±5 nA
Power-supply current (I_+)	±20 nA
Package options	12-bump WCSP

(1) $V_+ = 2.7$ V, $T_A = 25°C$

Table 3. FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

LOGIC DIAGRAM



A. IN1 and IN2 are control inputs referenced to V_{IO}.

ABSOLUTE MAXIMUM RATINGS[1] [2]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+ V_{IO}	Supply voltage range[3]		–0.5	4.6	V
V_{NC} V_{NO} V_{COM}	Analog voltage range[3] [4] [5]		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0, or V_{NC}, V_{NO}, V_{COM} > V_+ + 0.5	–50	50	mA
I_{NC} I_{NO} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	–64	64	mA
	On-state peak switch current		–100	100	
V_I	Digital input voltage range		–0.5	V_{IO} + 0.5	V
I_{IK}	Digital input clamp current[3] [4]	V_I < 0, or V_I > V_{IO}+ 0.5	–50	50	mA
I_+	Continuous current through V_+		–100	100	mA
I_{GND}	Continuous current through GND		–100	100	mA
θ_{JA}	Package thermal impedance[6]	YZT pacakge		TBD	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY(1)

V_+ = 2.7 V to 3.6 V, V_{IO} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ (V_{NO} or V_{NC}) ≤ 1.6, I_{COM} = –10 mA,	Switch ON, See Figure 13	25°C	2.7 V		3.5	5	Ω
				Full				6	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.6 V, I_{COM} = –10 mA,	Switch ON, See Figure 13	25°C	2.7 V		0.05	0.1	Ω
				Full				0.2	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ 1.6 V, I_{COM} = –10 mA,	Switch ON, See Figure 13	25°C	2.7 V		2	3	Ω
				Full				4	
NC, NO OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = 3 V, or V_{NO} or V_{NC} = 3 V, V_{COM} = 0.3 V,	Switch OFF, See Figure 14	25°C	3.6 V	–5	0.1	5	nA
				Full		–15		15	
NC, NO ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} or V_{NC} = 0.3 V, V_{COM} = Open, or V_{NO} or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–10	0.2	10	nA
				Full		–30		30	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} or V_{NC} = Open, V_{COM} = 0.3 V, or V_{NO} or V_{NC} = Open, V_{COM} = 3 V,	Switch ON, See Figure 15	25°C	3.6 V	–10	0.2	10	nA
				Full		–30		30	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}	V_{IO} = 1.65 V to 1.95 V		Full		0.65 × V_{IO}		V_{IO}	V
Input logic low	V_{IL}	V_{IO} = 1.65 V to 1.95 V		Full		0		0.35 × V_{IO}	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_{IO} or 0		25°C	3.6 V	–2	0.1	2	nA
				Full		–10		10	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_{IO} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY[1] (continued)

V_+ = 2.7 V to 3.6 V, V_{IO} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V+, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	1	6.5	9	ns
				Full	2.7 to 3.6 V	1		11.5	
Turn-off time	t_{OFF}	V_{COM} = V+, R_L = 50 Ω,	C_L = 35 pF See Figure 17	25°C	3.3 V	1	2	4	ns
				Full	2.7 to 3.6 V	1		5	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = 0.6 V, R_L = 50 Ω,	C_L = 35 pF See Figure 18	25°C	3.3 V	0.5	4	8	ns
				Full	2.7 to 3.6 V	0.5		9	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF See Figure 22	25°C	3.3 V		5.5		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = 1.3 V or GND, Switch OFF,	See Figure 16	25°C	3.3 V		3.5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = 1.3 V or GND, Switch ON,	See Figure 16	25°C	3.3 V		10.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = 1.3 V or GND, Switch ON,	See Figure 16	25°C	3.3 V		10.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND	See Figure 16	25°C	3.3 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON See Figure 19	25°C	2.7 V		800		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 200 MHz,	Switch OFF See Figure 20	25°C	2.7 V		–40		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 200 MHz,	Switch ON See Figure 21	25°C	2.7 V		–39		dB
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V	–20	1	20	nA
				Full		–500		500	
Logic supply current	I_{IO}	V_I = V_{IO} or GND,	Switch ON or OFF	25°C	3.6 V	–10	1	10	nA
				Full		–200		200	

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY(1)

V_+ = 2.3 V to 2.7 V, V_{IO} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					0		V_+	V
ON-state resistance	r_{on}	0 ≤ (V_{NO} or V_{NC}) ≤ 1.3, I_{COM} = –10 mA,	Switch ON, See Figure 13	25°C	2.3 V		4	5.5	Ω
				Full				7	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.3 V, I_{COM} = –10 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.05	0.1	Ω
				Full				0.2	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ 1.3 V, I_{COM} = –10 mA,	Switch ON, See Figure 13	25°C	2.3 V		2.5	4	Ω
				Full				4.5	
NC, NO OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} or V_{NC} = 0.2 V, V_{COM} = 2.3 V, or V_{NO} or V_{NC} = 2.3 V, V_{COM} = 0.2 V,	Switch OFF, See Figure 14	25°C	2.7 V	–5	0.1	5	nA
				Full		–15		15	
NC, NO ON leakage current	$I_{NO(ON)}$, $I_{NC(ON)}$	V_{NO} or V_{NC} = 0.2 V, V_{COM} = Open, or V_{NO} or V_{NC} = 2.3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–5	0.2	5	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} or V_{NC} = Open, V_{COM} = 0.2 V, or V_{NO} or V_{NC} = Open, V_{COM} = 2.3 V,	Switch ON, See Figure 15	25°C	2.7 V	–1	0.05	1	nA
				Full		–10		10	
Digital Control Inputs (IN1, IN2)(2)									
Input logic high	V_{IH}	V_{IO} = 1.65 V to 1.95 V		Full		0.65 × V_{IO}		V_{IO}	V
Input logic low	V_{IL}	V_{IO} = 1.65 V to 1.95 V		Full		0		0.35 × V_{IO}	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_{IO} or 0		25°C	2.7 V	–1	0.05	1	nA
				Full		–10		10	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{IO} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY[(1)] (continued)

V_+ = 2.3 V to 2.7 V, V_{IO} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V+, R_L = 50 Ω,	C_L = 35 pF See Figure 17	25°C	2.5 V	1	7	11	ns
				Full	2.3 to 2.7 V	1		13	
Turn-off time	t_{OFF}	V_{COM} = V+, R_L = 50 Ω,	C_L = 35 pF See Figure 17	25°C	2.5 V	1	2.5	4.5	ns
				Full	2.3 to 2.7 V	1		5.5	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = 0.6 V, R_L = 50 Ω,	C_L = 35 pF See Figure 18	25°C	2.3 V	1	4	8	ns
				Full	2.3 to 2.7 V	1		10	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF See Figure 22	25°C	2.5 V		4		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = 1.6 V or GND, Switch OFF,	See Figure 16	25°C	2.5 V		3.5		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = 1.6 V or GND, Switch ON,	See Figure 16	25°C	2.5 V		10.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = 1.6 V or GND, Switch ON,	See Figure 16	25°C	2.5 V		10.5		pF
Digital input capacitance	C_I	V_I = V_+ or GND	See Figure 16	25°C	2.5 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON See Figure 19	25°C	2.3 V		800		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 200 MHz,	Switch OFF See Figure 20	25°C	2.3 V		–40		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 200 MHz,	Switch ON See Figure 21	25°C	2.3 V		–39		dB
Supply									
Positive supply current	I_+	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V	–10	1	10	nA
				Full		–350		350	
Logic supply current	I_{IO}	V_I = V_{IO} or GND,	Switch ON or OFF	25°C	2.7 V	–5	1	5	nA
				Full		–200		200	

TYPICAL CHARACTERISTICS

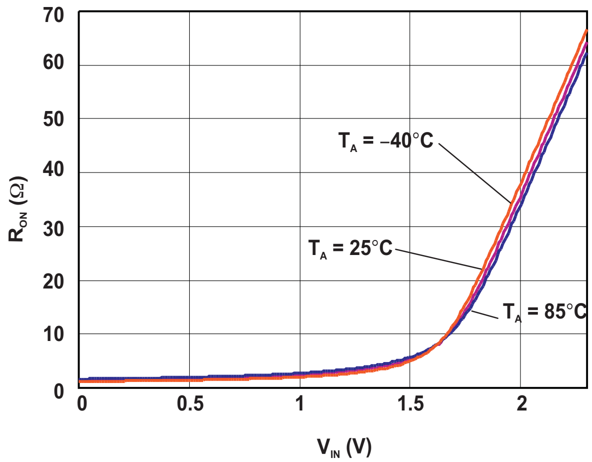


Figure 1. r_{on} vs V_I (NC, NO, or COM), V_+=2.3 V

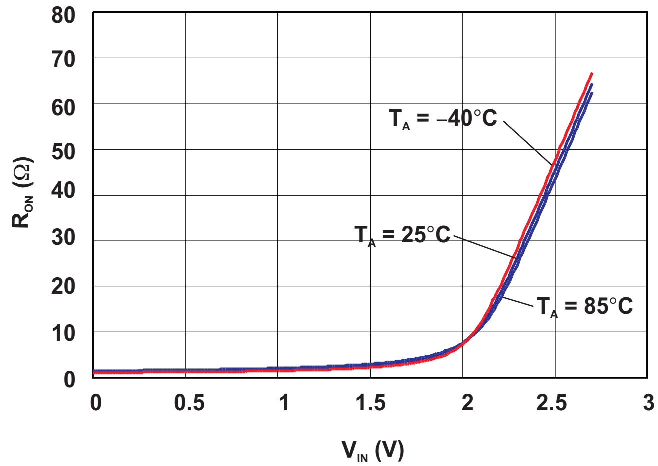


Figure 2. r_{on} vs V_I (NC, NO, or COM), V_+=2.7 V

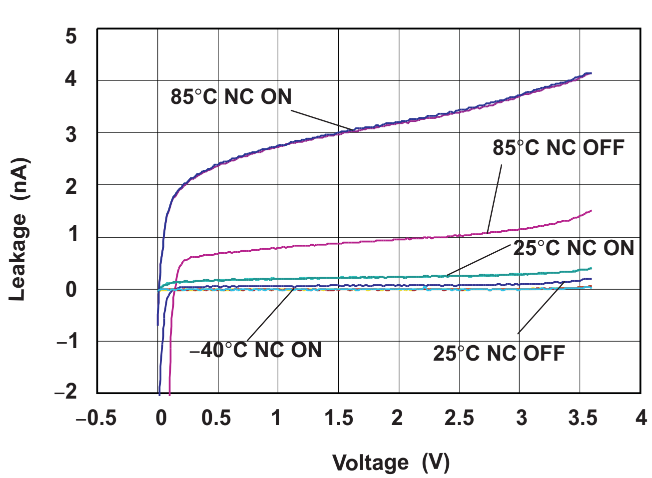


Figure 3. Analog Switch Leakage Current vs V_I (NC, NO, or COM), V_+=3.6 V

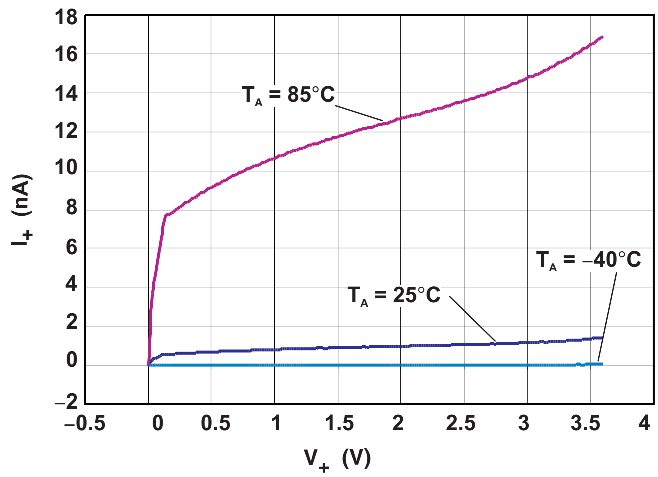


Figure 4. I_+ Supply Current vs V_+

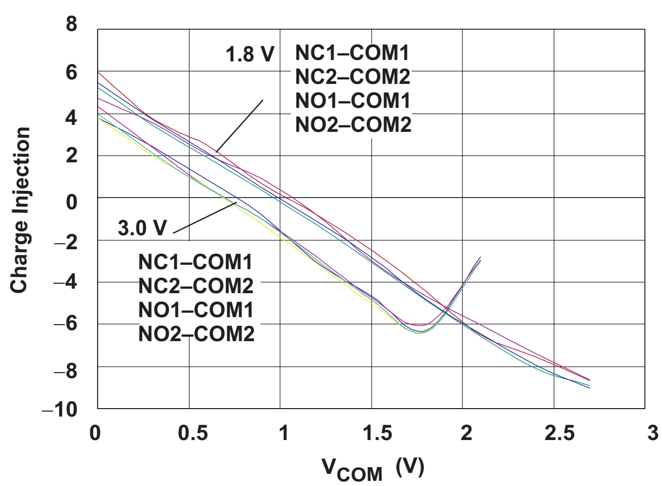


Figure 5. Charge Injection vs V_{COM}

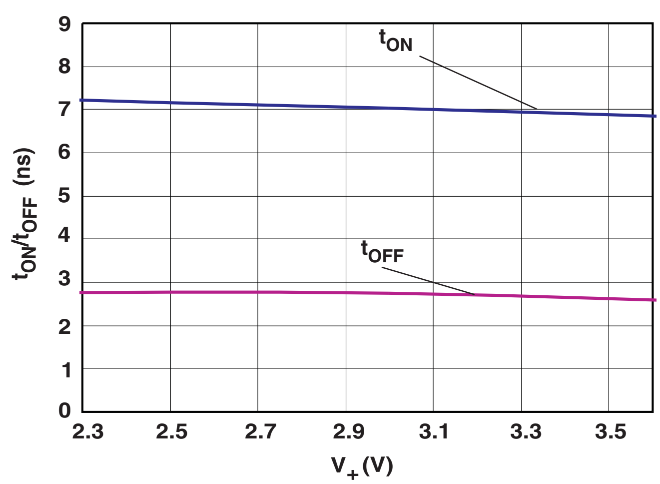


Figure 6. t_{on}/t_{off} vs V_+

TYPICAL CHARACTERISTICS (continued)

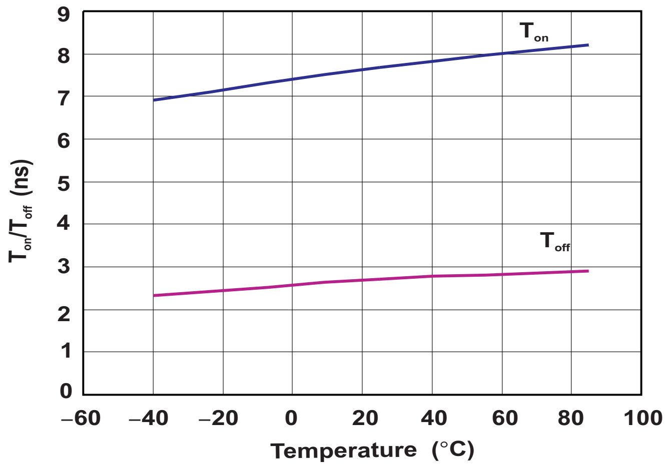


Figure 7. t_{on}/t_{off} vs Temperature, V_+ = 2.3 V

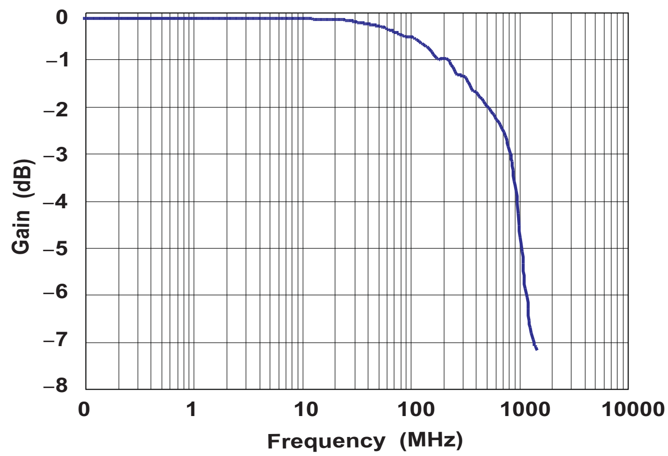


Figure 8. Bandwidth, V_+=2.5 V

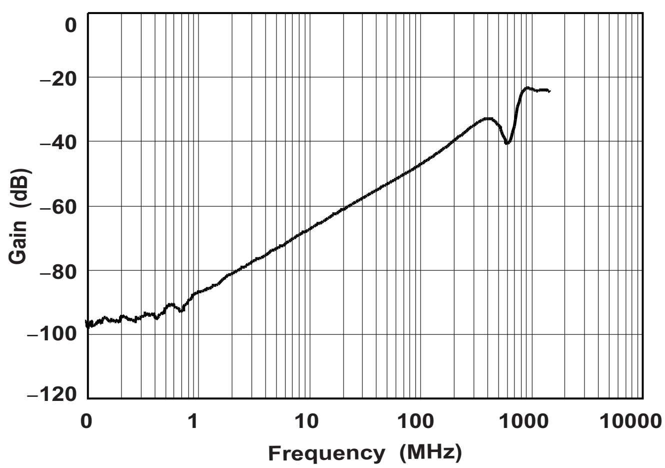


Figure 9. OFF Isolation vs Frequency, V_+=2.5 V

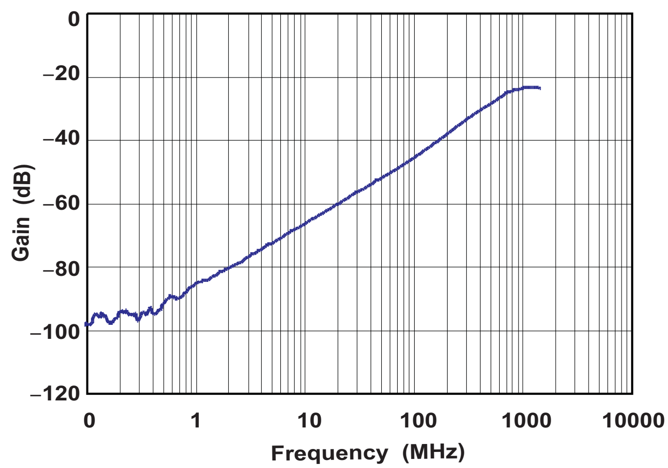


Figure 10. Crosstalk vs Frequency, V_+=2.5 V

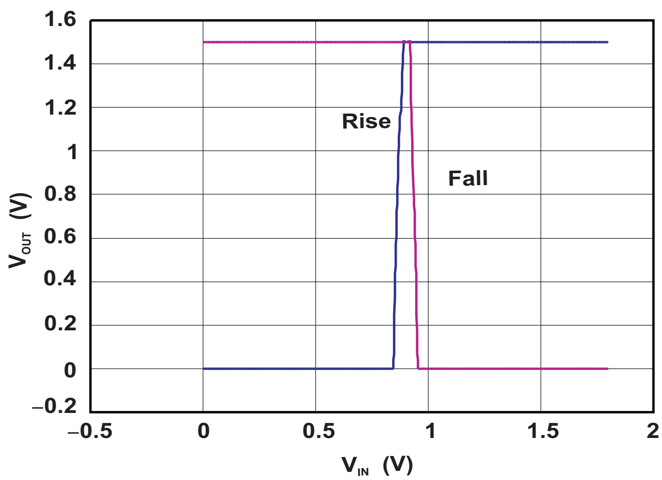


Figure 11. Threshold Voltage, V_{IO}=1.8 V, V_+=2.7 V

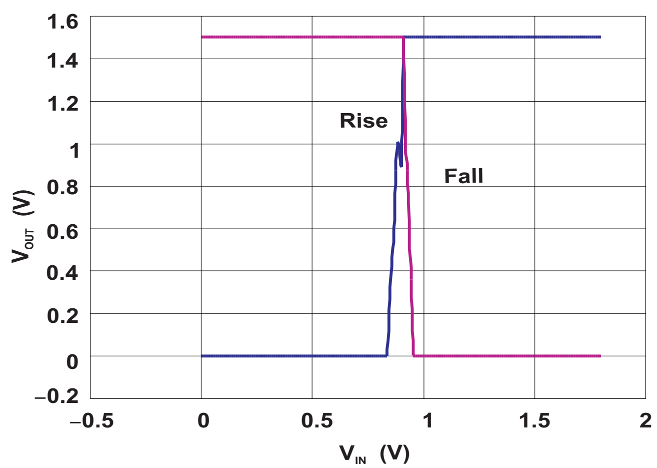


Figure 12. Threshold Voltage, V_{IO}=1.8V, V_+=3.6 V

PARAMETER MEASUREMENT INFORMATION

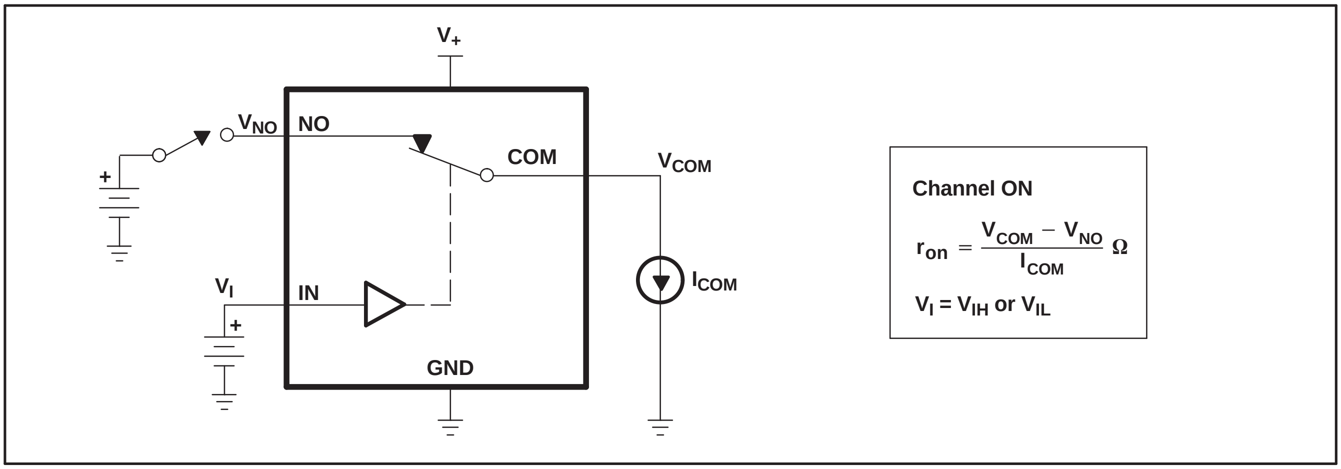


Figure 13. ON-State Resistance (r_{on})

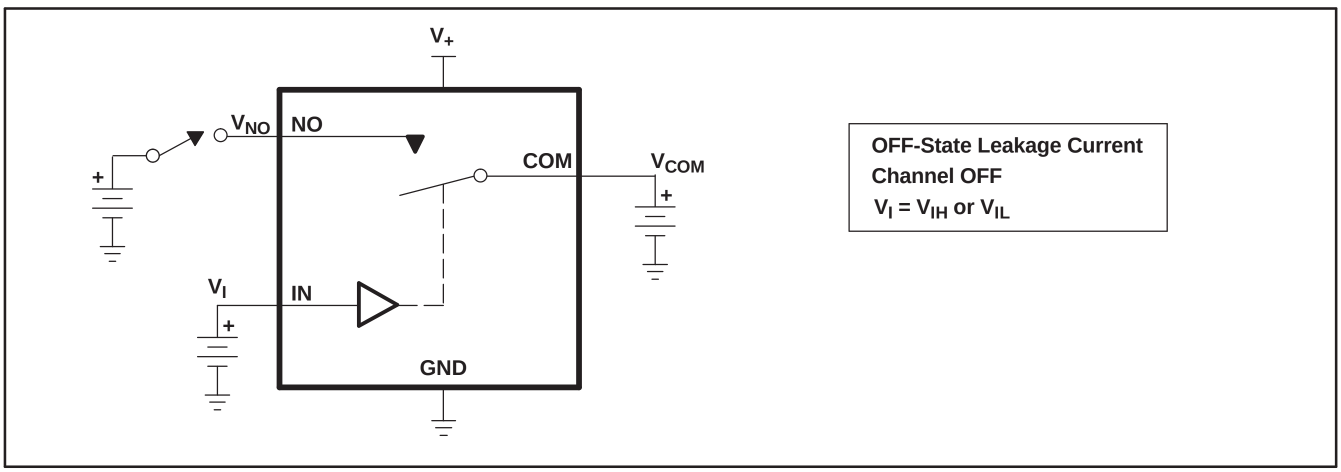


Figure 14. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWROFF)}$)

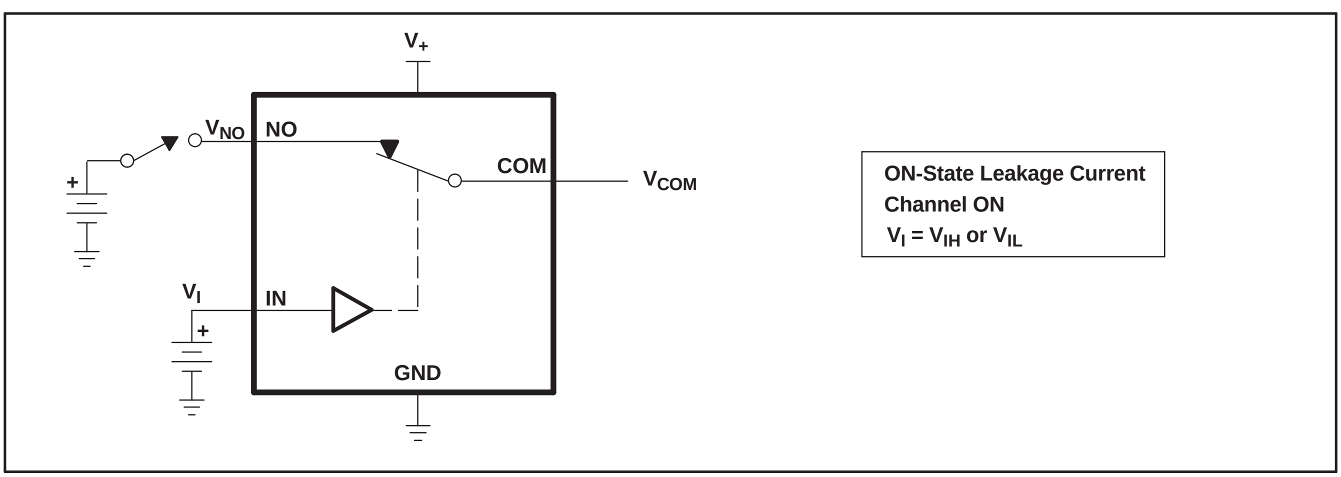


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

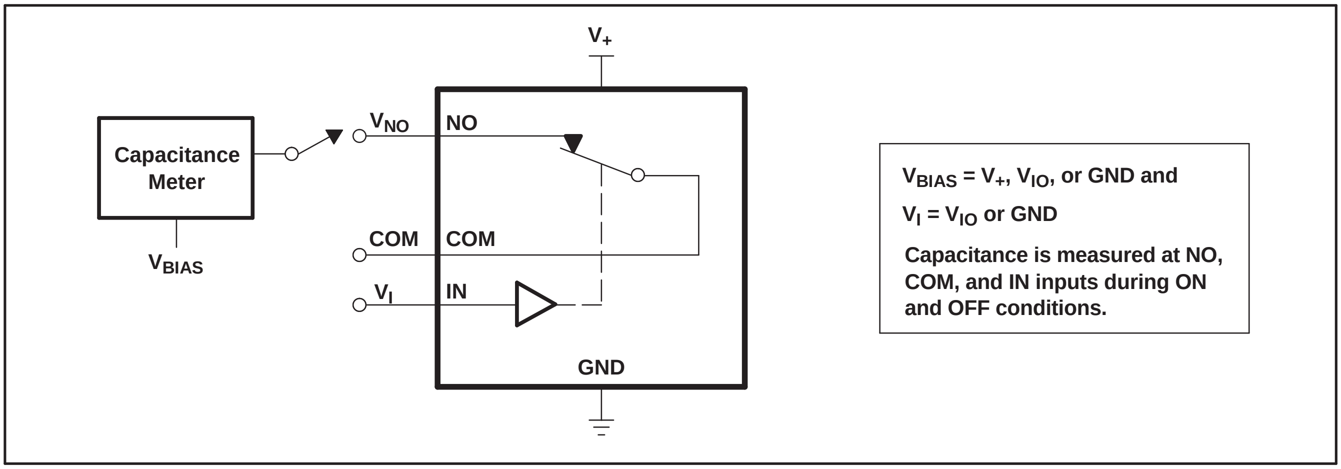
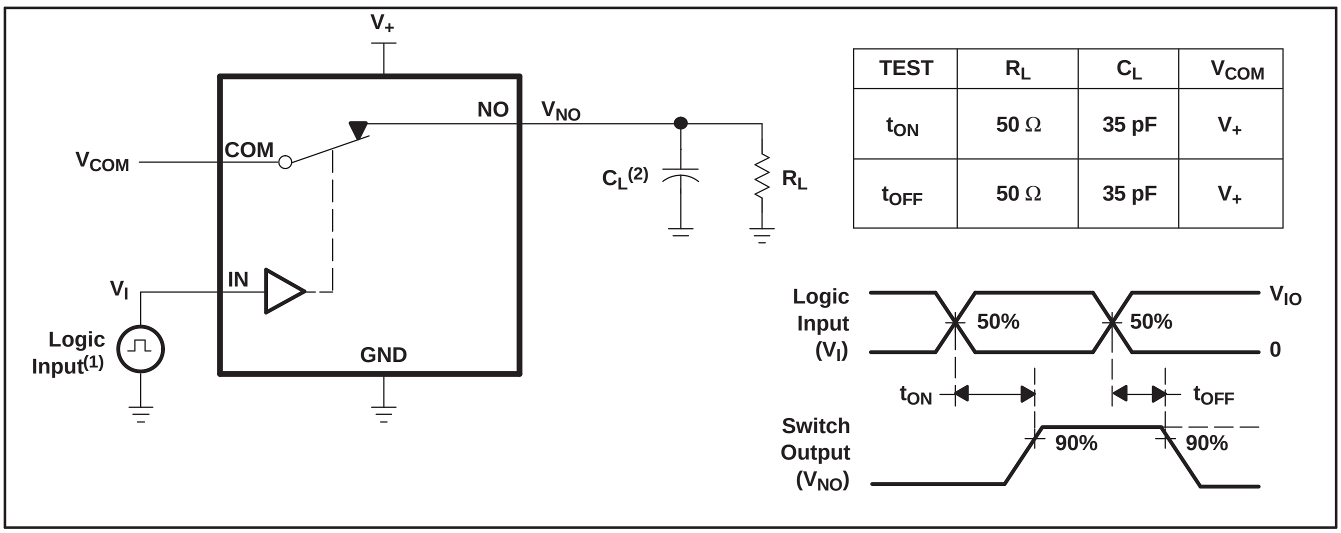


Figure 16. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)

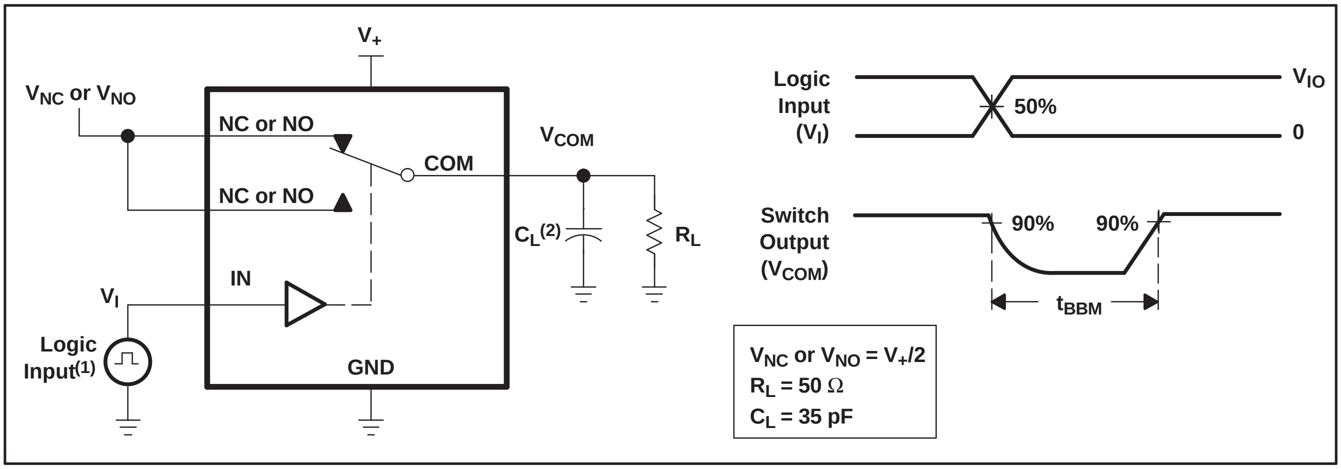


TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)



(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 18. Break-Before-Make Time (t_{BBM})

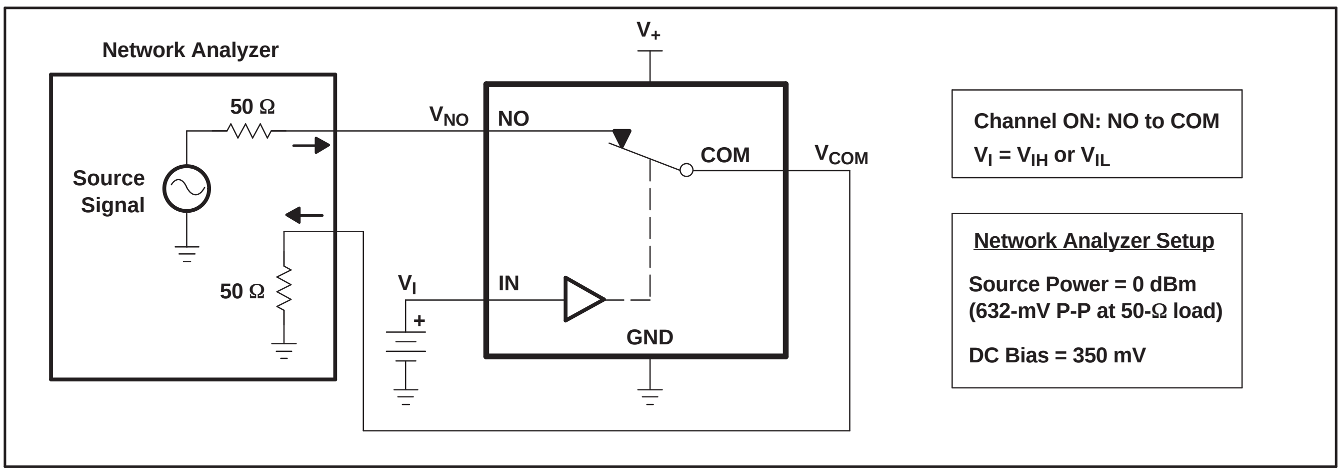


Figure 19. Bandwidth (BW)

PARAMETER MEASUREMENT INFORMATION (continued)

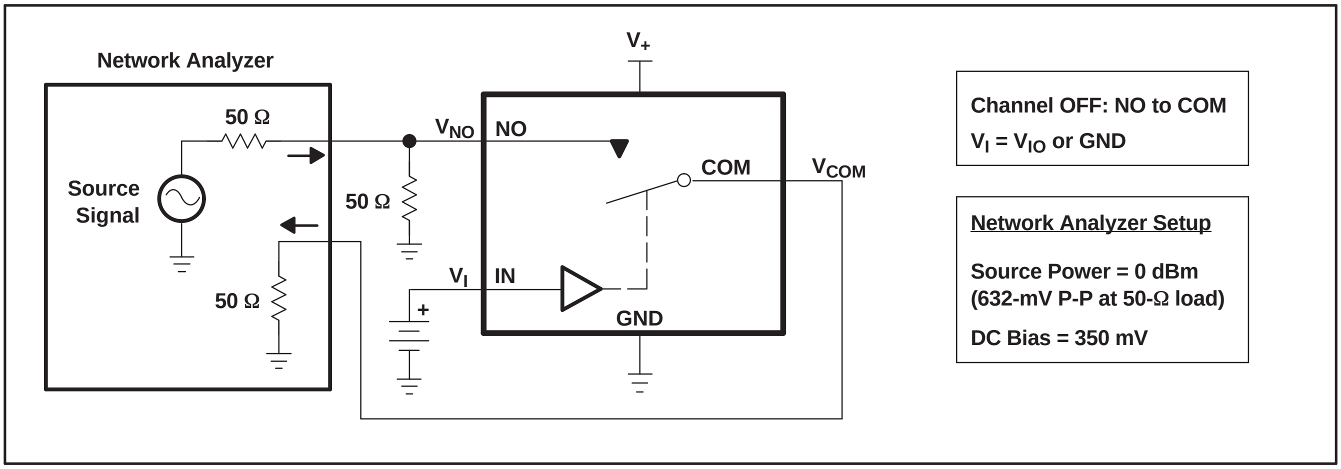


Figure 20. OFF Isolation (O_{ISO})

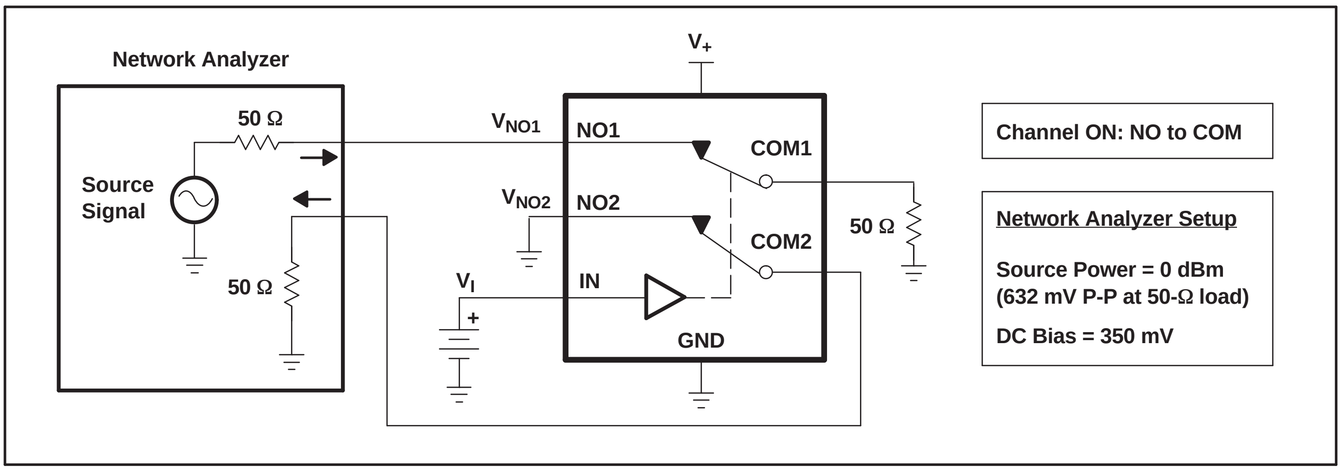
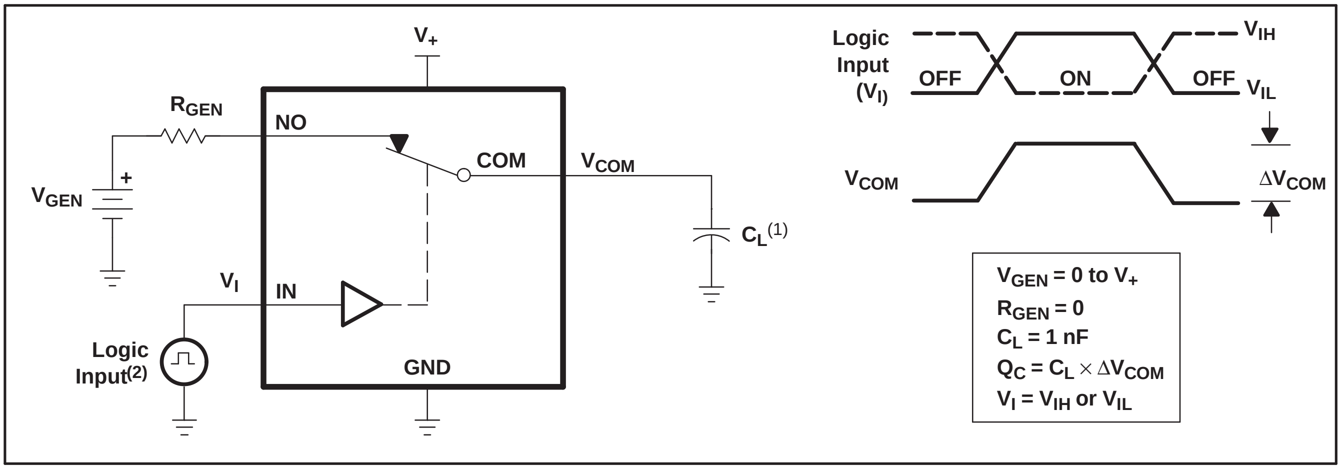


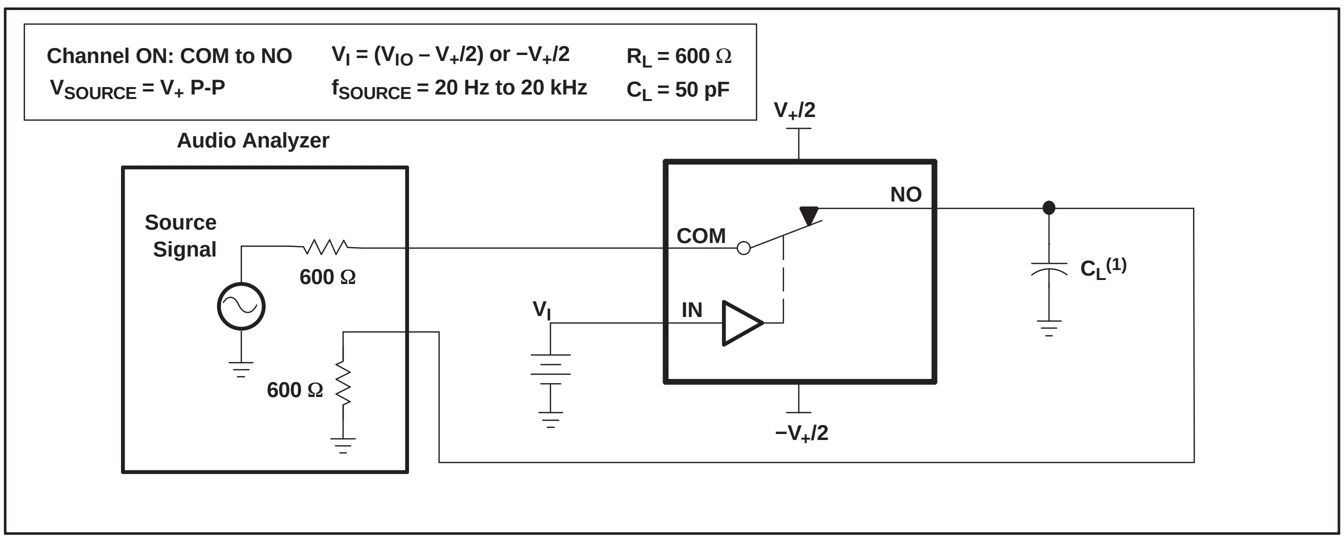
Figure 21. Crosstalk (X_{TALK})

PARAMETER MEASUREMENT INFORMATION (continued)



(1) C_L includes probe and jig capacitance.
(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 22. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 23. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3DS26227YZTR	ACTIVE	DSBGA	YZT	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(262 ~ 267 ~ 26N)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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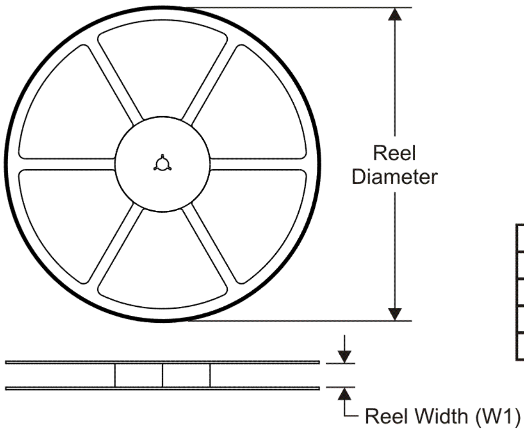
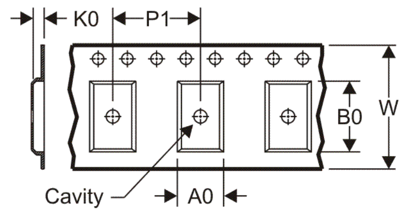
TAPE AND REEL INFORMATION

REEL DIMENSIONS

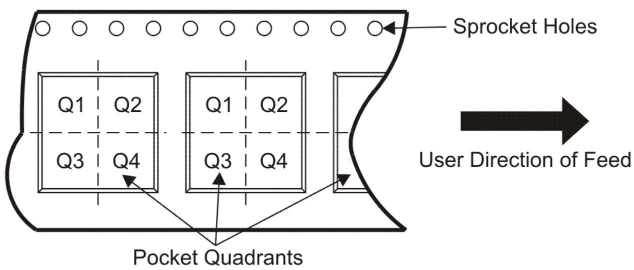


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

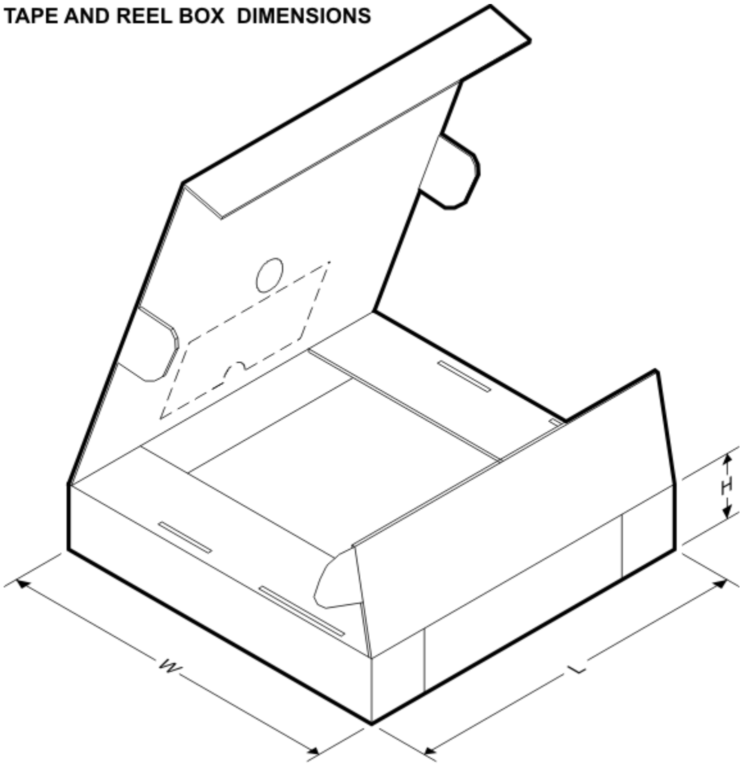
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DS26227YZTR	DSBGA	YZT	12	3000	178.0	9.2	1.49	1.99	0.75	4.0	8.0	Q2

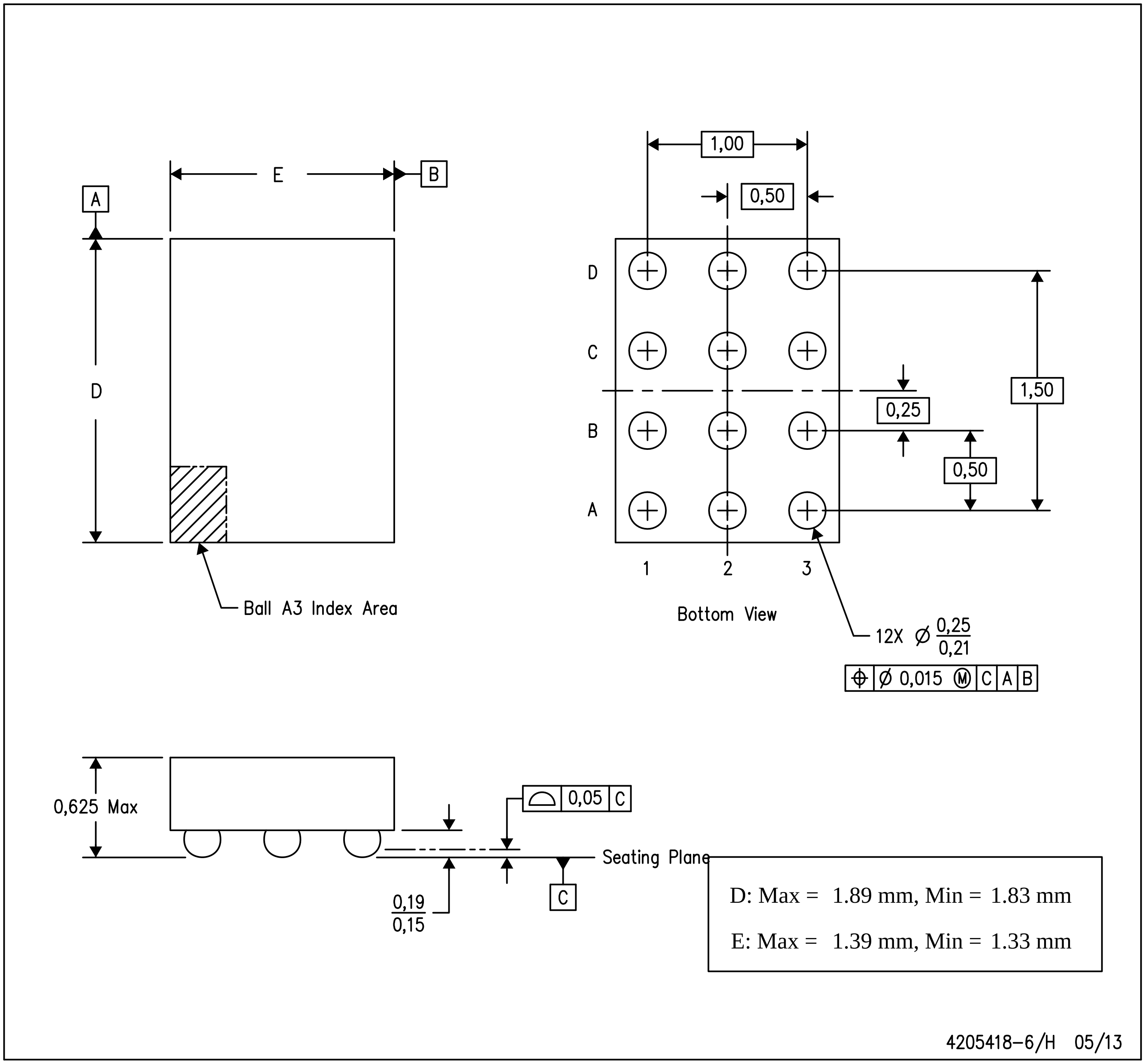
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DS26227YZTR	DSBGA	YZT	12	3000	220.0	220.0	35.0

YZT (R–XBGA–N12) (CUSTOM) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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