HD6802W

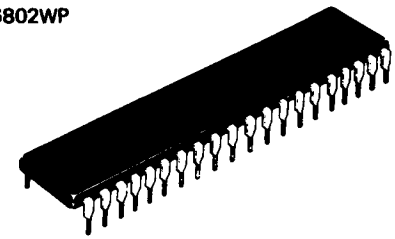
MPU (Microprocessor with Clock and RAM)

HD6802W is the enhanced version of HD6802 which contains MPU, clock and 256 bytes RAM. Internal RAM has been extended from 128 to 256 bytes to increase the capacity of system read/write memory for handling temporary data and manipulating the stack.

The internal RAM is located at hex addresses 0000 to 00FF. The first 32 bytes of RAM, at hex addresses 0000 to 001F, may be retained in a low power mode by utilizing V_{CC} standby, thus facilitating memory retention during a power-down situation.

The HD6802W is completely software compatible with the HD6800 as well as the entire HMCS6800 family of parts. Hence, the HD6802W is expandable to 65k words.

HD6802WP

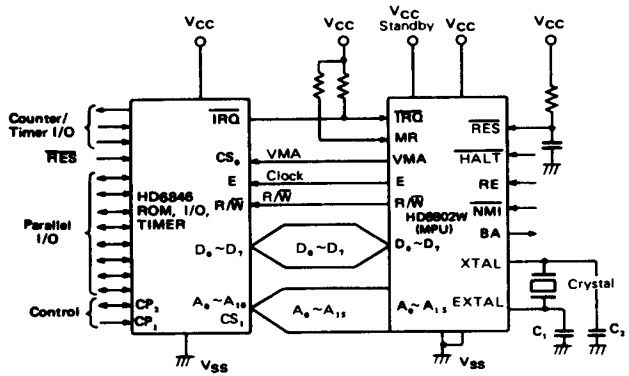


(DP-40)

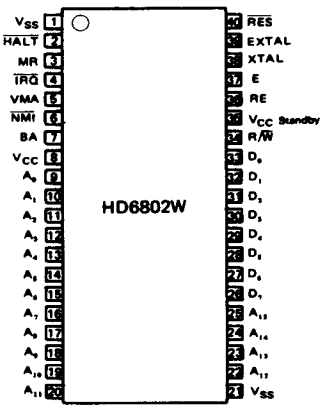
■ FEATURES

- On-Chip Clock Circuit
- 256 × 8 Bit On-Chip RAM
- 32 Bytes of RAM are Retainable
- Software-Compatible with the HD6800, HD6802
- Expandable to 65k words
- Standard TTL-Compatible Inputs and Outputs
- 8 Bit Word Size
- 16 Bit Memory Addressing
- Interrupt Capability

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

2

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A expanded block diagram of the HD6802W is shown in Fig. 1. As shown, the number and configuration of the registers are the same as the HD6802 except that the internal RAM has been extended to 256 bytes.

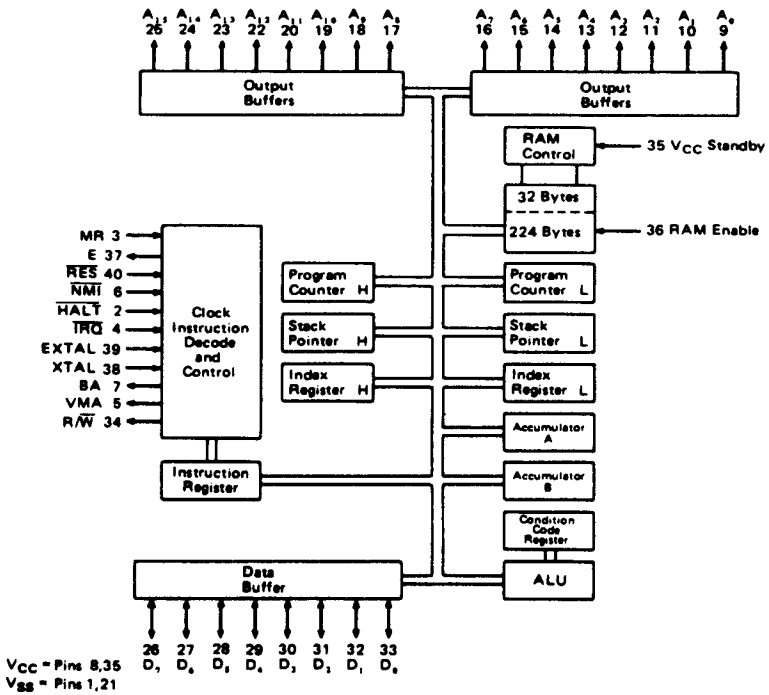

Figure 1 Expanded Block Diagram

Address Map of RAM is shown is Fig. 2.

The HD6802W has 256 bytes of RAM on the chip located at hex addresses 0000 to 00FF. The first 32 bytes of RAM, at hex addresses 0000 to 001F, may be retained in a low power mode by utilizing V_{CC} standby and setting RAM Enable Signal "Low" level, thus facilitating memory retention during a power-down situation.

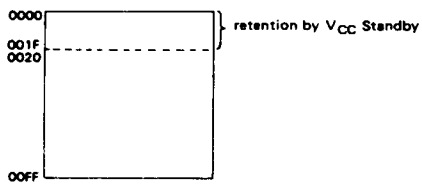

Figure 2 Address Map of HD6802W

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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC} * V_{CC} Standby*	-0.3 ~ +7.0	V
Input Voltage	V_{in}*	-0.3 ~ +7.0	V
Operating Temperature	T_{opr}	-20 ~ +75	°C
Storage Temperature	T_{stg}	-55 ~ +150	°C

* With respect to V_{SS} (SYSTEM GND)

(NOTE) Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol		min	typ	max	Unit
Supply Voltage	V_{CC} *		4.75	5.0	5.25	V
	V_{CC} Standby*		4.0			
Input Voltage	V_{IL}*		-0.3	–	0.8	V
	V_{IH}*	Except $\overline{RES}$	2.0	–	V_{CC}	V
		$\overline{RES}$	V_{CC} -0.75	–	V_{CC}	
Operation Temperature	T_{opr}		-20	25	75	°C

* With respect to V_{SS} (SYSTEM GND)

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{CC}=5.0V±5%, V_{CC} Standby=5.0V±5%, V_{SS}=0V, Ta=-20~+75°C, unless otherwise noted.)

Item		Symbol	Test Condition	min	typ*	max	Unit
Input "High" Voltage	Except $\overline{RES}$	V_{IH}		2.0	–	V_{CC}	V
	$\overline{RES}$			V_{CC}-0.75	–	V_{CC}	
Input "Low" Voltage	Except $\overline{RES}$	V_{IL}**		-0.3	–	0.8	V
	$\overline{RES}$			-0.3	–	0.8	
Output "High" Voltage	D_0~D_7, E	V_{OH}	I_{OH} = -205μA	2.4	–	–	V
	A_0~A_{15}, R/$\overline{W}$, VMA		I_{OH} = -145μA	2.4	–	–	
	BA		I_{OH} = -100μA	2.4	–	–	
Output "Low" Voltage		V_{OL}	I_{OL} = 1.6mA	–	–	0.4	V
Three State (Off State) Input Current	D_0~D_7	I_{TSI}	V_{in} = 0.4~2.4V	-10	–	10	μA
Input Leakage Current	Except D_0~D_7	I_{in} ***	V_{in} = 0~5.25V	-2.5	–	2.5	μA
Power Dissipation		P_D ****		–	0.7	1.2	W
Input Capacitance	D_0~D_7	C_{in}	V_{in}=0V, T_a=25°C, f=1.0MHz	–	10	12.5	pF
	Except D_0~D_7			–	6.5	10	
Output Capacitance	A_0~A_{15}, R/$\overline{W}$, BA, VMA	C_{out}	V_{in}=0V, T_a=25°C, f=1.0MHz	–	–	12	pF

* T_a=25°C, V_{CC}=5V
** As $\overline{RES}$ input has histeresis character, applied voltage up to 2.4V is regarded as "Low" level when it goes up from 0V.
*** Does not include EXTAL and XTAL, which are crystal inputs.
**** In power-down mode, maximum power dissipation is less than 42mW.

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● **AC CHARACTERISTICS (V_{CC}=5.0V±5%, V_{CC} Standby=5.0V±5%, V_{SS}=0V, Ta=-20~+75°C, unless otherwise noted.)**

1. CLOCK TIMING CHARACTERISTICS

Item		Symbol	Test Condition	min	typ	max	Unit
Frequency of Operation	Input Clock ÷ 4	f		0.1	–	1.0	MHz
	Crystal Frequency	f_{XTAL}		1.0	–	4.0	
Cycle Time		t_{cyc}	Fig. 4, Fig. 5	1.0	–	10	μs
Clock Pulse Width	"High" Level	$PW_{\phi H}$	at 2.4V (Fig. 4, Fig. 5)	450	–	4500	ns
	"Low" Level	$PW_{\phi L}$	at 0.4V (Fig. 4, Fig. 5)				
Clock Fall Time		t_{ϕ}	0.4V ~ 2.4V (Fig.4,Fig.5)	–	–	25	ns

2. READ/WRITE TIMING

Item	Symbol	Test Condition	min	typ*	max	Unit
Address Delay	t_{AD}	Fig. 4, Fig. 5, Fig. 8	–	–	270	ns
Peripheral Read Access Time	t_{acc}	Fig. 4	530	–	–	ns
Data Setup Time (Read)	t_{DSR}	Fig. 4	100	–	–	ns
Input Data Hold Time	t_{H}	Fig. 4	10	–	–	ns
Output Data Hold Time	t_{H}	Fig. 5	20	–	–	ns
Address Hold Time (Address, R/$\overline{W}$, VMA)	t_{AH}	Fig. 4, Fig. 5	10	–	–	ns
Data Delay Time (Write)	t_{DDW}	Fig. 5	–	–	225	ns
Bus Available Delay	t_{BA}	Fig. 6, Fig. 7, Fig. 9, Fig. 10	–	–	250	ns
Processor Controls Processor Control Setup Time	t_{PCS}	Fig. 6 ~ Fig. 9, Fig. 11	200	–	–	ns
Processor Control Rise and Fall Time (Measured at 0.8V and 2.0V)	t_{PCr}, t_{PCf}	Fig. 6 ~ Fig. 9, Fig. 11, Fig. 12, Fig. 14	–	–	100	ns

* Ta = 25°C, V_{CC} = 5V

3. POWER DOWN SEQUENCE TIMING, POWER UP RESET TIMING AND MEMORY READY TIMING

Item	Symbol	Test Condition	min	typ	max	Unit
RAM Enable Reset Time (1)	t_{RE1}	Fig. 12	150	–	–	ns
RAM Enable Reset Time (2)	t_{RE2}	Fig. 12	E-3 cycles	–	–	
Reset Release Time	t_{LRES}	Fig. 11	20	–	–	ms
RAM Enable Reset Time (3)	t_{RE3}	Fig. 11	0	–	–	ns
Memory Ready Setup Time	t_{SMR}	Fig. 14	300	–	–	ns
Memory Ready Hold Time	t_{HMR}	Fig. 14	0	–	200	ns

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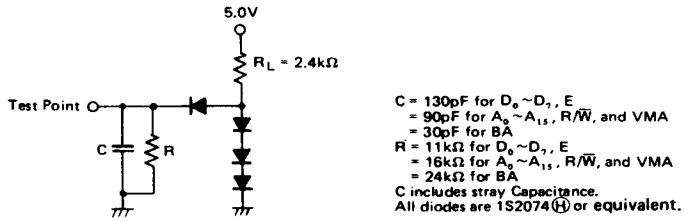

Figure 3 Bus Timing Test Load

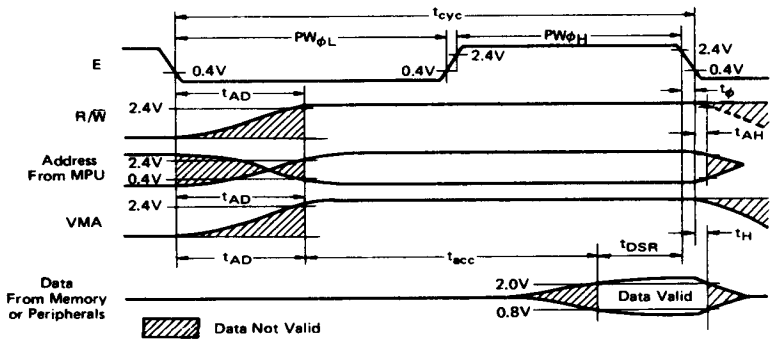

Figure 4 Read Data from Memory or Peripherals

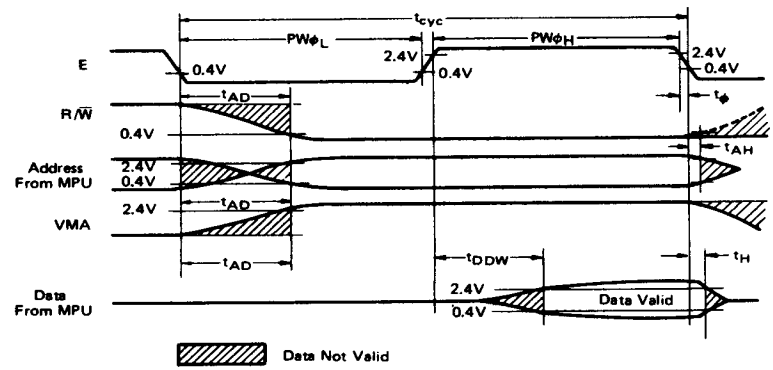

Figure 5 Write Data in Memory or Peripherals

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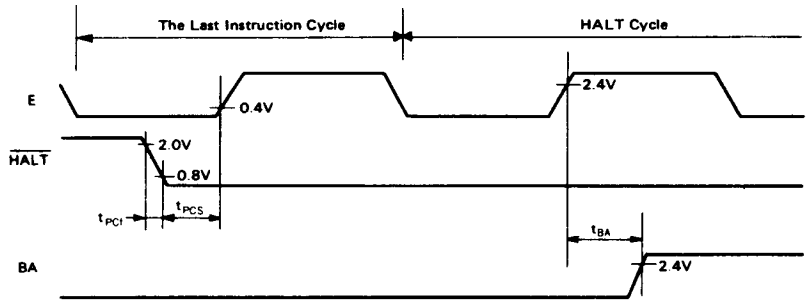

Figure 6 Timing of $\overline{\text{HALT}}$ and BA

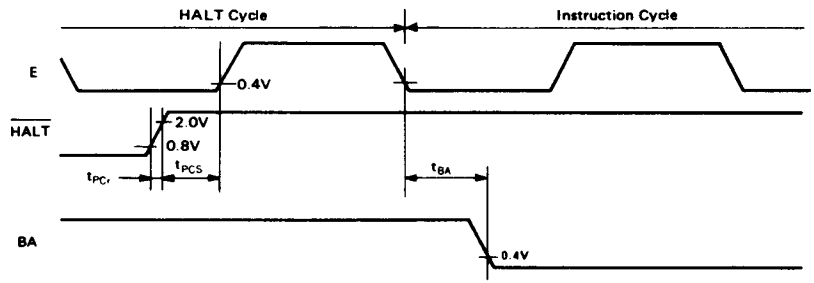

Figure 7 Timing of $\overline{\text{HALT}}$ and BA

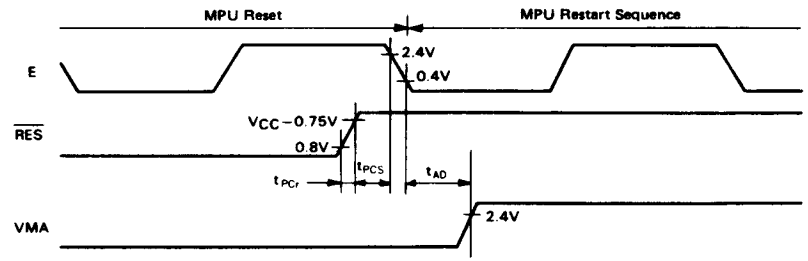

Figure 8 $\overline{\text{RES}}$ and MPU Restart Sequence

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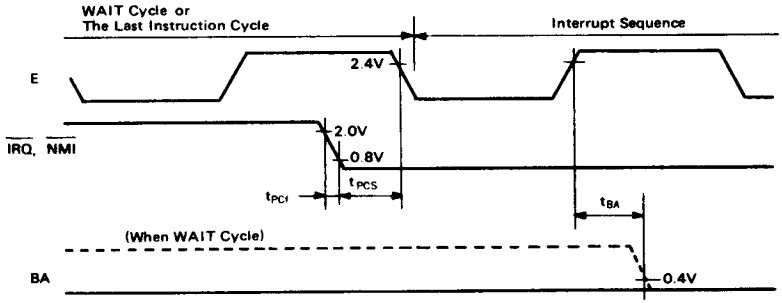

Figure 9 $\overline{IRQ}$ and $\overline{NMI}$ Interrupt Timing

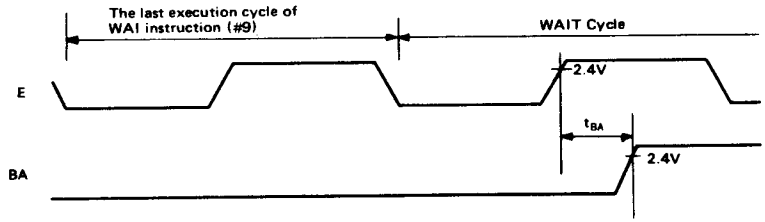

Figure 10 WAI Instruction and BA Timing

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■ HD6802W MPU SIGNAL DESCRIPTION

- **Address Bus ($A_0 \sim A_{15}$)**

Sixteen pins are used for the address bus. The outputs are capable of driving one standard TTL load and 90pF.

- **Data Bus ($D_0 \sim D_7$)**

Eight pins are used for the data bus. It is bidirectional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load and 130pF.

Data Bus will be in the output mode when the internal RAM is accessed. This prohibits external data entering the MPU. It should be noted that the internal RAM is fully decoded from $0000 to $00FF. External RAM at $0000 to $00FF must be disabled when internal RAM is accessed.

- **$\overline{\text{HALT}}$**

When this input is in the "Low" state, all activity in the machine will be halted: This input is level sensitive.

In the halt mode, the machine will stop at the end of an instruction. Bus Available will be at a "High" state. Valid Memory Address will be at a "Low" state. The address bus will display the address of the next instruction.

To insure single instruction operation, transition of the $\overline{\text{HALT}}$ line must not occur during the last t_{PCS} of E and the $\overline{\text{HALT}}$ line must go "High" for one Clock cycle.

$\overline{\text{HALT}}$ should be tied "High" if not used. This is good engineering design practice in general and necessary to insure proper operation of the part.

- **Read/Write (R/$\overline{\text{W}}$)**

This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read ("High") or Write ("Low") state. The normal standby state of this signal is Read ("High"). When the processor is halted, it will be in the logical one state ("High").

This output is capable of driving one standard TTL load and 90pF.

- **Valid Memory Address (VMA)**

This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 90pF may be directly driven by this active high signal.

- **Bus Available (BA)**

The Bus Available signal will normally be in the "Low" state. When activated, it will go to the "High" state indicating that the microprocessor has stopped and that the address bus is available (but not in a three-state condition). This will occur if the $\overline{\text{HALT}}$ line is in the "Low" state or the processor is in the wait state as a result of the execution of a WAI instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level.

The processor is removed from the wait state by the occurrence of a maskable (mask bit I=0) or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30pF.

- **Interrupt Request ($\overline{\text{IRQ}}$)**

This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait, until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The $\overline{\text{HALT}}$ line must be in the "High" state for interrupts to be serviced. Interrupts will be latched internally while $\overline{\text{HALT}}$ is "Low".

A 3kΩ external register to V_{CC} should be used for wire-OR and optimum control of interrupts.

- **Reset ($\overline{\text{RES}}$)**

This input is used to reset and start the MPU from a power-down condition, resulting from a power failure or an initial start-up of the processor. When this line is "Low", the MPU is inactive and the information in the registers will be lost. If a "High" level is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced "High". For the restart, the last two(FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$. Power-up and reset timing and power-down sequences are shown in Fig. 11 and Fig. 12 respectively.

- **Non-Maskable Interrupt ($\overline{\text{NMI}}$)**

A low-going edge on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the $\overline{\text{IRQ}}$ signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory. A 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are sampled when E is "High" and will start the interrupt routine on a "Low" E following the completion of an instruction. $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ should be tied "High" if not used. This is good engineering design practice in general and necessary to insure proper operation of the part. Fig. 13 is a flowchart describing the major decision paths and interrupt vectors of the microprocessor. Table 1 gives the memory map for interrupt vectors.

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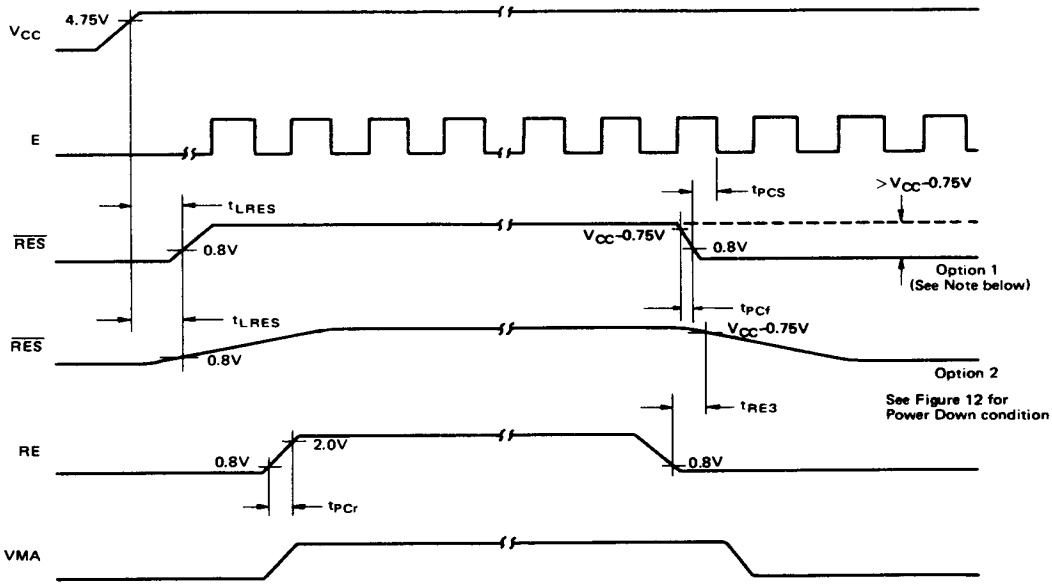

(NOTE) If option 1 is chosen, $\overline{RES}$ and RE pins can be tied together.

Figure 11 Power-up and Reset Timing

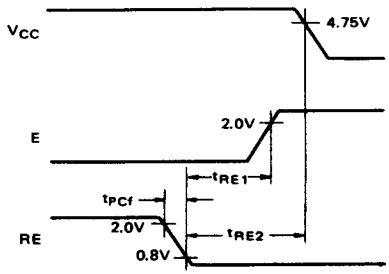

Figure 12 Power-down Sequence

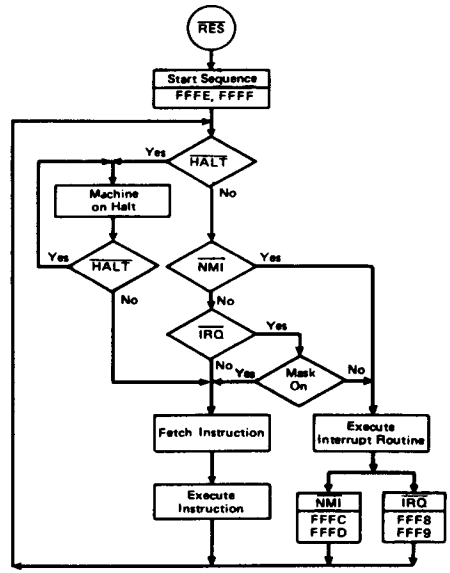

Figure 13 MPU Flow Chart

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Table 1 Memory Map for Interrupt Vectors

Vector MS	Vector LS	Description	
FFFE	FFFF	Restart	($\overline{RES}$)
FFFC	FFFD	Non-Maskable Interrupt	($\overline{NMI}$)
FFFA	FFFB	Software Interrupt	(SWI)
FFF8	FFF9	Interrupt Request	($\overline{IRQ}$)

- **RAM Enable (RE)**

A TTL-compatible RAM enable input controls the on-chip RAM of the HD6802W. When placed in the "High" state, the on-chip memory is enabled to respond to the MPU controls. In the "Low" state, RAM is disabled. This pin may also be utilized to disable reading and writing the on-chip RAM during a power-down situation. RAM enable must be "Low" three cycles before V_{CC} goes below 4.75V during power-down.

RE should be tied to the correct "High" or "Low" state if not used. This is good engineering design practice in general and necessary to insure proper operation of the part.

- **EXTAL and XTAL**

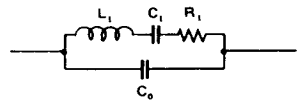
The HD6802W has an internal oscillator that may be crystal controlled. These connections are for a parallel resonant fundamental crystal (AT cut). A divide-by-four circuit has been added to the HD6802W so that a 4MHz crystal may be used in lieu of a 1MHz crystal for a more cost-effective system. Pin39 of the HD6802W may be driven externally by a TTL input signal if a separate clock is required. Pin38 is to be left open in this mode.

An RC network is not directly usable as a frequency source on pins 38 and 39. An RC network type TTL or CMOS oscillator will work well as long as the TTL or CMOS output drives the HD6802W.

If an external clock is used, it may not be halted for more than 4.5μs. The HD6802W is a dynamic part except for the internal RAM, and requires the external clock to retain information.

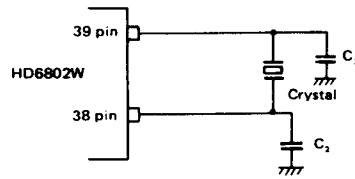
Conditions for Crystal (4 MHz)

- AT Cut Parallel resonant
- C_0 = 7 pF max.
- R_1 = 80Ω max.



Crystal Equivalent Circuit

Recommended Oscillator (4MHz)



$C_1 = C_2 = 22pF \pm 20\%$

When using the crystal, see the note for Board Design of the Oscillation Circuit in HD6802W.

- **Memory Ready (MR)**

MR is a TTL compatible input control signal which allows stretching of E. When MR is "High", E will be in normal operation. When MR is "Low", E may be stretched integral multiples of half periods, thus allowing interface to slow memories. Memory Ready timing is shown in Fig. 14.

MR should be tied "High" if not used. This is good engineering design practice in general and necessary to insure proper operation of the part. A maximum stretch is 4.5μs.

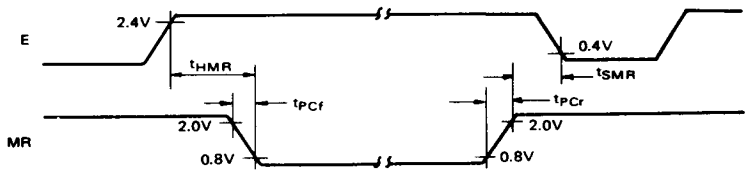


Figure 14 Memory Ready Control Function

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- **Enable (E)**

This pin supplies the clock for the MPU and the rest of the system. This is a single phase, TTL compatible clock. This clock may be conditioned by a Memory Ready Signal. This is equivalent to ϕ_2 on the HD6800.

- **V_{CC} Standby**

This pin supplies the dc voltage to the first 32 bytes of RAM as well as the RAM Enable (RE) control logic. Thus retention of data in this portion of the RAM on a power-up, power-down, or standby condition is guaranteed at the range of 4.0 V to 5.25 V. Maximum current drain at 5.25V is 8mA.

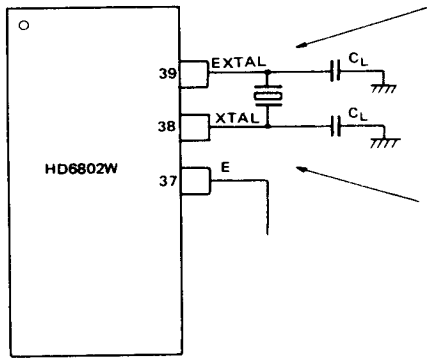
■ MPU INSTRUCTION SET

The HD6802W has a set of 72 different instructions. Included are binary and decimal arithmetic, logical, shift, rotate, load, store, conditional or unconditional branch, interrupt and stack manipulation instructions.

This instruction set is the same as that for the 6800MPU (HD6800 etc.) and is not explained again in this data sheet.

■ NOTE FOR BOARD DESIGN OF THE OSCILLATION CIRCUIT IN HD6802W

In designing the board, the following notes should be taken when the crystal oscillator is used.

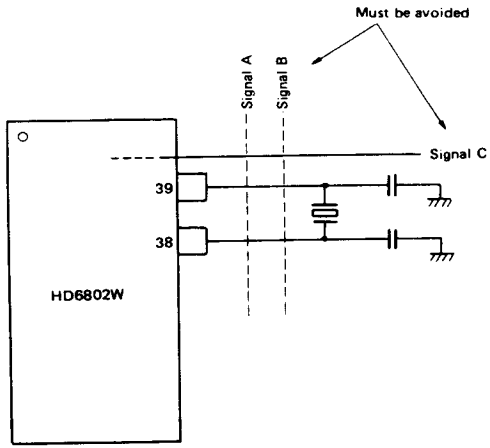


Crystal oscillator and load capacity C_L must be placed near the LSI as much as possible.

Normal oscillation may be disturbed when external noise is induced to pin 38 and 39.

Pin 38 signal line should be wired apart from pin 37 signal line as much as possible. Don't wire them in parallel, or normal oscillation may be disturbed when E signal is feedbacked to XTAL.

The following design must be avoided.



A signal line or a power source line must not cross or go near the oscillation circuit line as shown in the left figure to prevent the induction from these lines and perform the correct oscillation. The resistance among XTAL, EXTAL and other pins should be over 10MΩ.

Figure 15 Note for Board Design of the Oscillation Circuit

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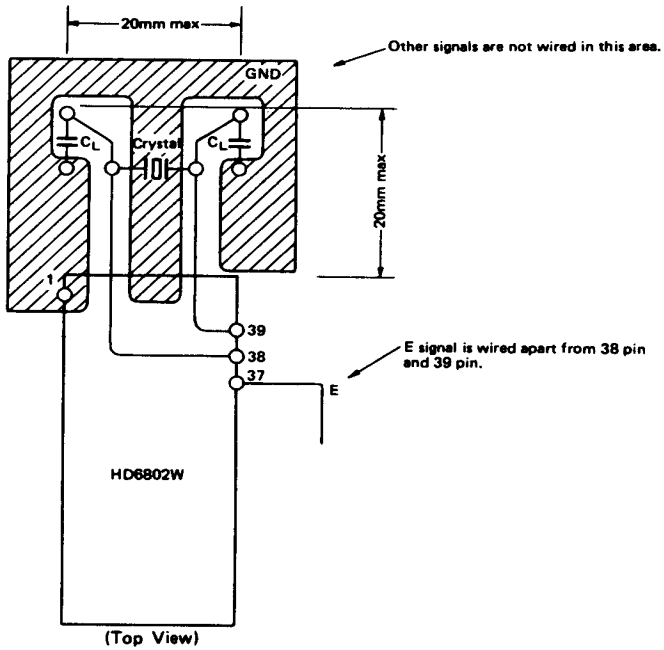

Figure 16 Example of Board Design Using the Crystal Oscillator

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■ NOTE FOR THE RELATION BETWEEN WAI INSTRUCTION AND HALT OPERATION OF HD6802W

When $\overline{HALT}$ input signal is asserted to "Low" level, the MPU will be halted after the execution of the current instruction except WAI instruction.

The "Halt" signal is not accepted after the fetch cycle of the WAI instruction (See ① in Fig. 17). In the case of the "WAI" instruction, the MPU enters the "WAIT" cycle after stacking the internal registers and outputs the "High" level on the BA line.

When an interrupt request signal is input to the MPU, the MPU accepts the interrupt regardless the "Halt" signal and releases the "WAIT" state and outputs the interrupt's vector address. If the "Halt" signal is "Low" level, the MPU halts after the fetch of new PC contents. The sequense is shown below.

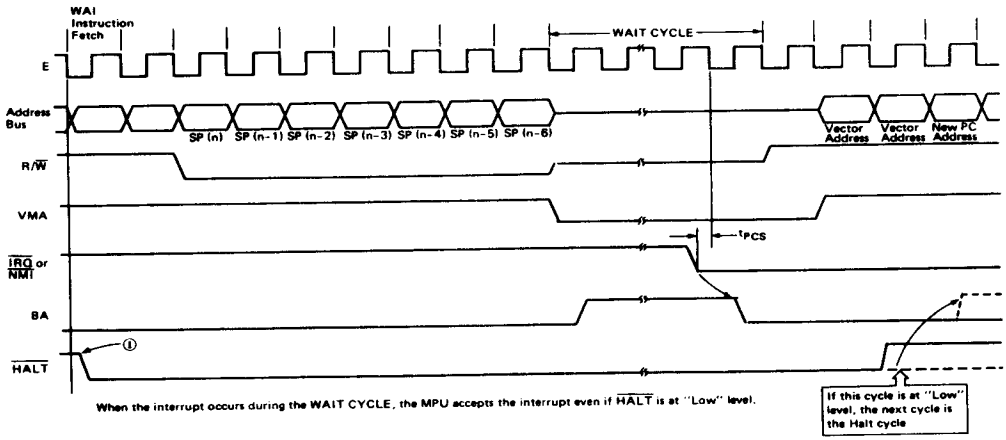

Figure 17 HD6802W WAIT CYCLE & $\overline{HALT}$ Request

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