Preliminary Data Sheet, DS1, July 2000

MuSLIC

Multichannel Subscriber Line Interface Concept

PEB 3465 Version 1.2

PEB 31666/31664 Version 1.3

PEB 4166/4164 Version 2.3

Wired Communications

Infineon technologies

Never stop thinking.

Edition 2000.07.06

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

MuSLIC

Multichannel Subscriber Line Interface Concept

PEB 3465 Version 1.2

PEB 31666/31664 Version 1.3

PEB 4166/4164 Version 2.3

Wired Communications

Infineon technologies

Never stop thinking.

MuSLIC
PRELIMINARY
Revision History: **2000.07.06** DS1

Previous Version: Preliminary Data Sheet DS1

Page	Subjects (major changes since last revision)
Page 50	Version register added to **Table 6**.
Page 51	Status Register: Bit SAMPLE_RDY added.
Page 52	**Figure 22** “Reading of Sample Results” added.
Page 49	Interrupt (INTR) signal active level for Intel mode and Motorola mode added.
Page 54	**Table 7** “Interrupt Register”: “idle” added. Further description added.
Page 56	Former chapter 3.2.3 “Interrupt Timing” including former figure “Interrupt Timing” removed.
Page 57	**Figure 25** “Interrupt Handling (First Step)” added.
Page 58	**Figure 26** “Interrupt Handling (Second Step - Interrups in one Channel)” added.
Page 59	**Figure 27** “Interrupt Handling (Second Step - Interrupts in two or more Channels)” added.
Page 75	Configuration Register SCR3: Bits MODEM, USGAIN and ZSWITCH added.
Page 84	Bits Mo, M1, M2: Note on pin IO1 of the QAP added.
Page 104	Extended Operation Test Register XTR6: Bit GAINBB added, description for bit DITOFF changed, **Table 10** "Important factors by using MuSLICOS" added.
Page 122	**Table 11** Operating Modes MuSLIC-E added
Page 131	Unbalanced Ringing: Description on improved support of external ringing delay added.

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com/products

Table of Contents **Page**

Table of Contents **Page**

List of Figures

List of Figures **Page**

List of Tables

1 Introduction

The MuSLIC, a chip set of three highly sophisticated ICs, bridges the gap between the analog and the digital signal transmission in modern telecommunication systems.

This highly integrated chip set supports to realize an extremely compact Analog Subscriber Line Interface module. Only a few external components are required and there is no trimming or adjustment necessary to meet worldwide recommendations.

Each device is made of the best fitting technology (CMOS, BiCMOS and Smart Power technology) and the standard SMD-packages P-MQFP and P-DSO are used.

The chip set consists of three out of seven available ICs:

Table 1 MuSLIC Chip Set ICs

PEB 31664 PEB 31665 PEB 31666	MuPP µC-S MuPP IOM®-2 MuPP µC-E	Multichannel Processor for POTS
PEB 3465	QAP	Quad Analog POTS
PEB 4164 PEB 4165 PEB 4166	AHV-SLIC-S AHV-SLIC AHV-SLIC-E	Advanced High Voltage Subscriber Line Circuit

Note: The term "MuPP-µC" in this document applies to both chips MuPP µC-E (PEB 31666) and MuPP µC-S (PEB 31664). The term AHV-SLIC applies to both chips AHV-SLIC-E (PEB 4166) and AHV-SLIC-S (PEB 4164).

This document describes the combination of MuPP µC, QAP and AHV-SLIC in detail.

The combination of MuPP IOM-2, QAP and AHV-SLIC (PEB 4165) is described within a second document. Nevertheless, other possible combinations of MuPP and AHV-SLIC devices can also be implemented.

Note: For more detailed description please refer to the MuSLIC chip set Selection Guide and the Application Note "Differences between MuSLIC-E and MuSLIC-S".

PRELIMINARY

Multichannel Subscriber Line Interface Concept MuSLIC

PEB 3465
PEB 4166/4
PEB 31666/4

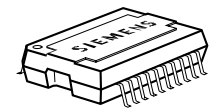
BiCMOS, CMOS, Smart Power

1.1 Features

- Chip set of three well fitted chips optimized for a 16 POTS-base system
- Including all low and high voltage SLIC functions
- Only a few external components are required
- No trimming or adjustments are required
- Specification according to relevant ITU-T Q.552 Z interface, LSSGR and DTAG recommendations
- Digital signal processing technique
- Advanced low power CMOS and BiCMOS[1)] and Smart Power technology
- PCM encoded digital voice transmission (A-law , µ-law and linear)
- 8 bits parallel microcontroller interface for Intel- and Motorola-like processors
- Multiplexed and demultiplexed address/data bus mode possible
- High performance AD and DA conversion
- Programmable digital filters for
  - Impedance matching
  - Transhybrid balancing
  - Frequency response
  - Gain
- Advanced test capabilities (PEB31666 only)
  - Integrated line and circuit tests
  - Two programmable tone generators

P-MQFP-80-1

P-MQFP-64-1



P-DSO-20-5

1) Abbreviations see **Chapter 9**

Type	Package
PEB 3465 V1.2	P-MQFP-80-1
PEB 31666/4 V1.3	P-MQFP-64-1
PEB 4166/4 V2.3	P-DSO-20-5

- Fully digital programmable DC-Characteristic
  - Programmable constant current from 0 to 70 mA for MuSLIC S2/E2
  - Programmable resistive values from 0 to 2 × 800 Ω
  - Programmable constant voltage
- Programmable integrated Teletax injection and filtering during Active in on-hook and off-hook (PEB 31666 only):
  - Programmable up to 10 Vrms at Ring/Tip-wire of the AHV-SLIC
  - Programmable frequency (12/16 kHz)
- Polarity reversal (programmable soft or hard)
- Integrated (balanced) ringing generation with zero crossing injection (PEB 4166 only):
  - Programmable frequency between 16.6 and 70 Hz
  - Programmable amplitude up to 85 Vrms at Ring/Tip-wire of the AHV-SLIC
- Three operating modes: Power Down, Active and Ringing
- Off-hook detection with programmable thresholds for all operating modes
- Integrated ring trip detection with zero crossing turn off function
- Ground start and loop start possible
- Integrated checksum calculation for CRAM (AC and DC separated)
- Linecard identification
- Sensing of transversal and longitudinal line current
- Battery voltage – 15 V … – 80 V; Auxiliary voltage + 5 V… + 85 V (PEB 4166 only).
- Second negative battery voltage for power saving at short lines
- Boosted battery mode with up to 150 V supply for long telephone lines and up to 85 Vrms balanced ringing (PEB 4166 only)
- Reliable 170 V Smart Power technology
- Standard SMD packages: P-MQFP-64-1 and P-MQFP-80-1 for the low voltage parts and small power package P-DSO-20-5 for the high voltage device

1.2 PEB 3465 (QAP)

1.2.1 Logic Symbol (PEB 3465)

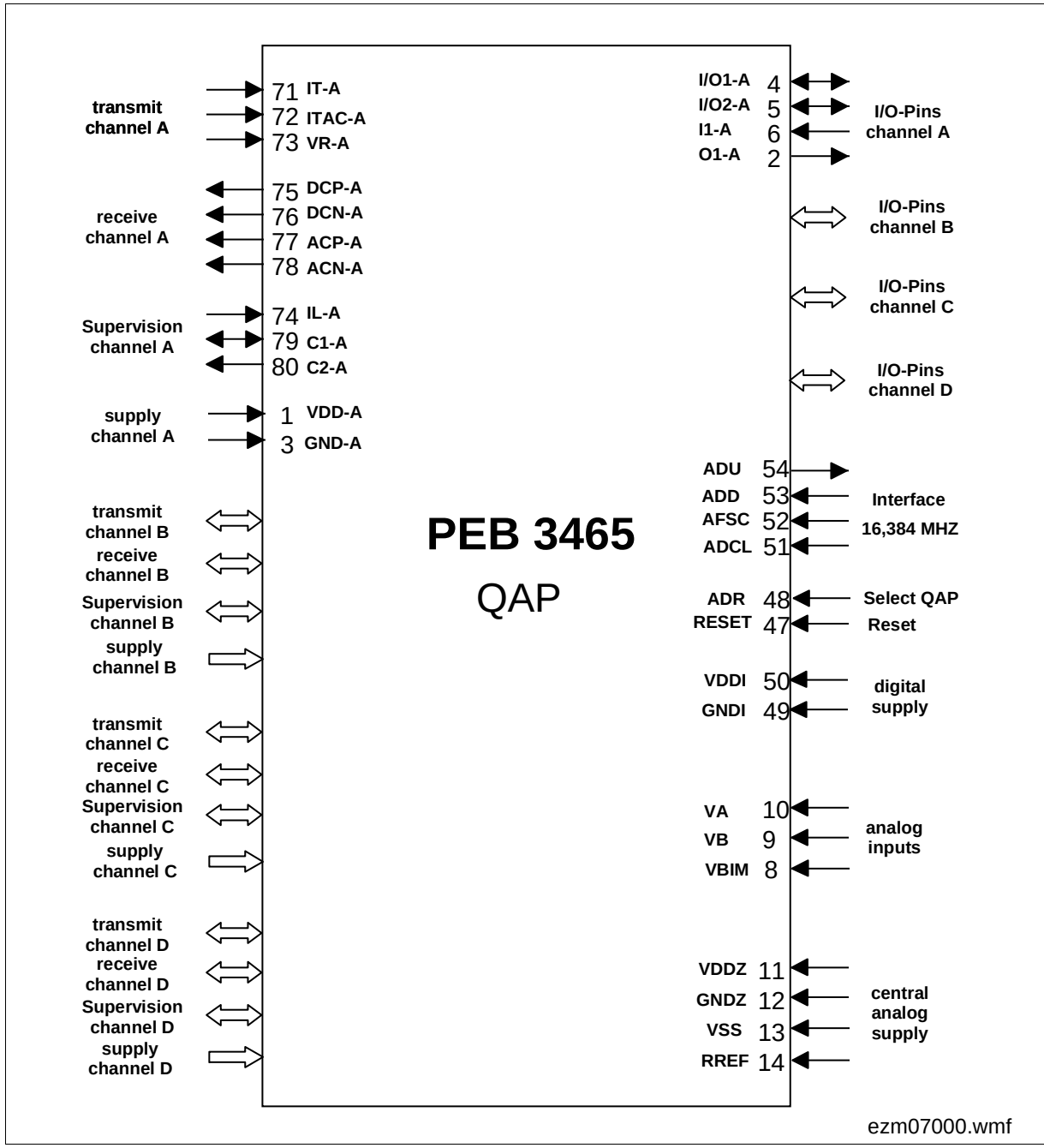


Figure 1 Logic Symbol (PEB 3465)

1.2.2 Pin Configuration (PEB 3465)

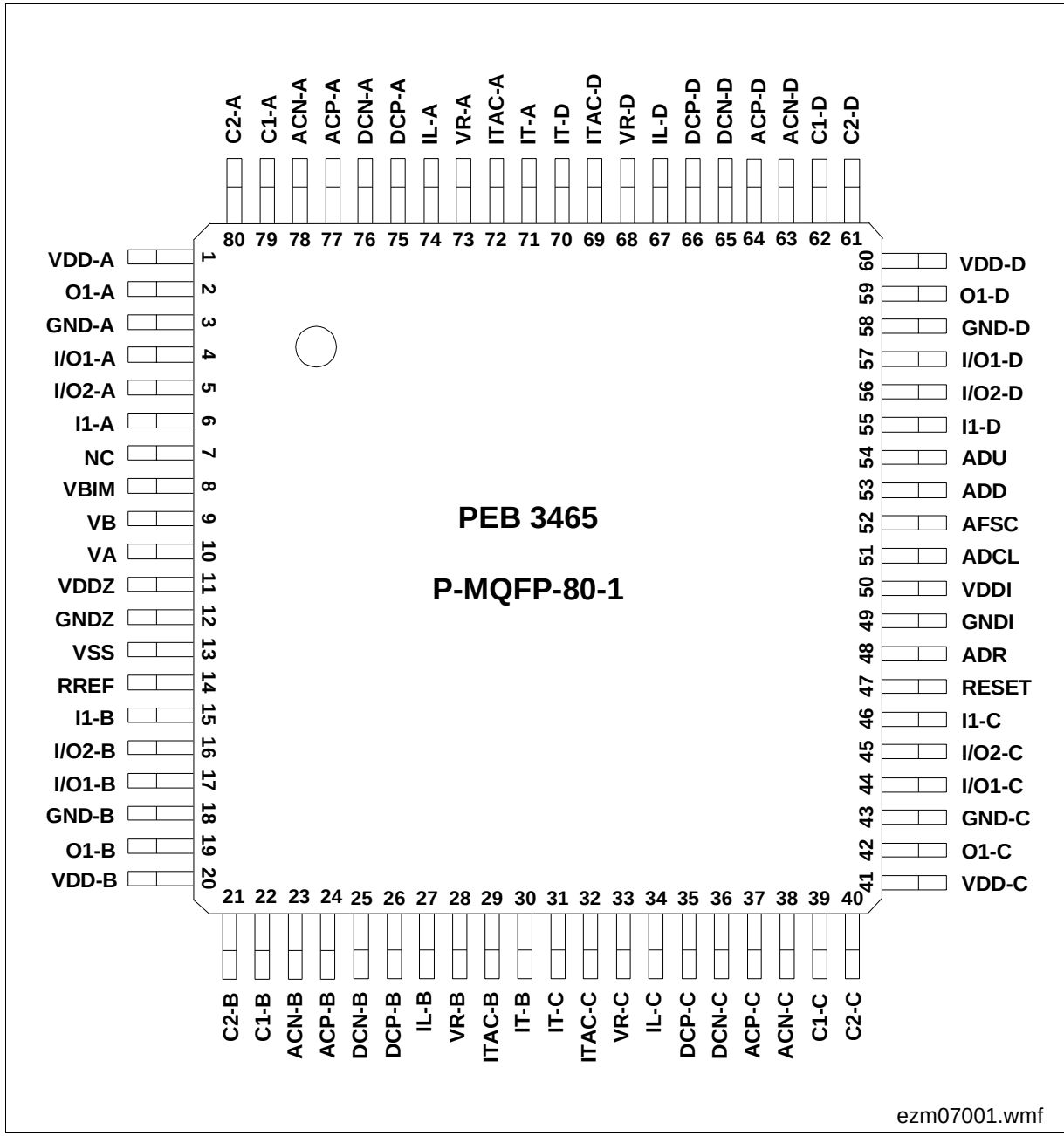


Figure 2 Pin Configuration (PEB 3465)

1.2.3 Pin Definition and Functions (PEB 3465)

The following tables group the pins according to their functions. They include pin number, pin name, type and a brief description of the function.

Pin No.	Name	Type	Function
Power Supply Pins			
1	VDD-A	–	+ 5 V analog supply voltage (channel A)
20	VDD-B	–	+ 5 V analog supply voltage (channel B)
41	VDD-C	–	+ 5 V analog supply voltage (channel C)
60	VDD-D	–	+ 5 V analog supply voltage (channel D)
3	GND-A	–	Analog ground (channel A)
18	GND-B	–	Analog ground (channel B)
43	GND-C	–	Analog ground (channel C)
58	GND-D	–	Analog ground (channel D)
11	VDDZ	–	+ 5 V analog supply voltage (bias)
12	GNDZ	–	Analog ground (bias)
13	VSS	–	– 5 V Analog supply voltage
50	VDDI	–	Digital supply voltage (+ 3.3 V or +5 V)
49	GNDI	–	Digital ground
Interface Pins to MuPP µC (PEB 31666/4)			
54	ADU	O	Analog data upstream
53	ADD	I	Analog data downstream
51	ADCL	I	Analog data-clock
52	AFSC	I	Analog frame sync.
48	ADR	I	Select odd or even port nr.
47	RESET	I	Interface-reset (active high)

Pin No.	Name	Type	Function
Interface to AHV-SLIC (PEB 4166/4)			
71	IT-A	I	Transversal current input (AC+DC), channel A
72	ITAC-A	I	Transversal current input (AC), channel A
73	VR-A	I	Reference input, channel A
74	IL-A	I	Longitudinal current input, channel A
77	ACP-A	O	Two wire output voltage (ACP), channel A
78	ACN-A	O	Two wire output voltage (ACN), channel A
75	DCP-A	O	Two wire output voltage (DCP), channel A
76	DCN-A	O	Two wire output voltage (DCN), channel A
79	C1-A	I/O	Digital Interface to AHV-SLIC, channel A
80	C2-A	O	Digital Interface to AHV-SLIC, channel A
30	IT-B	I	Transversal current input (AC+DC), channel B
29	ITAC-B	I	Transversal current input (AC), channel B
28	VR-B	I	Reference input, channel B
27	IL-B	I	Longitudinal current input, channel B
24	ACP-B	O	Two wire output voltage (ACP), channel B
23	ACN-B	O	Two wire output voltage (ACN), channel B
26	DCP-B	O	Two wire output voltage (DCP), channel B
25	DCN-B	O	Two wire output voltage (DCN), channel B
22	C1-B	I/O	Digital Interface to AHV-SLIC, channel B
21	C2-B	O	Digital Interface to AHV-SLIC, channel B
31	IT-C	I	Transversal current input (AC+DC), channel C
32	ITAC-C	I	Transversal current input (AC), channel C
33	VR-C	I	Reference input, channel C
34	IL-C	I	Longitudinal current input, channel C
37	ACP-C	O	Two wire output voltage (ACP), channel C
38	ACN-C	O	Two wire output voltage (ACN), channel C
35	DCP-C	O	Two wire output voltage (DCP), channel C
36	DCN-C	O	Two wire output voltage (DCN), channel C
39	C1-C	I/O	Digital Interface to AHV-SLIC, channel C

Pin No.	Name	Type	Function
40	C2-C	O	Digital Interface to AHV-SLIC, channel C
70	IT-D	I	Transversal current input (AC+DC), channel D
69	ITAC-D	I	Transversal current input (AC), channel D
68	VR-D	I	Reference input, channel D
67	IL-D	I	Longitudinal current input, channel D
64	ACP-D	O	Two wire output voltage (ACP), channel D
63	ACN-D	O	Two wire output voltage (ACN), channel D
66	DCP-D	O	Two wire output voltage (DCP), channel D
65	DCN-D	O	Two wire output voltage (DCN), channel D
62	C1-D	I/O	Digital Interface to AHV-SLIC, channel D
61	C2-D	O	Digital Interface to AHV-SLIC, channel D

IO Pins[1)]

4	IO1-A	I/O	User-programmable I/O pin, channel A
5	IO2-A[2)]	I/O	User-programmable I/O pin, channel A
6	I1-A	I	Fixed input pin, channel A
2	O1-A	O	Fixed output pin, channel A
17	IO1-B	I/O	User-programmable I/O pin, channel B
16	IO2-B[2)]	I/O	User-programmable I/O pin, channel B
15	I1-B	I	Fixed input pin, channel B
19	O1-B	O	Fixed output pin, channel B
44	IO1-C	I/O	User-programmable I/O pin, channel C
45	IO2-C[2)]	I/O	User-programmable I/O pin, channel C
46	I1-C	I	Fixed input pin, channel C
42	O1-C	O	Fixed output pin, channel C
57	IO1-D	I/O	User-programmable I/O pin, channel D
56	IO2-D[2)]	I/O	User-programmable I/O pin, channel D
55	I1-D	I	Fixed input pin, channel D
59	O1-D	O	Fixed output pin, channel D

Pin No.	Name	Type	Function
Miscellaneous Function Pins			
14	RREF	O	test pin, do not connect
10	VA	I	Voltage sense a
9	VB	I	Voltage sense b
8	VBIM	I	Battery image sense input
Pins not Used			
7	N.C.	–	Not connected (not used)

1) Unused fixed input pn shave to terminated with pull up or pull down.
Unused programmable pins chould be programmed to output.

2) If the PEB3465 is used together with the AHV-SLICs PEB4164 or PEB4166 it is recommended to use the IO2-Pin to drive the C3-Pin of the AHV-SLIC.

1.2.4 Functional Block Diagram (PEB 3465)

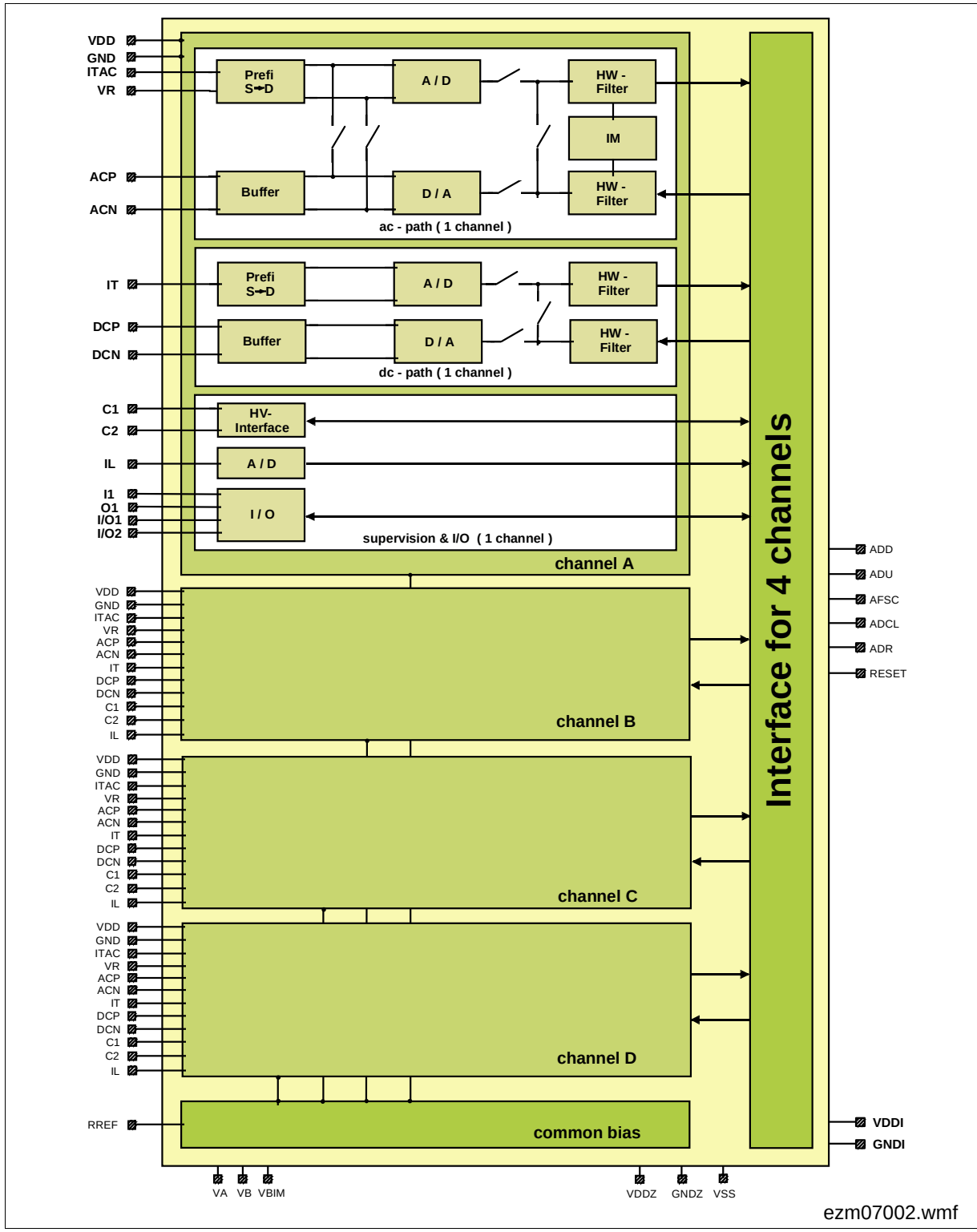


Figure 3 Functional Block Diagram (PEB 3465)

1.3 PEB 31666/4 (MuPP µC)

1.3.1 Logic Symbol (PEB 31666/4)

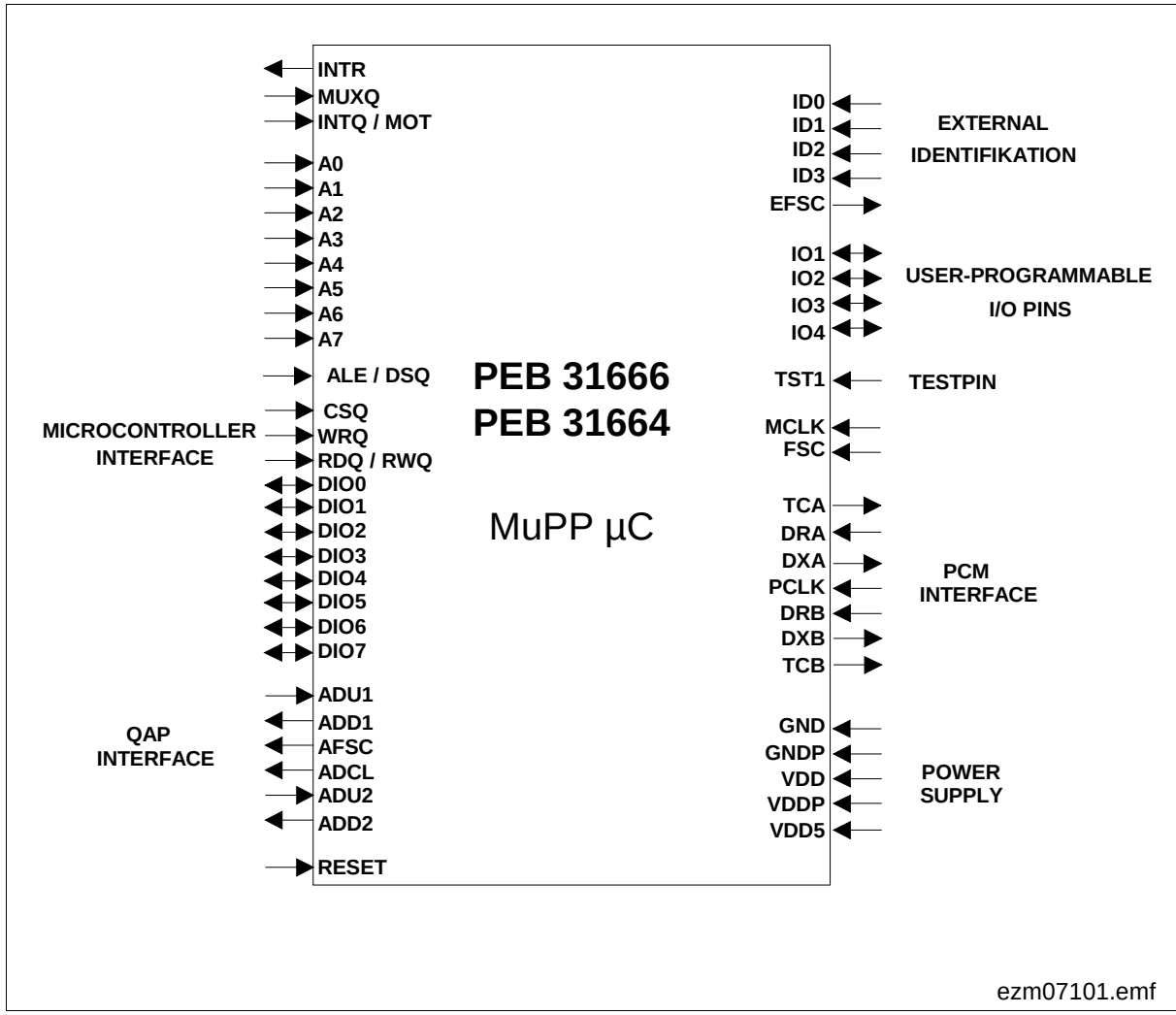


Figure 4 Logic Symbol (PEB 31666/4)

1.3.2 Pin Configuration (PEB 31666/4)

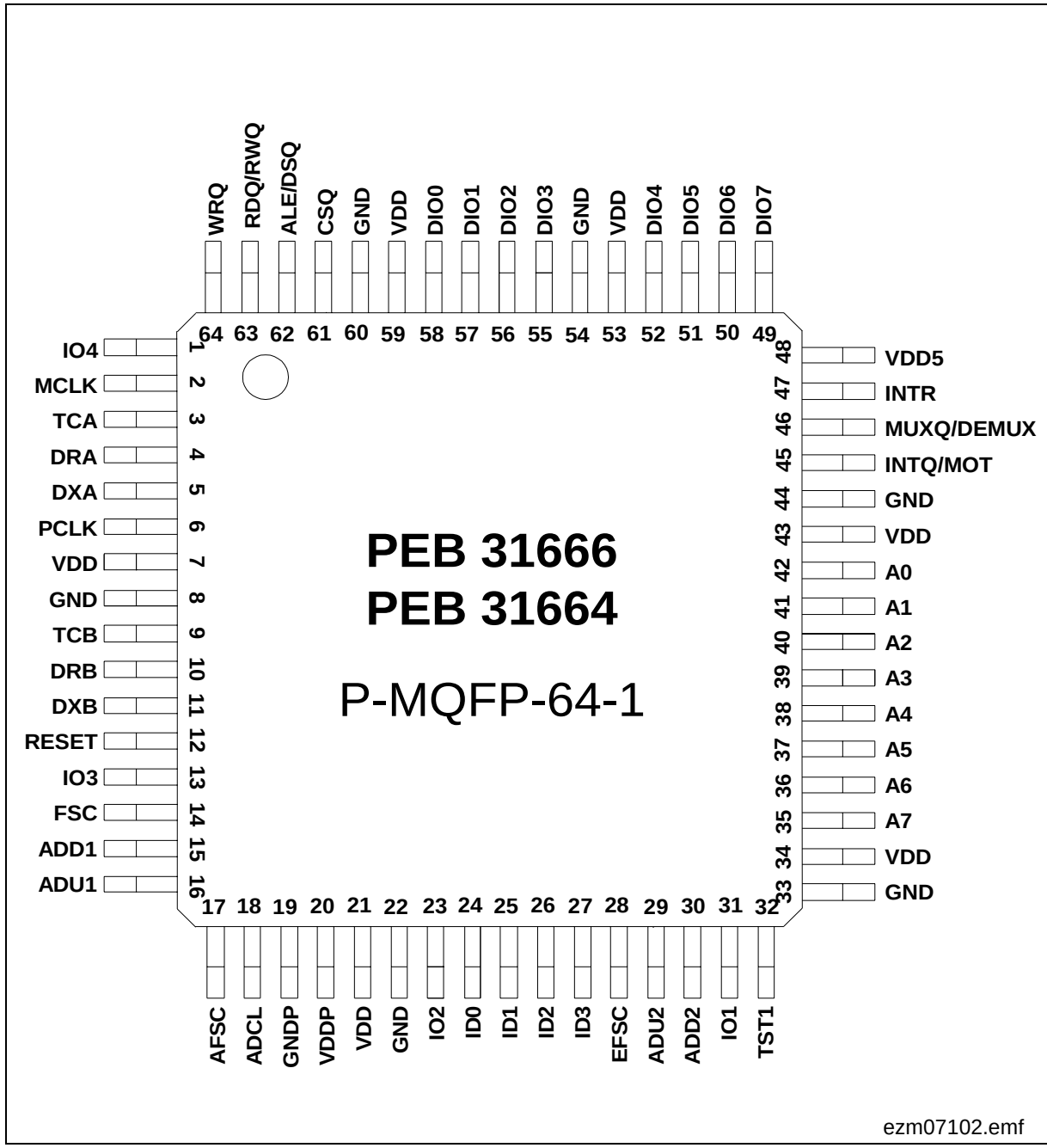


Figure 5 Pin Configuration (PEB 31666/4)

1.3.3 Pin Definitions and Functions (PEB 31666/4)

The following tables group the pins according to their functions. They include pin number, pin name, type and a brief description of the function.

Pin No.	Name	Type	Function
Power Supply Pins			
8, 22, 33, 44, 54, 60	GND	–	Digital ground
19	GNDP	–	Digital ground for PLL
7, 21, 34, 43, 53, 59	VDD	–	+ 3.3 V digital supply voltage
20	VDDP	–	+ 3.3 V digital supply voltage for PLL
48	VDD5	–	+ 5 V digital supply voltage
PCM Pins			
3	TCA	O	Transmit control output for highway A, open drain
4	DRA	I	Receive data for highway A
5	DXA	O	Transmit data for highway A
9	TCB	O	Transmit control output for highway B, open drain
10	DRB	I	Receive data for highway B[1)]
11	DXB	O	Transmit data for highway B
6	PCLK	I	PCM-clock

[1)] If unused, terminate input pins with pull-up or pull-down

Pin No.	Name	Type	Function
MuPP µC/QAP Interface			
15	ADD1	O	1st QAP-bus data downstream
16	ADU1	I	1st QAP-bus data upstream[1)]
17	AFSC	O	QAP frame sync
18	ADCL	O	QAP data-clock
30	ADD2	O	2nd QAP-bus data downstream
29	ADU2	I	2nd QAP-bus data upstream[1)]
Microcontroller Interface			
2	MCLK	I	Master-clock (4.096 MHz)
14	FSC	I	Frame sync
42	A0	I	Address 0
41	A1	I	Address 1
40	A2	I	Address 2
39	A3	I	Address 3
38	A4	I	Address 4
37	A5	I	Address 5
36	A6	I	Address 6
35	A7	I	Address 7
61	CSQ	I	µC chip select (active low)
62	ALE /DSQ	I	µC address latch enable / dataselect (active low), (Motorola)
63	RDQ / RWQ	I	µC data-clock read (active low)/ read-write (Motorola)
64	WRQ	I	µC data-clock write (active low)
46	MUXQ / DEMUX	I	µC Multiplex / demultiplex mode
45	INTQ / MOT	I	µC Intel / Motorola mode
58	DIO0	I/O	µC data / address
57	DIO1	I/O	µC data / address

[1)] In case only 8 Channels are used, terminate ADUx with an pull up of approx. 10kOhm.

Pin No.	Name	Type	Function
56	DIO2	I/O	µC data / address
55	DIO3	I/O	µC data / address
52	DIO4	I/O	µC data / address
51	DIO5	I/O	µC data / address
50	DIO6	I/O	µC data / address
49	DIO7	I/O	µC data / address
47	INTR	O	Interrupt

IO Pins

31	IO1	I/O	User-programmable I/O pin
23	IO2	I/O	User-programmable I/O pin
13	IO3	I/O	User-programmable I/O pin
1	IO4	I/O	User-programmable I/O pin

Miscellaneous Function Pins

12	RESET	I	Reset (active high)
24	ID0	I	External identification. Serial data input for external device (see **“XR7 and XR8 Extended Operation Register 7 to 8” on Page 96**)
25	ID1	I	Must be set to 1 for external identification
26	ID2	I	Must be set to 1 for external identification
27	ID3	I	Must be set to 1 for external identification
28	EFSC	O	External ASIC frame sync
32	TST1	I	Test pin (for normal operation it must be connected to GND)
2	MCLK	I	Master clock 4.096 MHz
14	FSC	I	Frame sync

1.3.4 Functional Block Diagram (PEB 31666/4)

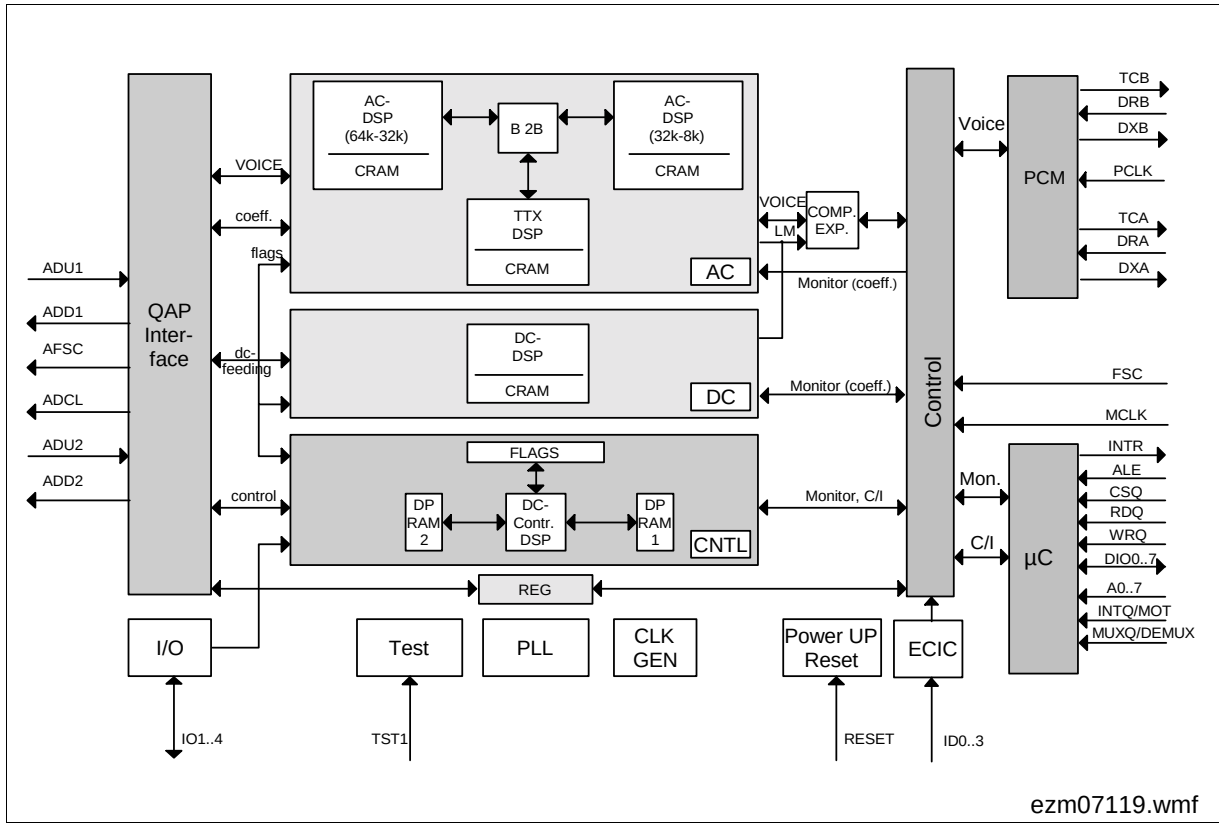


Figure 6 Functional Block Diagram (PEB 31666/4)

1.4 PEB 4166/4 (AHV-SLIC)

1.4.1 Logic Symbol (PEB 4166/4)

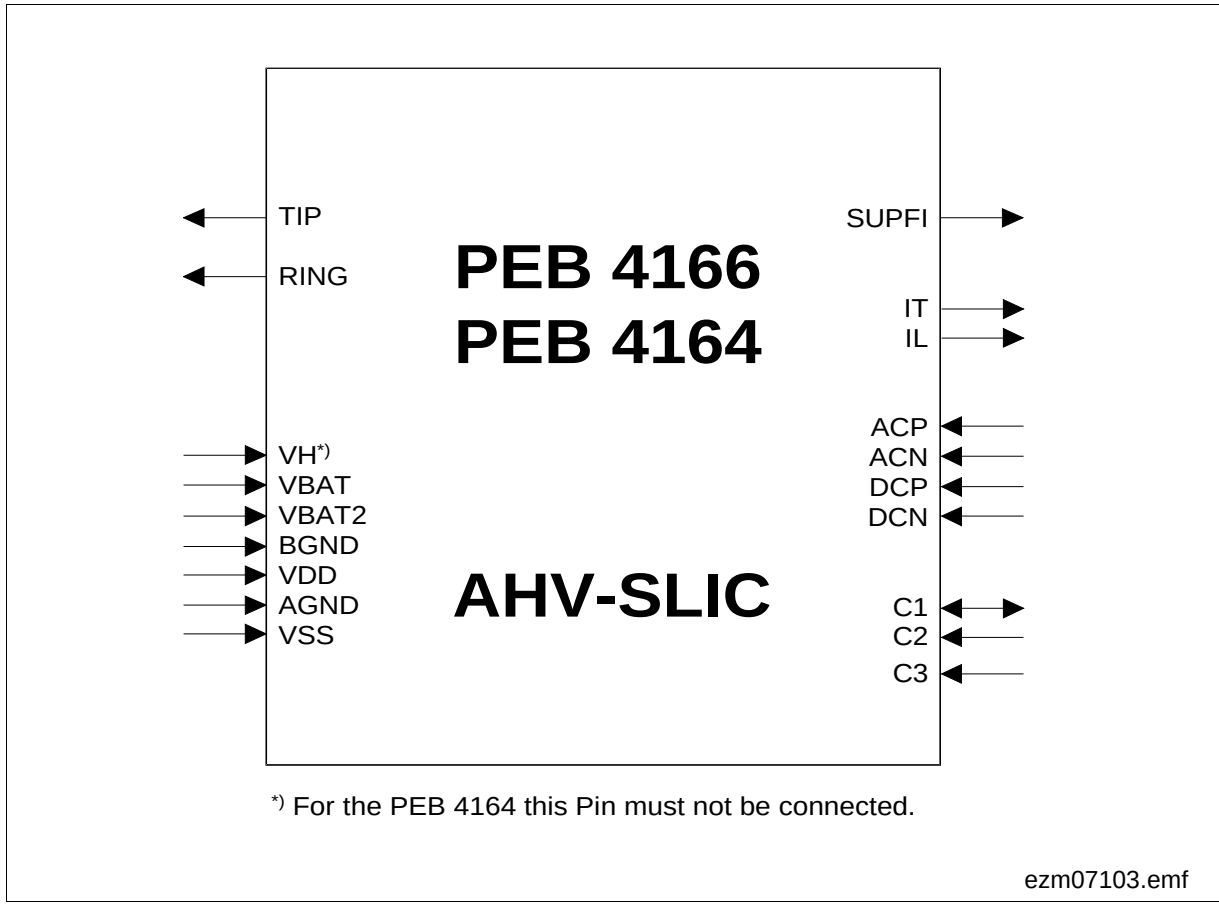
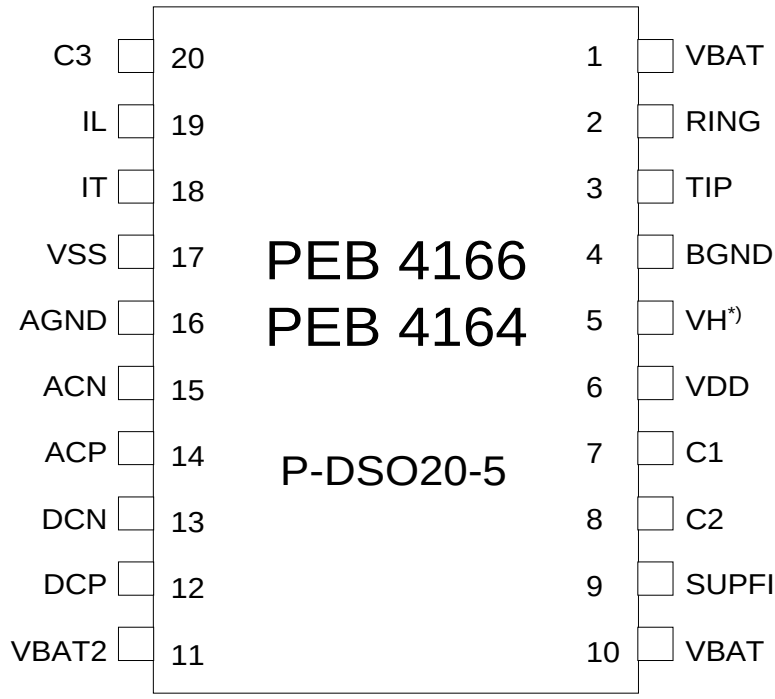


Figure 7 Logic Symbol (PEB 4166/4)

1.4.2 Pin Configuration (PEB 4166/4)



*) For the PEB 4164 this Pin must not be connected.

ezm07104.emf

Figure 8 Pin Configuration (PEB 4166/4)

1.4.3 Pin Definition and Functions (PEB 4166/4)

The following tables group the pins according to their functions. They include pin number, pin name, type and a brief description of the function.

Pin No.	Symbol	Type	Description
Power Supply Pins			
1,10	VBAT	–	Negative battery supply voltage (– 15 … – 80 V), referred to BGND
11	VBAT2	–	Second negative battery supply voltage (– 15 V ≥ VBAT2 ≥ VBAT); allows power saving at short lines. If unused connect to VBAT.
5	VH*)	–	Auxiliary positive battery supply voltage (+ 5 … + 85 V) used in ringing mode. If unused connect to VDD.
4	BGND	–	Battery ground: TIP, RING, VBAT, VBAT2 and VH refer to this pin
6	VDD	–	Positive supply voltage (+ 5 V), referred to AGND
17	VSS	–	Negative supply voltage (– 5 V), referred to AGND
16	AGND	–	Analog ground: VDD, VSS and all signal and control pins with the exception of TIP and RING refer to AGND
Line Interface Pins			
2	RING	O	Subscriber loop connection RING
3	TIP	O	Subscriber loop connection TIP
Interface Pins to QAP			
7	C1	I/O	Ternary logic input, controlling the operation mode; in case of thermal overload this pin sinks a current of typ. 150 µA
8	C2	I	Ternary logic input, controlling the operation mode
20	C3	I	Binary logic input, controlling the operation mode; can be non connected if not used

*) For the PEB 4164 the Pin VH is internal connected to VDD; so it must not be connected externally.

Pin No.	Symbol	Type	Description
12,13	DCP,DCN	I	Differential two wire DC-input voltage; multiplied by factor – 25 and related to (VH – VBAT) / 2, DCN appears at TIP and DCP at RING output, respectively
14,15	ACP,ACN	I	Differential two wire AC-input voltage; multiplied by factor – 3.125, ACN appears at TIP and ACP at RING output, respectively
18	IT	O	Current output representing the transversal current scaled down by a factor of 50.
19	IL	O	Current output: longitudinal line current scaled down by a factor of 50.

Miscellaneous

9	SUPFI	O	Reference voltage defining the common mode line potential. An external capacitance together with the internal 30 kΩ resistance enables supply voltage filtering.

1.4.4 Functional Block Diagram (PEB 4166/4)

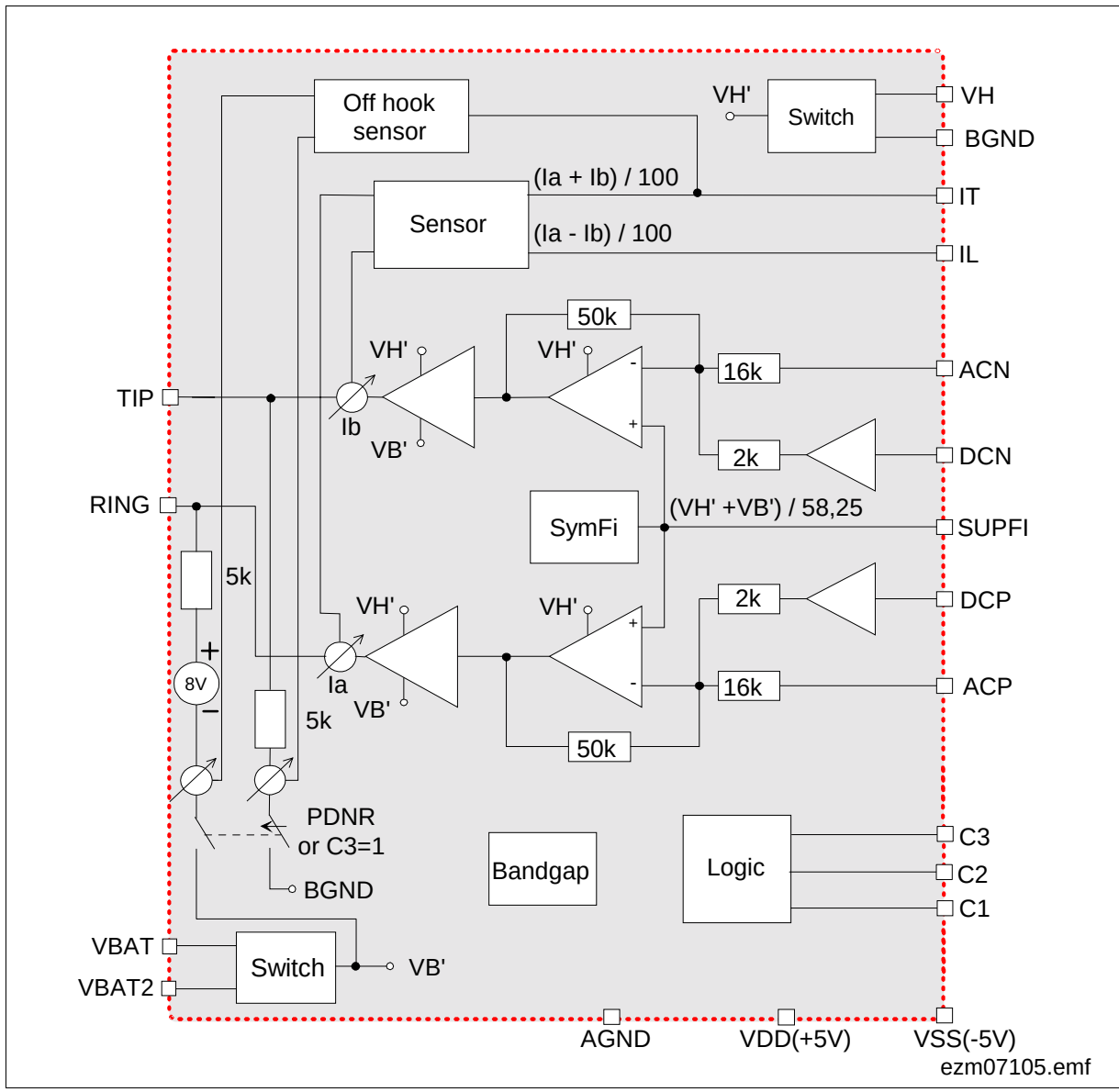


Figure 9 Functional Block Diagram (PEB 4166/4)

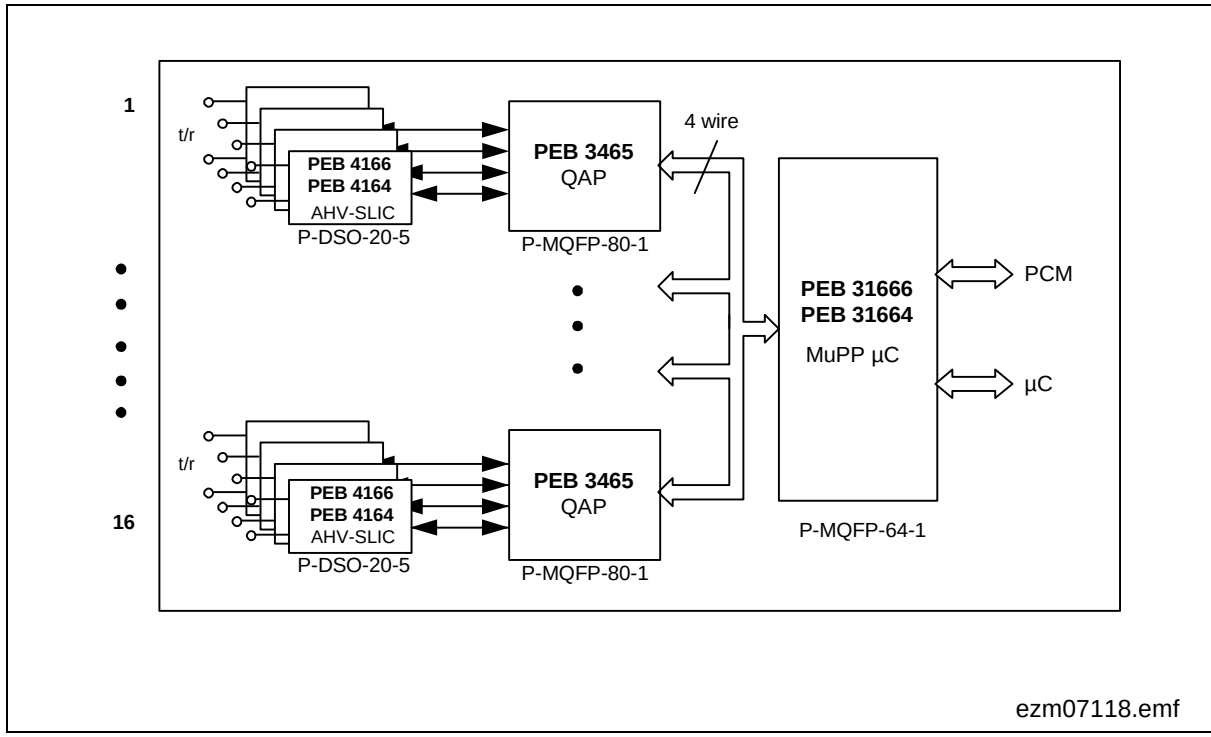


Figure 10 Central Office Analog Linecard for 16 Subscribers

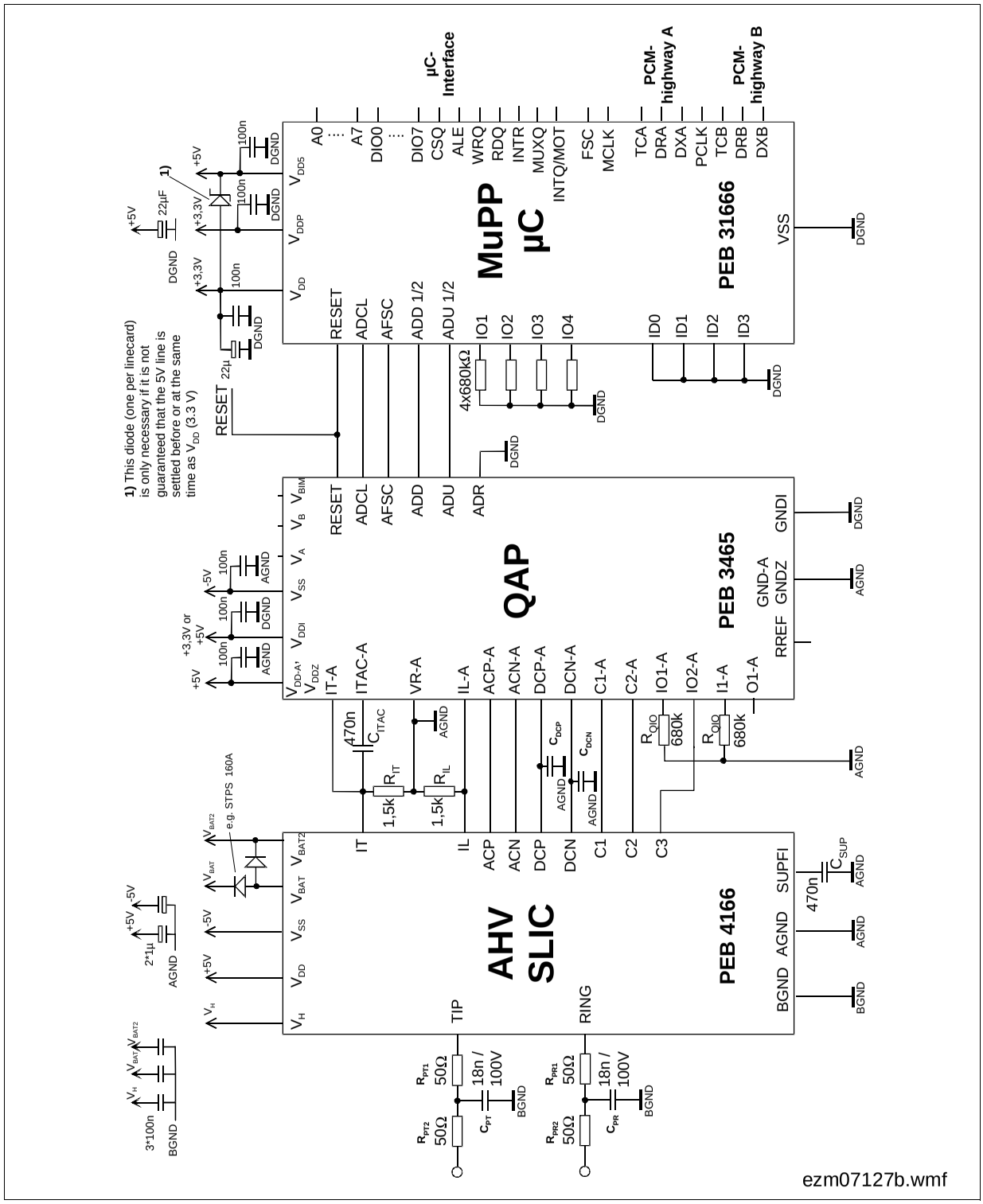


Figure 11 Typical Application Circuit of the MuSLIC Chip Set

For the connection of the AHV-SLIC and the QAP to the MuPP µC only one channel is depicted here.

Table 2 List of Components in Typical Application Circuit (Figure 11)

Symbol	Value			Unit	Tolerance
	min.	typ.	max.		
R_{PT1} [1]	30	50		Ω	0.1 %
R_{PT2} [2]	0	50		Ω	0.1 %
R_{PR1}	30	50		Ω	0.1 %
R_{PR2}	0	50		Ω	0.1 %
R_{IT}		1.5		kΩ	1 %
R_{IL}		1.5		kΩ	1 %
R_{QIO}		680		kΩ	5 %
R_{MIO}		680		kΩ	5 %
C_{PT}	0.2	18	20	nF	10 %
C_{PR}	0.2	18	20	nF	10 %
C_{ITAC}		470		nF	10 %
$C_{DCP/N}$		100		nF	10 %
C_{SUP}		470		nF	10 %

1) Absolut value not critical, but matching with R_{PR1} is important.

2) Absolut value not critical, but matching with R_{PR2} is important.

2 Functional Description

The Multichannel Subscriber Line Interface Codec Filter chip set, MuSLIC, is a logic continuation of the well established family of the Infineon Technologies PCM-Codec-Filter-ICs with the integration of all DC-feeding, ringing, supervision and meterpulse injection features on chip as well. Fabricated in advanced CMOS, BiCMOS and High Voltage technology SPT170 the MuSLIC is tailored for very flexible solutions in analog/ digital communication systems.

The chip set consists of the digital signal processor for 16 channels (MuPP µC, multichannel processor for POTS), the analog/digital and digital/analog converter for 4 channels (QAP, quad analog POTS) and the high voltage interface chip for 1 channel (AHV-SLIC, advanced high voltage subscriber line interface circuit).

The MuPP µC uses the benefits of a DSP not only for the voice channel but even for line feeding and supervision which leads to a very high flexibility without the need of external components. Based on an advanced digital filter concept, the PEB 31666 (MuPP µC) and the PEB 3465 (QAP) provides excellent transmission performance. The new filter concept leads to a maximum of independence between the different filter blocks. Each filter block can be seen as a one to one representative of the corresponding network element. Together with the software package MuSLICOS, filter optimizing to different applications can be done in a clear and straight forward procedure. The AC frequency behavior is mainly determined by the digital filters. Using the oversampling 1 bit SD-AD/ DA converters, linearity is only limited by second order parasitic effects.

The digital solution offers free programmability of feeding current and voltage as well as very fast settling of the DC-operating point after transitions. A 0.3 Hz lowpass filter in the DC-loop is mainly responsible for the system stability.

Additionally Teletax generation and filtering is implemented as well as free programmable balanced ring generation with zero-crossing injection. Off-hook detection with programmable thresholds is possible in all operating modes. To reduce overall power consumption of the linecard, the MuPP µC, the QAP and the AHV-SLIC provide a Power Down mode.

To program the MuSLIC or to get status information about the chip set or the system the MuSLIC has a 8-bit-parallel simple Microcontroller Interface.

The AHV-SLIC-E PEB4166 provides battery feeding between – 15 V and – 80 V and ringing injection with a differential ring voltage up to 85 Vrms. In order to achieve these high amplitudes, an auxiliary positive battery voltage is used during ringing. This voltage can also be applied to drive very long telephone lines. The AHV-SLIC-S PEB4164 does not support this auxiliary positive voltage.

A kind of power management can be performed by using a second battery supply voltage for power saving at short lines.

The AHV-SLIC is designed for a voltage feeding - current sensing line interface concept and provides sensing of transversal and longitudinal currents on both wires. In Power Down mode the AHV-SLIC is switched off turning the line outputs to a high impedance state. Off-hook supervision is provided by activating a line current sensor.

2.1 Principles

2.1.1 Signal Flow Graph: AC

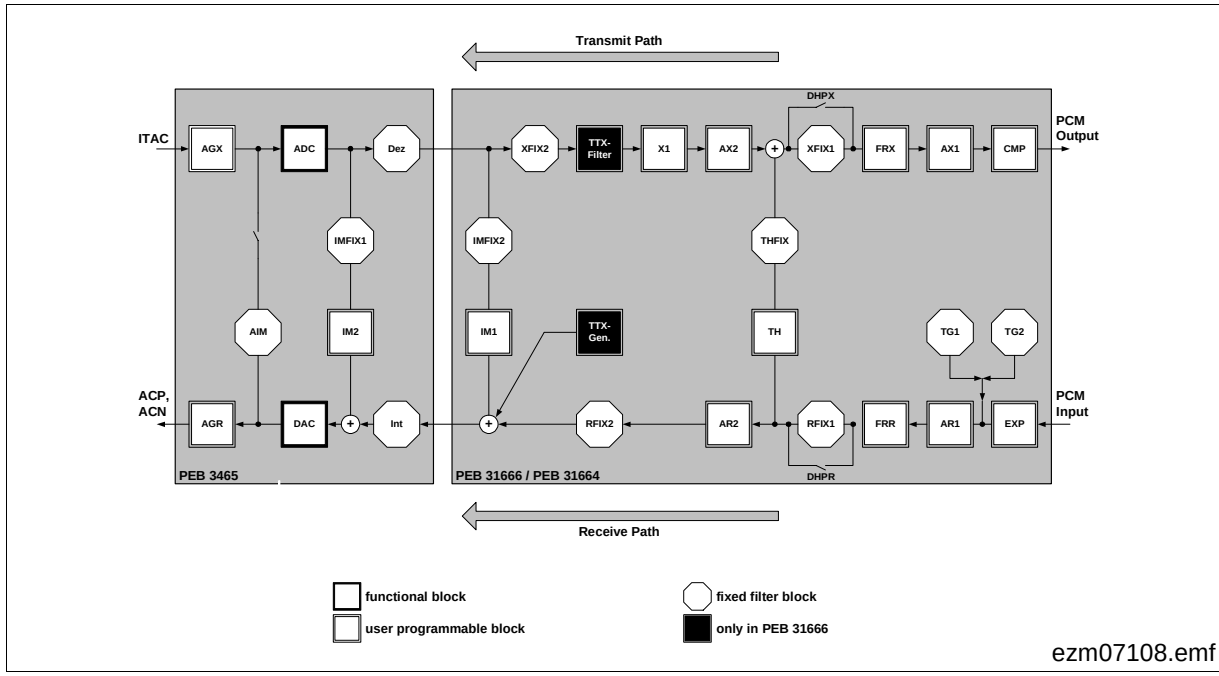


Figure 12 Signal Flow Graph: AC

Transmit Path

The analog input signal has to be connected to pin ITAC of the PEB 3465 by an external capacitor (470 nF) for AC/DC separation. After passing a programmable gain stage (AGX = 0, 3.5 or 9.5 dB, digitally compensated) and a simple antialiasing prefilter the voice signal is converted to a 1-bit digital data stream in the ΣΔ-converter. The first down sampling steps are done in fast running digital hardware filters on the PEB 3465. This down sampled AC-signal (64 kHz sampling rate) is sent to the MuPP µC via the MuPP µC/QAP-Interface in the ADU-channel. The following signal processing is done in the DSP-machine of the MuPP µC. The benefits of this are the programmability of frequency and gain behavior. At the end the fully processed signal is transferred to the PCM Interface in a PCM-compressed (A-law / µ-law) signal representation.

Receive Path

The digital input signal is received via the PCM Interface of the MuPP µC. Expansion, PCM-lowpass-filtering, gain correction and frequency response correction are the next steps which are done by the DSP-machine. This 64 kHz AC signal is sent from the MuPP µC to the QAP via the MuPP µC/QAP-Interface in the ADD-channel. The up sampling interpolation steps are processed by fast hardware structures in the PEB 3465 to reduce the DSP-workload. The 1-bit data stream is then converted to an analog equivalent. A subsequent programmable gain stage (AGR = 0 or – 3,5 dB) and smoothing filter provides the AC output signal at the pins ACP and ACN of the PEB 3465 for direct connection to the AHV-SLIC.

Loops

There are two different loops implemented: The Impedance Matching (IM) loop which is divided into 3 separate loops to guarantee very high flexibility to various impedances, and the Transhybrid Balancing (TH) loop.

2.1.2 Signal Flow Graph: DC

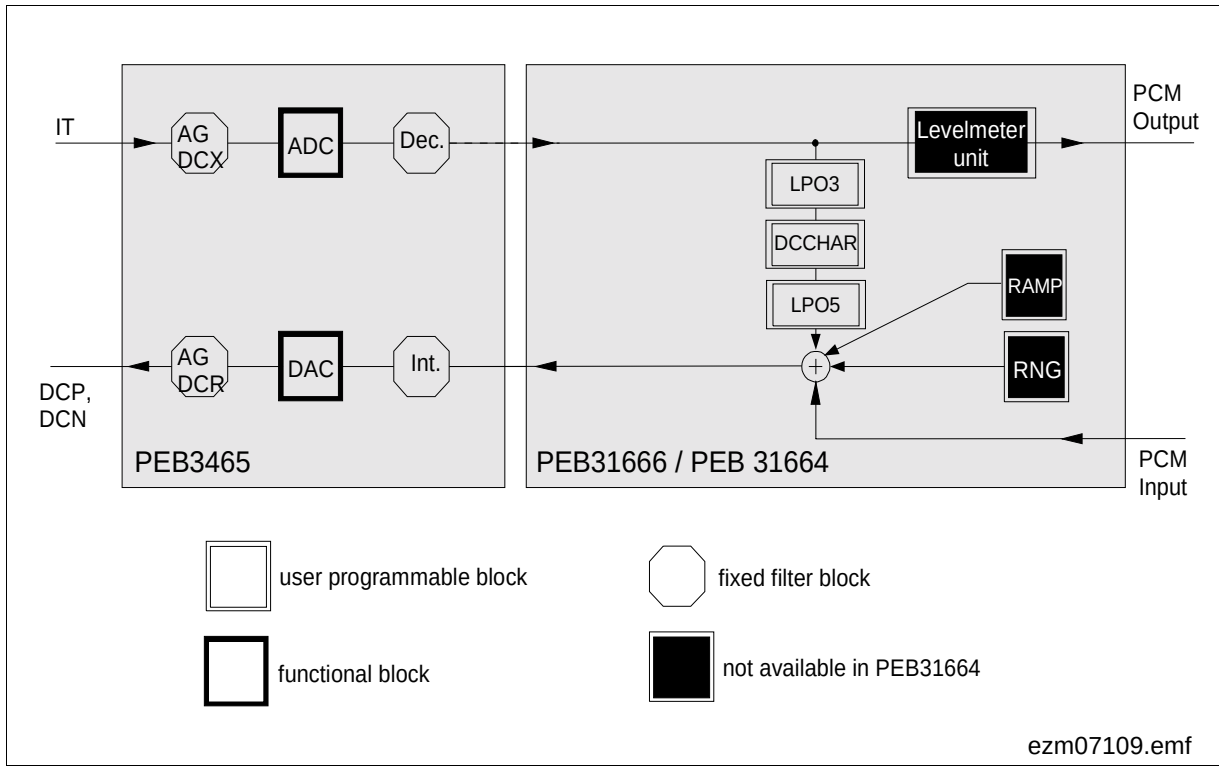


Figure 13 Signal Flow Graph: DC

DC Characteristic

The incoming information (transmit direction) at pin IT (scaled transversal AC + DC-current, transferred to a voltage via an external 1.5 kΩ resistor at IT) passes first a antialiasing filter and is then converted to a 1-bit digital data stream in the ΣΔ-converter. Down sampling is done in hardware filters of the PEB 3465. This DC-information (2 kHz sampling rate) is then fed to the MuPP µC where it is first lowpass filtered (0.3 Hz corner frequency) for stability and noise reasons. The following DC-characteristic consists of three branches which represents different kinds of feeding behavior. In typical applications it acts as a programmable constant current source (R_i > 30 kΩ). If the desired value cannot be held feeding switches automatically and smoothly to the resistive branch at V_{Lim}. The internal resitance in this range is programmable between 0 and 1.6kOhm (external fuse resistors not included). In the third branch the DC-Characteristic switches to a constant voltage behavior. In this area the slope of the DC-Characteristic is determined by the external fuse resistors. For superimposing voice as well as Teletax pulses the necessary drop at the line can be calculated and taken into account as well. The outgoing bit stream (2 kHz sampling rate), representing the DC-feeding value is then sent back to the PEB 3465 where a 1-bit ΣΔ-converter and a following smoothing filter (using 2* 100nF external capacitors) establish the desired values at the pins DCP and DCN, respectively. Depending on the operating mode (Active, Ringing, Active with Boosted Battery) a gain of 0 or 4 dB is inserted.

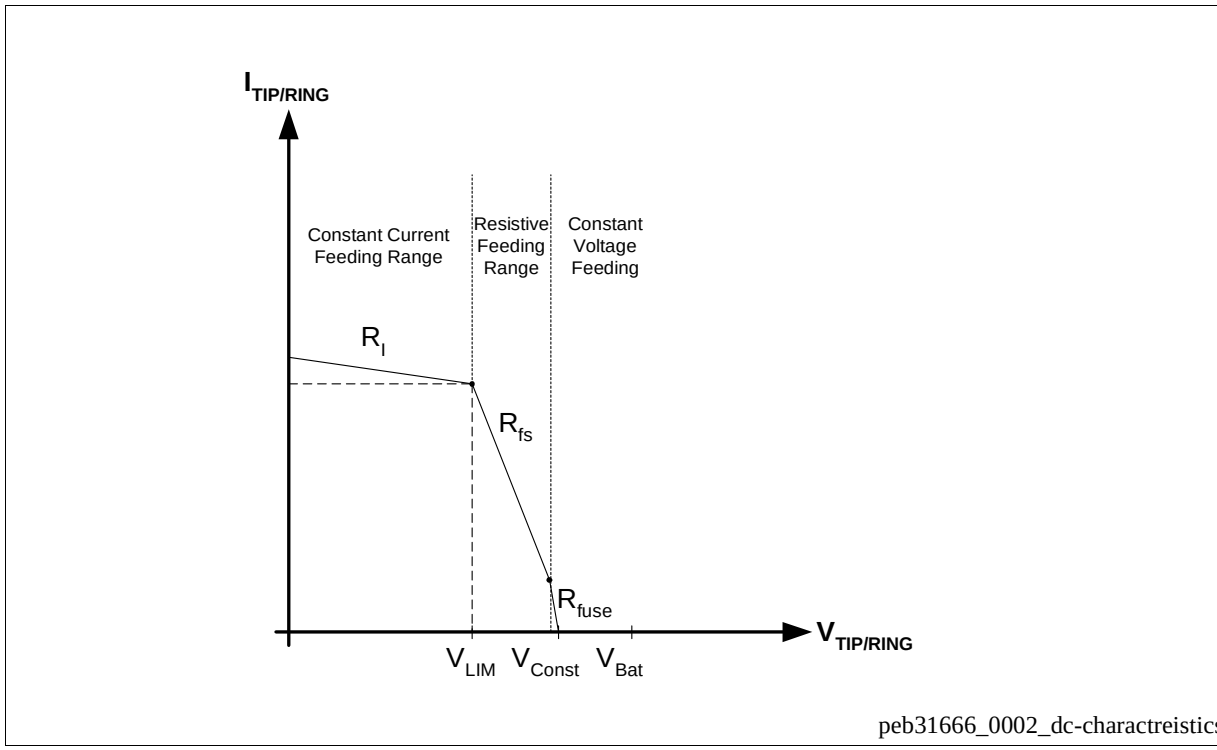


Figure 14 DC Characteristic in Normal Battery Mode

Supervision

The HOOK-information is the most important one and is provided via the µC-Interface (SCR8-4: HOOK; see **Page 82**), in all operating modes:

- Power Down: In this state the transversal line current is sensed by the AHV-SLIC and fed to the PEB 3465 via pin IT. Off-hook is detected if the voltage at IT exceeds a programmed value.
- Active: Off-hook is detected if the incoming voltage at IT exceeds a programmed value. To avoid instable information, lowpass filtering and a hysteresis is provided.
- Ringing: Off-hook is detected if the DC-value at IT exceeds the programmed Ring Trip threshold. The AC-value is filtered automatically. Ring Trip detection is reported within 2 cycles of the ring period and then the internal ring generator is switched off within 2 cycles at zero crossing of the ring voltage.

For Ground Key information the AHV-SLIC provides the longitudinal current information at the pin IL. The PEB 3465 uses a ΣΔ-converter - similar to the DC-transmit path - to convert this signal to its digital representation. The accuracy is ± 8% compared to ± 5% of the DC-path. The 1-bit digital data stream is also down sampled and sent to the MuPP µC via the ADU-channel of the MuPP µC/QAP-Interface. Generation of the Ground Key bit is done in the MuPP µC (SCR8-3: GNK; see **Page 82**)

Additional Features

The PEB 3465 provides three general purpose input pins (VA, VB, VBIM) for measuring. Via the MuPP µC/QAP-Interface it is possible to select one of these inputs for the measurement. The DC-signal at the selected input is converted to digital using the same ΣΔ-converter as for Ground Key information (accuracy of ± 8%) and sent to the MuPP µC. The input range is between – 2.4 V … + 2.4 V. As a further selection it is also possible to measure the internal VDDZ-voltage of the PEB 3465. This voltage is internal divided by 4 and can be measured by setting VDDIM.

2.1.3 AHV-SLIC

The Advanced High Voltage Subscriber Line IC's PEB4166 / PEB4164 are reliable interfaces between the telephone line and the QAP/MuPP.

The AHV-SLIC supports AC and DC control loops based on feeding a voltage V_{TR} to the line and sensing the transversal line current I_{Trans} (see **Figure 15**).

DC- and AC-voltages are handled separately with different gain on the AHV-SLIC. Both are applied differentially via pins DCP, DCN, and ACP, ACN, respectively. The line voltages V_R and V_T are the amplified input voltages, related to the mean supply voltage.

$V_T = V_{TIP} = (V_H' + V_B') / 2 - 25 \times V_{DCN} - 50/16 \times V_{ACN}$
$V_R = V_{RING} = (V_H' + V_B') / 2 - 25 \times V_{DCP} - 50/16 \times V_{ACP}$.

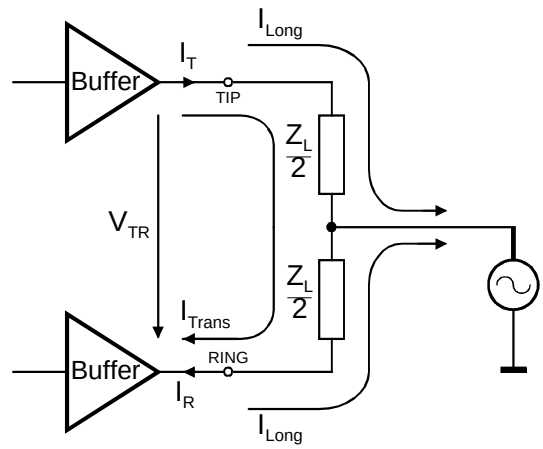
Note: Active mode: $V_H' = 0$, $V_B' = V_{BAT}$
Boosted battery mode: $V_H' = V_H - 2\ V$, $V_B' = V_{BAT}$ [1)]
Active2 mode: $V_H' = 0$, $V_B' = V_{BAT2}$

The transversal line voltage $V_{TR} = V_T - V_R$ is simply related to the input voltages:

$$V_{TR} = 25 \times (V_{DCP} - V_{DCN}) + 50/16 \times (V_{ACP} - V_{ACN}) = 50 \times V_{DCP} + 6.25 \times V_{ACP}$$

A reversed polarity of V_{TR} is easily obtained by changing the sign of $(V_{DCP} - V_{DCN})$.
Scaled images of the transversal and longitudinal currents are measured and provided at the IT and IL pin, respectively:

$I_{IT} = (I_T + I_R)/100 = I_{Trans}/50$ $\quad$ $I_{IL} = (I_T - I_R)/100 = I_{Long}/50$



$I_{Trans} = (I_T + I_R)/2$ $\quad$ $I_{Long} = (I_T - I_R)/2$

ezm07110.emf

Figure 15 Definition of Output Current Directions

1) For the AHV-SLIC-S (PEB 4164) VH = VDD = 5V

2.1.3.1 Operating Modes

The AHV-SLIC operates in different modes controlled by ternary logic signals at the C1 and C2 input and the binary logic signal at the C3 input (see **Table 3** and **Table 4**).

Table 3 Programming of Operating Modes (Pin C3 = 0 V or open)

C3 = 0V or open		C2 (Pin 8)		
		VIL	**VIM**	**VIH**
C1 (Pin 7)	**VIL**	PDNR-L	PDNR	HIR
	VIM	PDNH	BB-50	HIT
	VIH	ACT2	ACT	HIRT

PDNH..... Power Down High Impedance
PDNR..... Power Down Resistive
PDNR-L .... Power Down Resistive-Load
ACT..... Active Mode
ACT2..... Active Mode using VBAT2
BB-50..... Boosted Battery with min. 50 mA current limitation
HIR..... Ring wire set to high impedance
HIT ..... Tip wire set to high impedance
HIRT ..... Ring and Tip wires set to high impedance

Note:

Table 4 Programming of Operating Modes (Pin C3 = 5 V)

C3 = 5 V		C2 (Pin 8)		
		VIL	**VIM**	**VIH**
C1 (Pin 7)	**VIL**	PDNR-L	PDNR	HIR-R
	VIM	PDNH-R	BB-100	HIT-R
	VIH	ACT2-R	ACT-R	HIRT-R

Note: The '-R' suffix in Table 4 means that there is an internal 5 kΩ connection between TIP and GND and also between RING and VBAT.

BB-100 .....Boosted Battery with min. 90 mA current limitation (without 5 kΩ)

The Power Down (PDN) states are intended to reduce power consumption of the linecard to a minimum: the AHV-SLIC is switched off completely, no operation except off-hook supervision is available.

With respect to the output impedance of TIP and RING three PDN-modes have to be distinguished:

– The PDNR (Power Down Resistive) mode provides a connection of 5 kΩ each from TIP to BGND and RING to VBAT, respectively, while the outputs of the buffers show high impedance. The current through these resistors is sensed, 1/10 is transferred to the IT pin to allow off-hook supervision.
– The PDNH (Power Down High Impedance) mode offers high impedance at TIP and RING.
– The Power Down Resistive - Load (PDNR-L) state is automatically activated for a duration of 2 ms on any Power Down mode to any Active mode transition. The function is to preload the SUPFI capacitor in order to suppress line voltage transients.

Active (ACT): This is the regular transmit and receive mode for voiceband and Teletax. The line driving section is operated between VBAT and BGND.

Active2 (ACT2): This is the regular transmit and receive mode for voiceband and Teletax in which the reduced battery voltage VBAT2 is used (allows power saving at short lines). The line driving section is operated between VBAT2 and BGND.

Boosted battery (BB)[1]**:** In order to provide a balanced ring signal of up to 85 Vrms or to drive longer telephone lines, an auxiliary positive battery voltage VH is used, enabling a higher voltage across the line. Transmission performance remains unchanged compared with ACT mode.

High Impedance (HIR/HIT/HIRT)[1]**:** In this mode each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while the current through the RING output still can be measured by IT or IL. Programming HIR switches off the RING buffer. In the mode HIRT both buffers show high impedance.

2.1.3.2 Current Limitation / Overtemperature

In any operating mode except PDN the total current in the buffer output stages is limited to a maximum value of typically 100 mA. (exception modes with suffix "- 50")

If, however, the junction temperature exceeds 165 °C (typ.), the buffers are switched off completely; switching on again occurs with a hysteresis of 20 °C, i.e. at T_j = 145 °C.

Besides, for signalling overtemperature, the AHV-SLIC drains a current I_{OT} from pin C1. This current is sensed by the QAP and transferred in the ADU channel to the MuPP µC. The MuPP µC generates an interrupt signal on the µC interface, where the overtemperature condition can be identified by reading the interrupt register, SCR8 and TCR0.

1) Not possible together with PEB 4164

3 Interfaces

3.1 PCM Interface

Two serial PCM-interfaces are used for the transfer voice data. The PCM-interface consist of 8 pins:

PCLK: PCM-clock, 512 kHz to 8192 kHz

FSC: Frame synchronization clock, 8 kHz

DRA: Receive data input for PCM-highway A

DRB: Receive data input for PCM-highway B

DXA: Transmit data output for PCM-highway A

DXB: Transmit data output for PCM-highway B

TCA: Transmit control output for PCM-highway A, active low during transmission

TCB: Transmit control output for PCM-highway B, active low during transmission

The Frame Sync (FSC) pulse identifies the beginning of a receive and transmit frame for all of the 16 channels. The PCLK clock is the signal to synchronize the data transfer on both lines DXA (DXB) and DRA (DRB). Bytes in all channels are serialized to 8 bit width and MSB first. As a default setting, the rising edge indicates the start of the bit, while the falling edge is used to latch the contents of the received data on DRA (DRB). If the double clock rate is chosen (twice the transmission rate) the first rising edge indicates the start of a bit, while the second falling edge is used for latching the contents of the data line DRA (DRB) by default.

The data rate of the interface can vary from 2*512 kb/s to 2*8192 kb/s (2 highways) A frame may consist of up to 128 time slots of 8 bits each. In the Time Slot Configuration registers SCR6 and SCR7 the user can select an individual time slot, and an individual PCM-highway, for any of the 16 voice channels. Receive and transmit time slots can be programmed individually in normal mode (PCM) and in linear mode. An extra delay of up to 7 clocks, valid for all channels, as well as the sampling slope may be programmed (see register XR6).

When the MuPP µC is transmitting data on DXA (DXB), pin TCA (TCB) is activated to control an extra external driving device.

The following table shows possible examples for the PCM-interface, other frequencies like 768 kHz or 1536 kHz are also possible.

Table 5 PCM Interface Examples

	Frequency [kHz]	**Single/Double** [1/2]	**Time Slots** [per highway]	**Datarate** [kbit/s per highway]
	512	1	8	512
	1024	2	8	512
	1024	1	16	1024
	2048	2	16	1024
	2048	1	32	2048
	4096	2	32	2048
	4096	1	64	4096
	8192	2	64	4096
	8192	1	128	8192
Formula	**f**	**1**	**f/64**	**f**
Formula	**f**	**2**	**f/128**	**f/2**

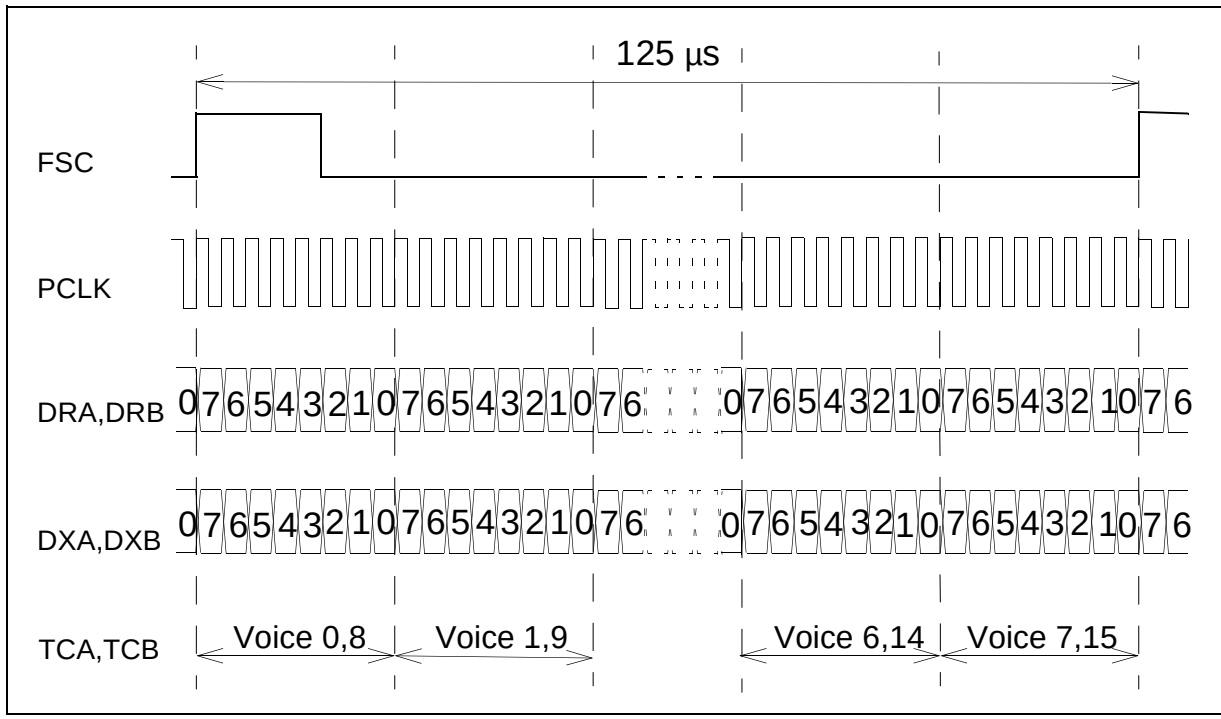


Figure 16 Example for Single Clock Rate, 512 kb/s

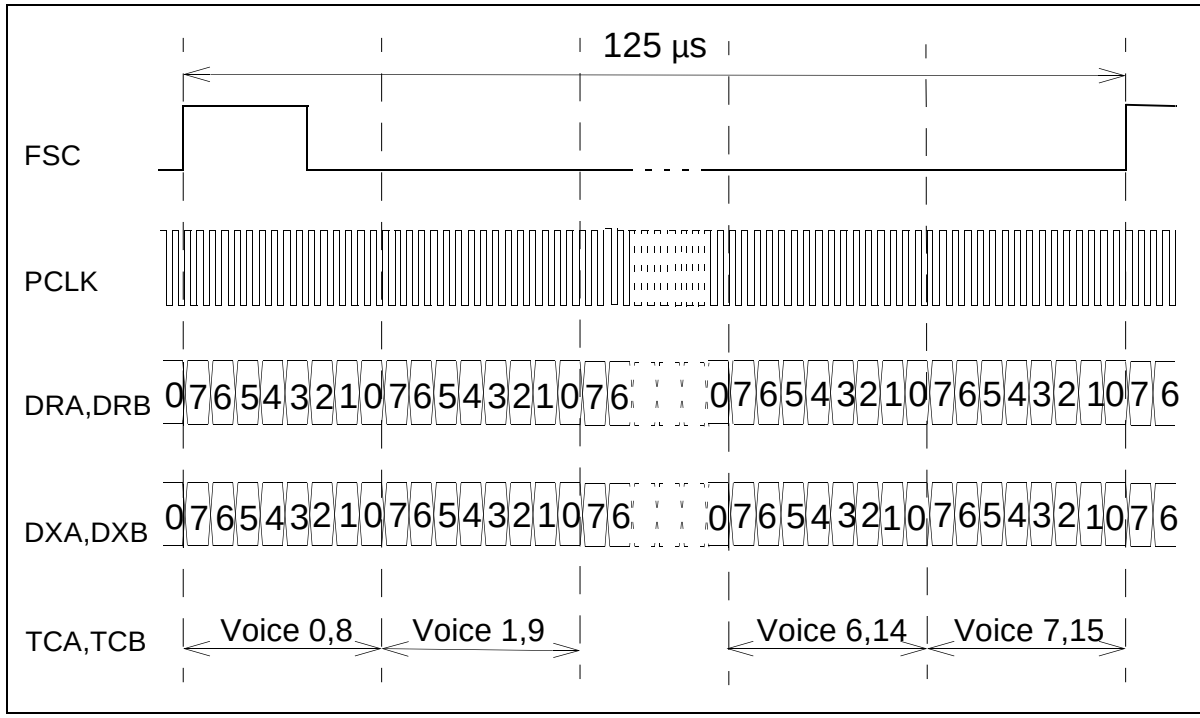


Figure 17 Example for Double Clock Rate, 512 kb/s

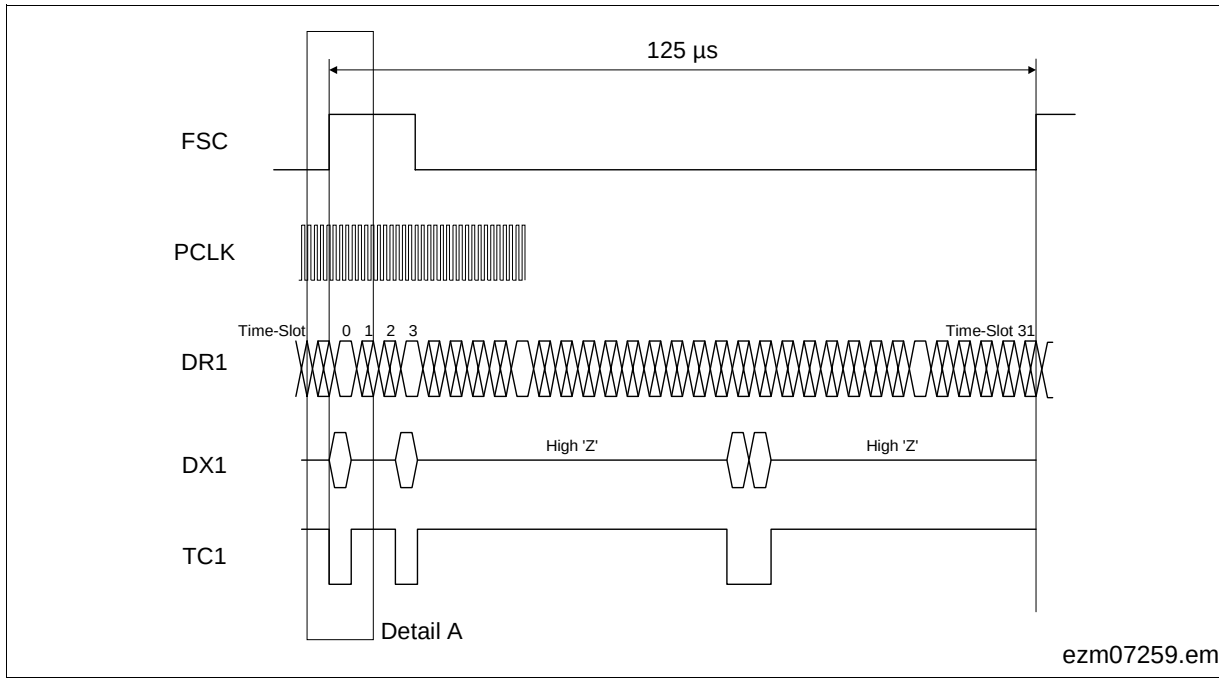


Figure 18 2048 kb/s, Single Clock Operation, only Highway A used

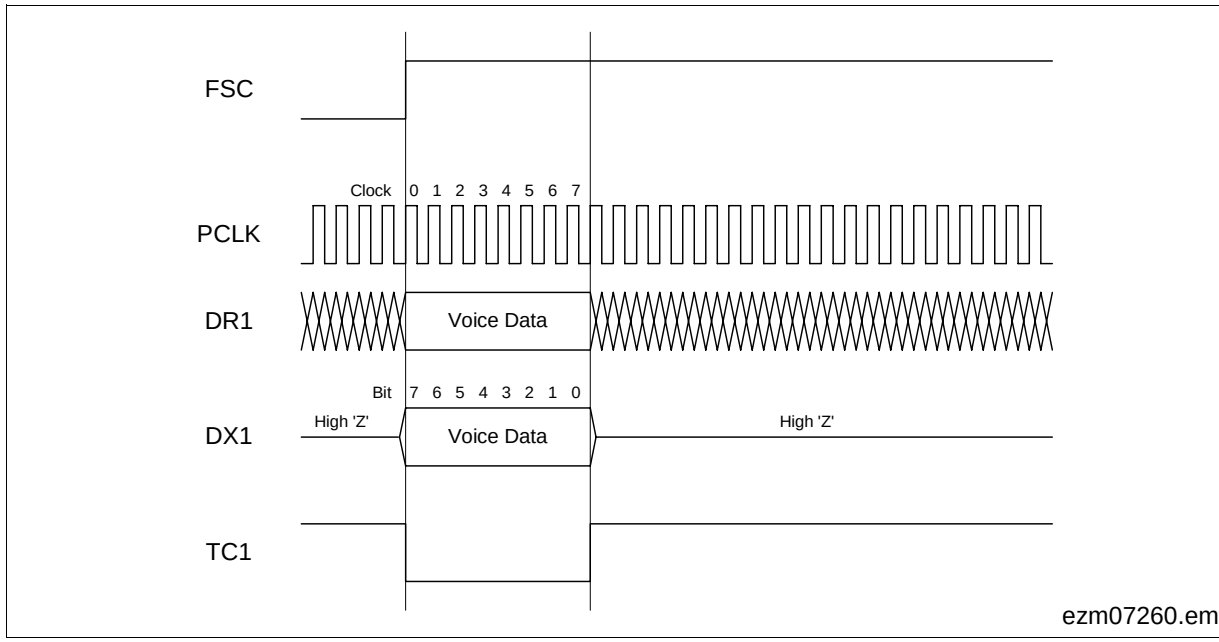


Figure 19 Detail A in Figure 18

For special purposes the DRA/B and DXA/B pins may be strapped together, and form bi-directional data-‘pin’ (like SIP with the SLD-bus).

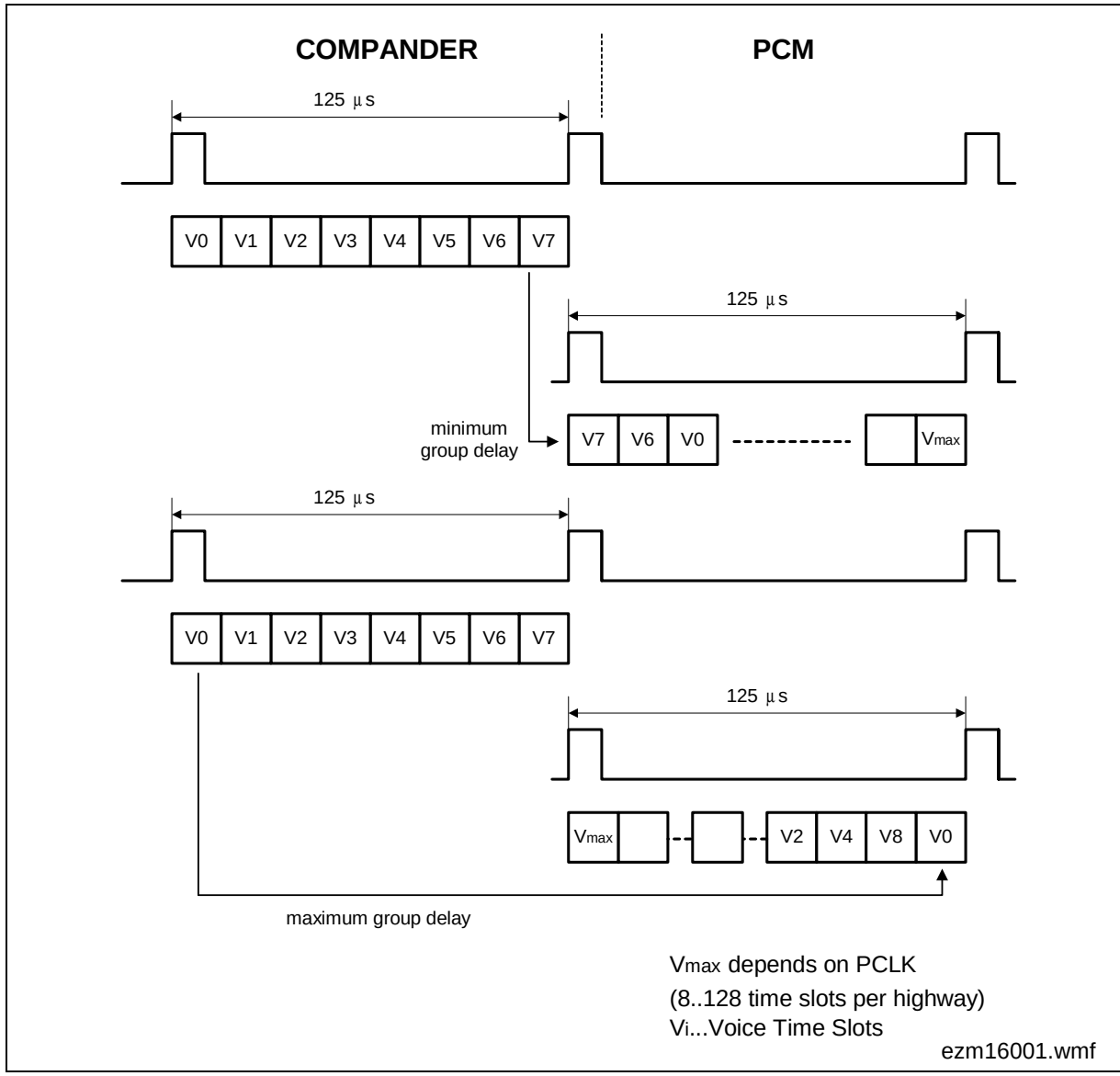


Figure 20 PCM-Group Delay Transmit

The group delay of the voice has 1 FSC (in average).

Figure 20 shows the conditions for the minimum and maximum group delay. In the minimum the group delay is almost 0, whereas in the maximum the delay will be almost 2 FSC's (~ 250 µsec).

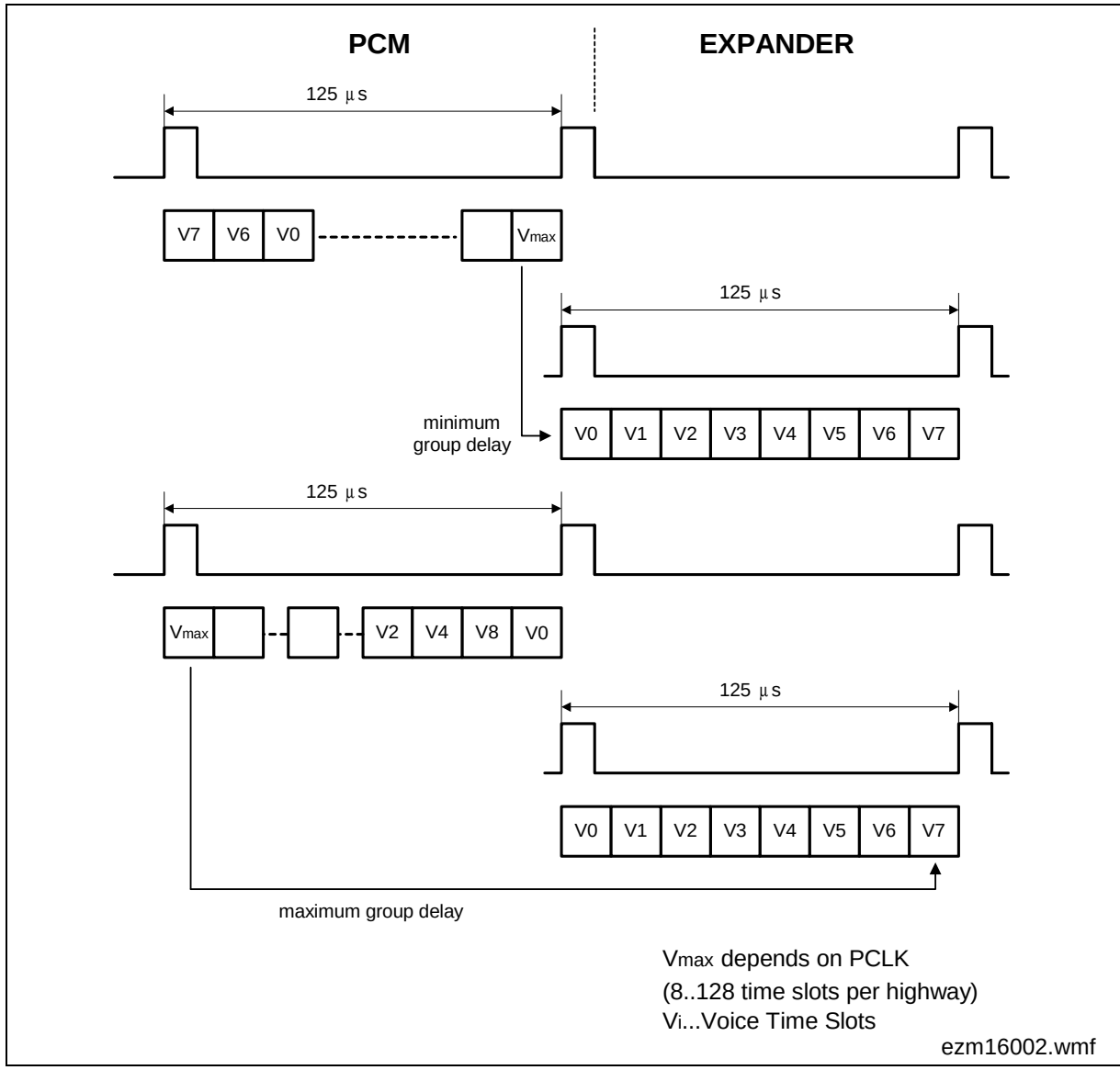


Figure 21 PCM-Group Delay Receive

The group delay of the voice has 1 FSC (in average).

Figure 21 shows the conditions for the minimum and maximum group delay. In the minimum the group delay is almost 0, whereas in the maximum the delay will be almost 2 FSC's (~ 250 µsec).

3.2 µC Interface

The parallel µC-Interface is used to communicate with an external master device and consists of six control lines (ALE/DSQ, CSQ, RDQ/RW, WRQ, DEMUX/MUXQ, INTQ/MOT), 8 bidirectional address/data lines (DIO0 … DIO7) and 8 address-lines (A0 ... A7) and provides fast parallel data transfer to a microcontroller device (Intel compatible and Motorola compatible families).

The µC-Interface of the MuPP µC has a multiplexed / non multiplexed 8-bit address/data bus and allows direct connection to a microcontroller of the Intel 8051-(MCS51/251-) family, the Infineon Technologies C16X-family and Motorola M68HCXX[1)] or M683XX[1)] family without additional components.

Intel / Infineon Technologies family:

Intel multiplexed mode:

MUXQ/DEMUX = 0

INTQ/MOT = 0

INTR active high

With each falling edge of ALE-line the MuPP µC latches the bus data on the 8 data lines DIO0...DIO7 and stores it as an address information. CSQ combined with RDQ or WRQ starts the data transfer cycle via the parallel µC-Interface. If CSQ is low, the data on DIO0...DIO7 will be valid on the rising edge of WRQ/RDQ. Depending on the previously latched address information, these data have a different meaning. In case of a reset command for the µC-Interface the address information 0000 0011 has to be sent together with the data information 1010 1010.

Data transfer to and from the MuSLIC is asynchron and the data will be transferred in bytes.

Intel demultiplexed mode:

MUXQ/DEMUX = 1

INTQ/MOT = 0

INTR active high

In Intel demultiplexed mode, the address- and the data-information is given on separate bus lines A0... A7 and DIO0...DIO7.

Every falling edge of the ALE-line latches the address information. CSQ combined with RDQ or WRQ starts the data transfer cycle in the same way as in the multiplexed mode.

1) Information is preliminary

Motorola demultiplexed mode

MUXQ/DEMUX = X (don’t care)

INTQ/MOT = 1

INTR active low

In Motorola mode address information and data information are given on separate bus lines (A0 ... A7, DIO0 ... DIO7). The address information has to be valid before RDQ/RWQ and ALE/DSQ are indicating a read- or write-cycle. The data information is latched by the rising edge of the ALE/DSQ signal.

Table 6 Possible Address Information to Identify the Following Data Nibbles

Address	Command	Function
00000000, 00H	channel	Preselection of channel for channel specifc commands SOP, TOP, COPI
00000001, 01H	status	Status register to control the read/ write-operations
00000010, 02H	interrupt register (read only)	Indicates channel and sources of pending interrupts
00000011, 03H	reset	Reset of the µC interface by write of data 0AAH to this address
00000100, 04H	reserved	
00000101, 05H	Interrupt Channel Reg. 1	Indication of pending interrupts on channel 0..7
00000110, 06H	Interrupt Channel Reg. 2	Indication of pending interrupts on channel 8..15
00000111, 07H	data	Data port for all register read/write-operations
00001100, 0CH	version register	When read, indicates the version of the MuPP µC device in hexadecimal representation. Value returned by current version = 13H

Status Register

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**CHKSUM_RDY**	**SAMPLE_RDY**	**DU_RDY**	**DD_RDY**

The Status Register controls the data transfer between MuPP and the System via the µC interface.

Note: A read operation of the status register resets all bits which are set at this time.

CHKSUM_RDY Checksum Ready; After start of the checksum generation by the XOP command this bit indicates the status of the checksum generation

CHKSUM_RDY = 0 Checksum generation in progress

CHKSUM_RDY = 1 Checksum generation finished

SAMPLE_RDY[1)] Sample Ready; Indicates that a new sample result is available in SCR4/5. Reading of sample results should be implemented according to flow chart **Figure 22**.

SAMPLE_RDY = 0 No new sample result is available.

SAMPLE_RDY = 1 New sample result is available (Bit SAMPLE_RDY is reset by status register read operation).

DU_RDY Data Upstream Ready; Indicates that valid data are aviable for a read command

DU_RDY = 0 Read data not valid

DU_RDY = 1 Read data valid

DD_RDY Data Downstream Ready; Indicates that a write operation (e. g. broadcast, block transfer) is finished

DD_RDY = 0 Write operation still in progress

DD_RDY = 1 Write operation finished

1) For PEB 31664 this bit has to be ignored

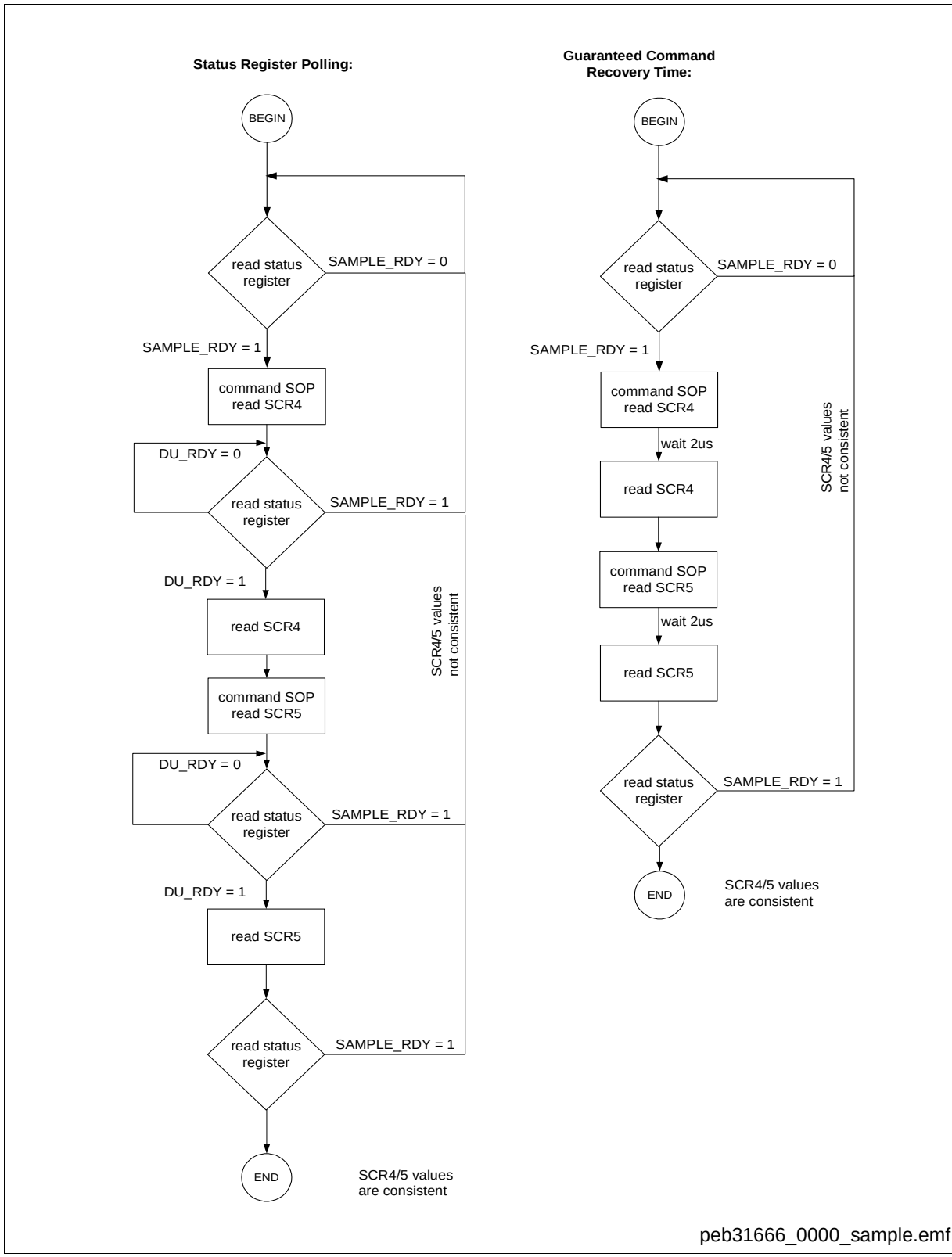


Figure 22 Reading of Sample Results

3.2.1 Interrupt Sequence

Description:

All of the 6 SCR8 bits (QIO2, QIO1, QI1, HOOK, GNK, SLCX) can generate an interrupt. All of the SCR8 bits can be masked to prevent the generation of an interrupt with the Mask-Register (except SLCX).

Behind SLCX there are more additional interrupt bits (described in **Chapter 4.1.3** at **Page 109**). Each of these bits which set the SLCX bit can be masked with the SCR2 register (except the RES bit).

Each of the 16 channel has its own SCR8-register. These registers can be read via the µC-interface (SOP command). The 2 LSB of the SCR8-register are not defined yet.

The interrupt channel registers indicate a pending interrupt in the corresponding channel. All 30 µs one channel will be handled and the corresponding interrupt channel register is set if an interrupt has occured. All 500 µs the interrupt channel registers will be updated. Information of the interrupt channel registers is reset by reading them.

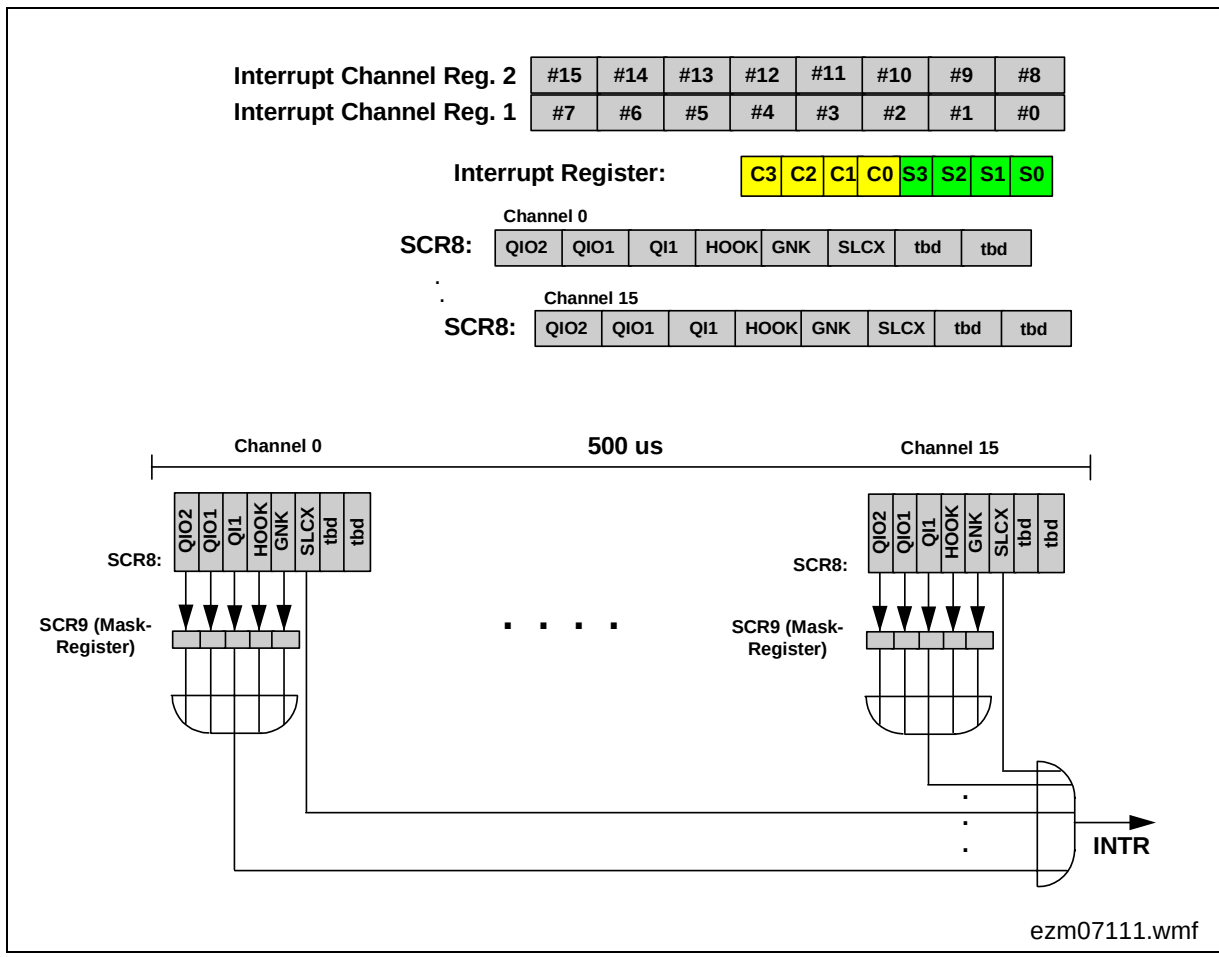


Figure 23 Interrupt Sequence

3.2.2 Interrupt Handling

Simple case: Only one interrupt occurs:

In this case it is very simple to get the IR source. The information is stored in the Interrupt Register. This register contains the channel-number in the 4 MSB and the source in the 4 LSB. Reading this register all information is available. But in the case of SLCX-interrupt the TCR0 register has to be read next to get the additional interrupt source.

- If no interrupt is pending, the interrupt register is responding the value 08h (see "idle (no interrupt)" in **Table 7**).
- Since it is not allowed to interrupt a data command (address 7 read/write) care must be taken, that data port access sequences resulting from normal command operations are not interrupted by access of the interrupt service routine.

Table 7 Interrupt Register

Interrupt Register	C3	C2	C1	C0	S3	S2	S1	S0
Channel 0	0	0	0	0				
.								
.								
.								
Channel 15	1	1	1	1				
	SLCX				0	0	0	0
	GNK				0	0	0	1
	HOOK				0	0	1	0
	QI1				0	0	1	1
	QIO1				0	1	0	0
	QIO2				0	1	0	1
	more than 1 interrupt				0	1	1	1
	more than 1 channel				1	1	1	1
idle (no interrupt)	0	0	0	0	1	0	0	0

Case: More than one interrupt was generated:

If more than one interrupt per channel occurs, the source bits (S3 ... S0) are set to 0111. The channel information in the Interrupt Register is valid and the interrupt source can be read from SCR8.

Interrupts in different channels generate 1111 in the source bits (S3 ... S0). In this case the channel information is not valid, because the Interrupt Register will be updated with each interrupt. In this case all SCR8-Registers must be read.

– General: SLCX-Interrupt:

In the case that one bit of the TCR0-register ist set, all other TCR0-bits cannot be modified as long as the TCR0-register is not read. After reading this register SLCX will be reset to 0 but not before two 8 kHz frames.

3.3 MuPP µC/QAP Interface

The MuPP µC/QAP-Interface, the link between the MuPP µC and the QAP, is a serial interface based on the 6 signals AFSC (analog frame sync), ADCL (analog data clock), ADU1/ADU2 (analog data upstream) and ADD1/ADD2 (analog data downstream). ADU1 and ADD1 are common to the first group of 8 time slots (channels) and ADU2 and ADD2 to the second 8 time slots (channels). AFSC and ADCL are common to both groups of time slots.

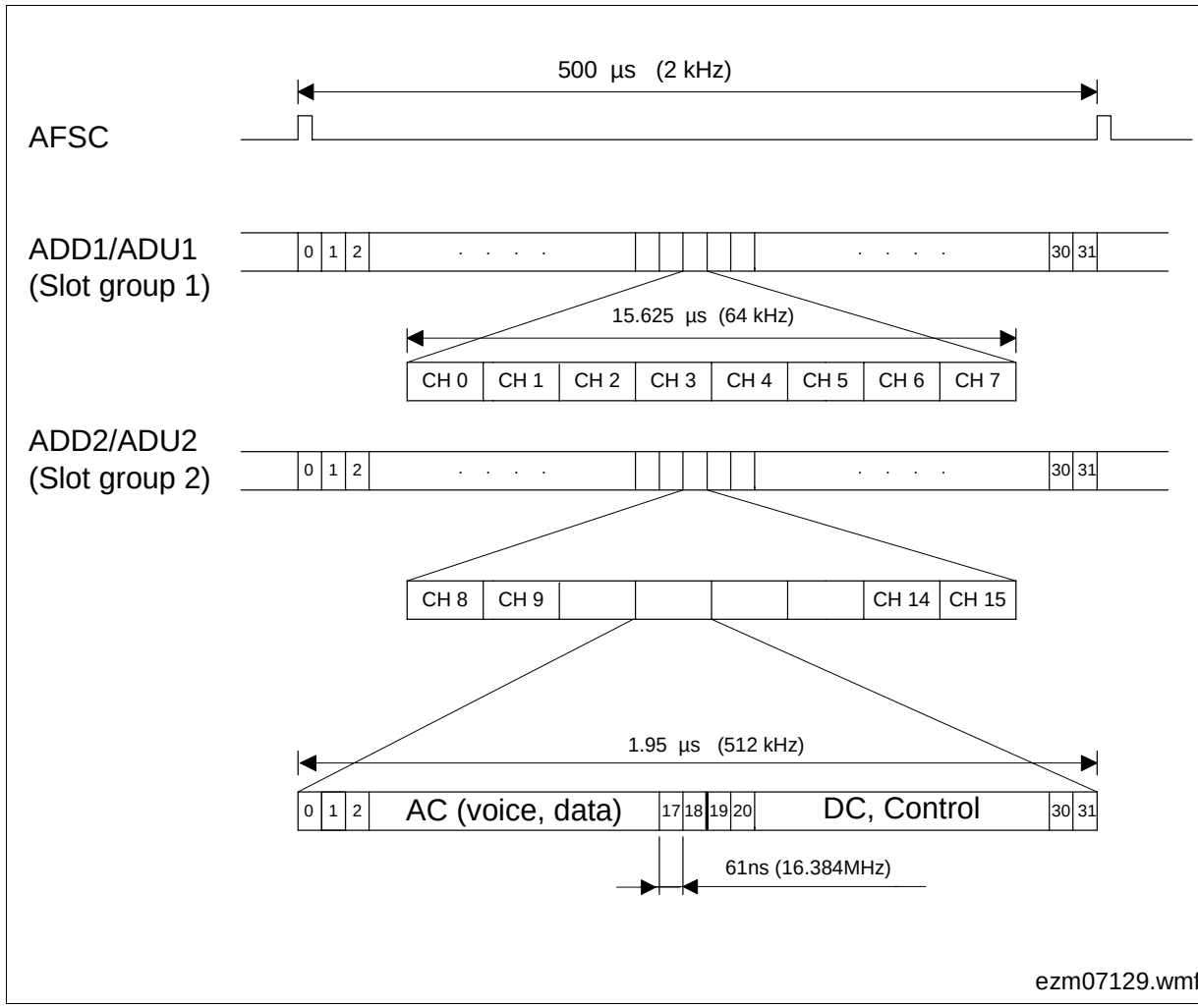


Figure 24 MuPP µC/QAP Interface: Frame, Bit Structure

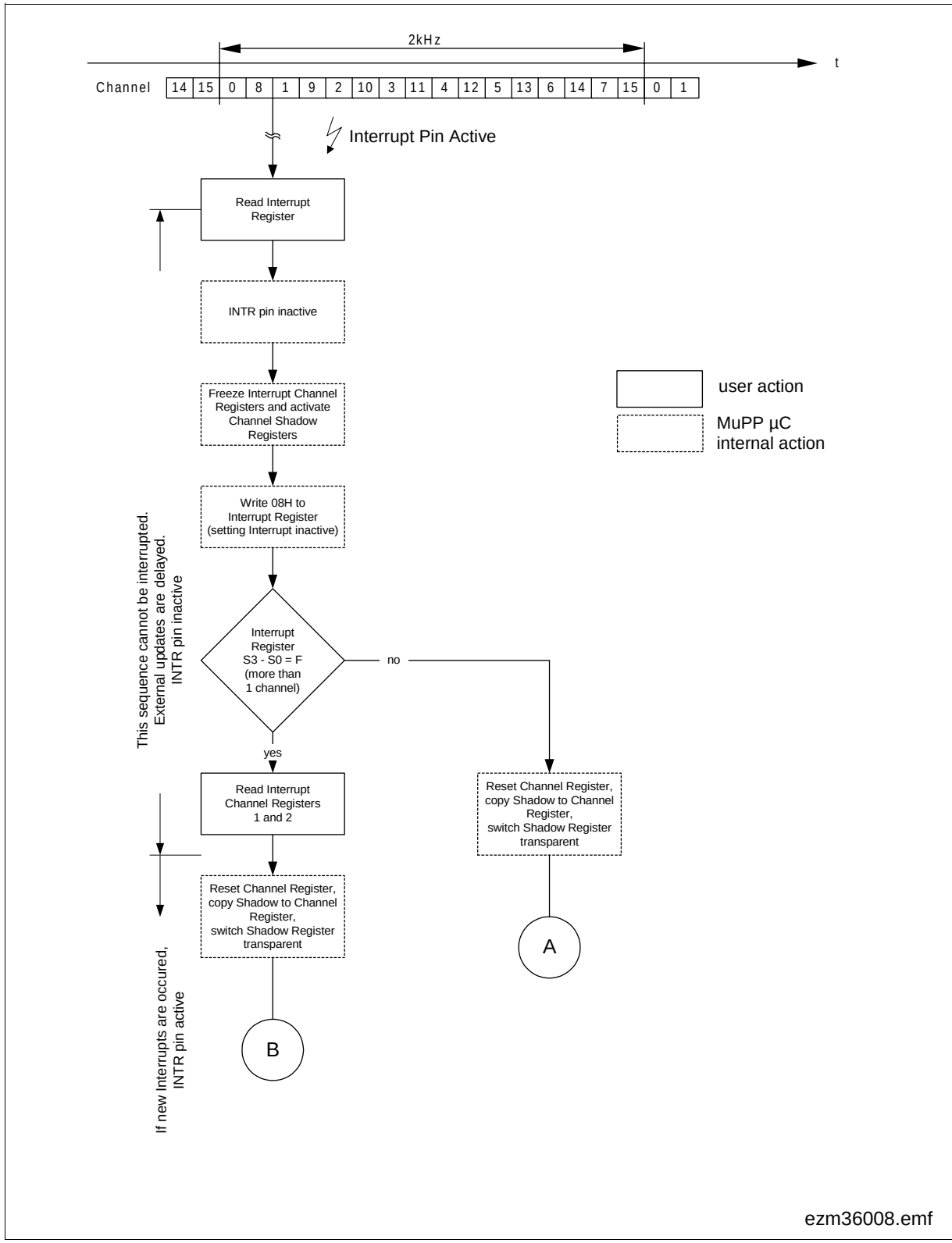


Figure 25 Interrupt Handling (First Step)

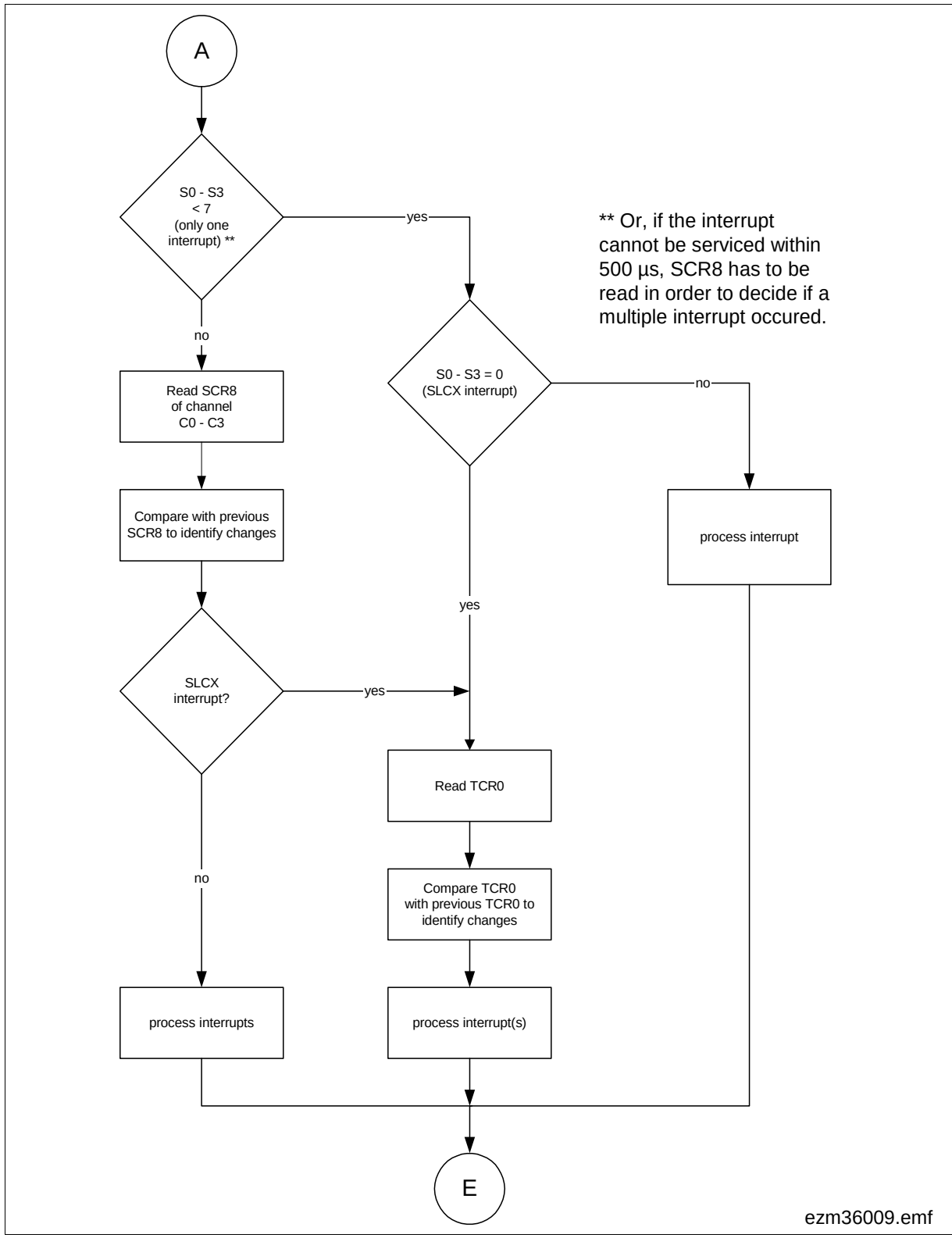


Figure 26 Interrupt Handling (Second Step - Interrupts in one Channel)

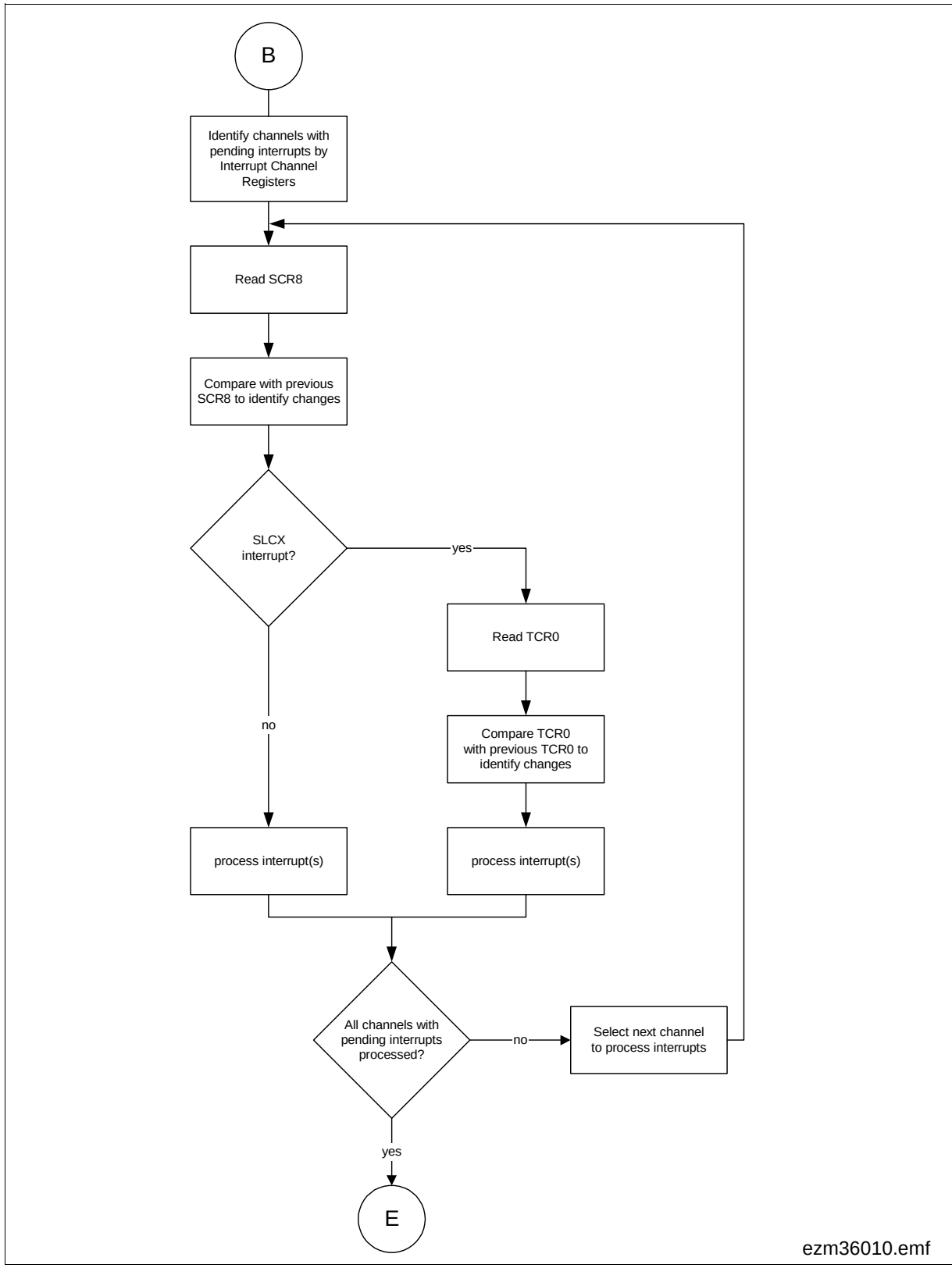


Figure 27 Interrupt Handling (Second Step - Interrupts in two or more channels)

3.4 QAP/AHV-SLIC Interface

Output Voltage AC (ACP, ACN)

The output voltage at the pins ACP and ACN represents the AC-information (including Teletax signal) at the receive path. The AC-information is received via the MuPP µC/QAP-Interface in the ADD channel. The 64-kHz Bitstream is converted to analog, passes a programmable gain stage of 0 / – 3.5 dB (TTX is also affected) and is buffered to drive a load of R_L > 15 kΩ and C_L < 20 pF, which is the input impedance of the AHV-SLIC.

Output Voltage DC (DCP, DCN)

The output voltage at the pins DCP and DCN represents the DC-information together with the Ring Burst at the receive path. The DC-information is received via the MuPP µC/QAP-Interface in the ADD channel. The 2-kHz Bitstream is D/A converted and is lowpass filtered by using two external smoothing capacitors of 2x100 nF. The pins are directly connected to the AHV-SLIC.

Transversal Current Sense AC - Input (ITAC)

The pin ITAC is the input voltage pin for the AC transversal current information from the AHV-SLIC in the transmit path. AC/DC separation is done by an external highpass filter (ext. capacitor = 470 nF). The input resistance is larger than 20 kΩ. Current/voltage conversion is performed via an external resistor of 1.5 kΩ (same for pin IT). The signal passes a programmable gain stage 0, 3.5 or 9.5 dB, is converted to digital and sent to the MuPP µC via the MuPP µC/QAP-Interface in the ADU channel (64-kHz Bitstream).

Transversal Current Sense DC - Input (IT)

The pin IT is the input voltage pin for the DC transversal current information from the AHV-SLIC in the transmit path. The input resistance is larger than 500 kΩ. Current/voltage conversion is done via an external resistor of 1.5 kΩ (same for pin ITAC). The voltage at pin IT is lowpass filtered and converted to digital. The bitstream (2 kHz) is sent to the MuPP µC via the MuPP µC/QAP-Interface for further signal processing.

Longitudinal Current Sense - Input (IL)

The scaled longitudinal current information transferred from the AHV-SLIC - the current/voltage conversion is done by an external resistor of 1.5 kΩ - is converted into digital and sent to the MuPP µC via the MuPP µC/QAP-Interface in the ADU channel. In the MuPP µC the IL-information is lowpass filtered (time programmable using DUPGNK-counter) and reported via the SCR8 (see **Page 82**) if the measured value exceeds a programmed limit. In Power Down, the GNK-bit is set to “0” and the setting of the Interrupt bit (SCR8) caused by GNK is prohibited.

Control Interface (C1, C2, C3)

In order to set the AHV-SLIC to different operating modes, the information of the board controller is passed through from the µC-Interface to the ternary AHV-SLIC interface pins C1, C2 and the binary interface pin C3 (see **Chapter 2.1.3.1**). It is recommended to connect the resp. IO-2 pin of the QAP to drive the resp. C3 pin of the AHV-SLIC (see **Table 3** and **Table 4** in **Chapter 2.1.3.1**).

For signalling “Over temperature” the AHV-SLIC drains a current (I_{OT}) from pin C1. This current is sensed by the PEB 3465 and transferred in the ADU channel to the MuPP µC. The MuPP µC sends the overtemperature message via the SCR8 (SLCX) and TCR0-5 to the µC Interface. This is possible in any operating states of the AHV-SLIC interface except for Power Down.

4 Programming the MuSLIC

With the appropriate commands, the MuSLIC can be programmed by the Microcontroller Interface.

Data transfer to and from the MuSLIC is asynchron and the data will be transferred in bytes.

(For more information, about the µC Interface see **Chapter 3.2**).

4.1 Types of µC Interface Bytes

The µC Interface bytes have to be interpreted as either commands or status information stored in configuration registers or the coefficient RAMs. There are 5 different types of MuSLIC commands which are selected by bit 4 and 5 (partly bit 2 and 3) as shown below.

SOP **STATUS OPERATION:** MuSLIC status setting/monitoring

Bit	7	6	5	4	3	2	1	0
	B	**RW**	**0**	**1**	**LSEL3**	**LSEL2**	**LSEL1**	**LSEL0**

XOP **EXTENDED OPERATION:** General settings

Bit	7	6	5	4	3	2	1	0
	0	**RW**	**1**	**0**	**LSEL3**	**LSEL2**	**LSEL1**	**LSEL0**

TOP **TRANSFER OPERATION:** Read certain status/Options only

Bit	7	6	5	4	3	2	1	0
	0	**R**	**1**	**1**	**0**	**0**	**LSEL1**	**LSEL0**

COP **COEFFICIENT OPERATION:** Filter coefficient setting/monitoring

Bit	7	6	5	4	3	2	1	0
	ICRAM	**RW**	**0**	**0**	**0**	**1**	**WCRAM1**	**WCRAM0**

COPI **COEFFICIENT OPERATION INITIALIZE:** Coefficient set assignment

Bit	7	6	5	4	3	2	1	0
	B	**RW**	**0**	**0**	**1**	**0**	**LSEL1**	**LSEL0**

Table 8 Storage of Programming Information

13 status configuration registers: (for each channel)	SCR0, … SCR10 accessed by SOP command
2 test registers: (for each channel)	STCR0, STCR1 accessed by SOP command
10 extended configuration registers:	XR0 … XR9 accessed by XOP command
19 extended test registers:	XTR0 … XTR18 accessed by XOP command
2 transfer configuration registers: (for each channel)	TCR0, TCR1 accessed by TOP command
AC- and DC-Coefficient RAMs:	CRAMs accessed by COP command
2 coefficient set assignment registers: (for each channel)	CAR0, CAR1 accessed by COPI command

Overview of commands and registers via the µC Interface:

SOP Command

Bit	7	6	5	4	3	2	1	0
SOP for SCR/STCR	B	RW	0	1	LSEL3	LSEL2	LSEL1	LSEL0

SOP Configuration Registers

Bit	7	6	5	4	3	2	1	0
SCR0	POLNR	N/BB	LB	ETG2	ETG1	ENO	ENTE	COR
SCR1	TTXNO	TTX12	NOSL	SOREV	SWDCC	ACT2	QIO2D	QIO1D
SCR2	VB/2M	ICONM	TEMPM	FAILM	MVAM	LSUPM	1	1
SCR3	AG6DB	LIN	LAW	COR8	PCMON	MODEM	USGAIN	AIM
SCR4	LOW Byte of DC-Offset Compensation							
SCR5	HIGH Byte of DC-Offset Compensation							
SCR6A	R-WAY	RS6	RS5	RS4	RS3	RS2	RS1	RS0
SCR6B	R-WAY	RS6	RS5	RS4	RS3	RS2	RS1	RS0
SCR7A	X-WAY	XS6	XS5	XS4	XS3	XS2	XS1	XS0

SCR7B	X-WAY	XS6	XS5	XS4	XS3	XS2	XS1	XS0
SCR8	QIO2	QIO1	QI1	HOOK	GNK	SLCX	0	0
SCR9	QIO2M	QIO1M	QI1M	HOOKM	GNKM	1	1	1
SCR10	QIO2	QIO1	QO1	M2	M1	M0	0	0
STCR0	FUSE3	FUSE2	FUSE1	FUSE0	0	0	0	0
STCR1	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0	0	0

NOTE: = **differences between MuSLIC-E and MuSLIC-S; for details see register description**

XOP Command

Bit	7	6	5	4	3	2	1	0
XOP for XR/XTR	0	RW	1	0	LSEL3	LSEL2	LSEL1	LSEL0

XOP Configuration Registers

Bit	7	6	5	4	3	2	1	0
XR0	MIO4D	MIO3D	MIO2D	MIO1D	MIO4	MIO3	MIO2	MIO1
XR1	DUPGNK				DUP			

XR2	REXTEN	CRSH_A	CRSH_B	FIXC	IDR	EX-MCLK	FIX-CHAN	0
XR3	LOW Byte of AC-CRAM checksum							
XR4	HIGH Byte of AC-CRAM checksum							
XR5	LOW Byte of DC-CRAM checksum							
XR6	HIGH Byte of DC-CRAM checksum							
XR7	ECIC1 (Byte 0 to Byte 14)							
XR8	ECIC2 (Byte 15 to Byte 29)							
XR9	C-MODE	C-S	R-S	DRV_0	Shift	PCM-OFFSET		

XOP Test Register[1]

Bit	7	6	5	4	3	2	1	0
XTR0	HIT	HIR	ELM	SOFTON	OPIM8M	DLP03	DLP5	DISPOFI
XTR1	CAL	LMSEL1	LMSEL0	LMNOTCH	LMBP	LM2PCM	PCM2DC	ITIME
XTR2	RING-ON	DDCC	DCAD16	ERAMP	ERECT	AC-ADCPD	AC-DACPD	AFE-OFF
XTR3	DHP-X	DHP-R	TH	FRX	FRR	AX	AR	IM
XTR4	DLB-8M	DLB-64K	DLB-32K	DLB-PCM	ALB-8M	0	0	DCHOLD
XTR5	DC-DLB	DC-ALBIT	0	DC-ALBIL	DC-ALBV	DCLMU2	DCLMU1	DCLMU0
XTR6	TTXL	GAINBB	NOAGC	ILITMUX	COT16	DITOFF	AXG0	ARG0
XTR7	QDETQ4	QDETQ3	QDETQ2	QDETQ1	0	0	CALMUX1	CALMUX0
XTR8	0	0	0	0	0	0	0	ENRSV
XTR9	0				Fuse 0 QAP 1	Fuse 0 QAP 2	Fuse 0 QAP 3	Fuse 0 QAP 4
XTR10	Fuse 1 QAP 1	Fuse 1 QAP 2	Fuse 1 QAP 3	Fuse 1 QAP 4	Fuse 2 QAP 1	Fuse 2 QAP 2	Fuse 2 QAP 3	Fuse 2 QAP 4
XTR11	Fuse 3 QAP 1	Fuse 3 QAP 2	Fuse 3 QAP 3	Fuse 3 QAP 4	Fuse 4 QAP 1	Fuse 4 QAP 2	Fuse 4 QAP 3	Fuse 4 QAP 4

XTR12	Blocktest 1							
XTR13	Blocktest 2							
XTR14	Blocktest 3							
XTR15	RSV1Q3	RSV1Q2	RSV1Q1	RSV1Q0	RSV2Q3	RSV2Q2	RSV2Q1	RSV2Q0
XTR16	RSV3Q3	RSV3Q2	RSV3Q1	RSV3Q0	RSV4Q3	RSV4Q2	RSV4Q1	RSV4Q0
XTR17	RSV5Q3	RSV5Q2	RSV5Q1	RSV5Q0	RSV6Q3	RSV6Q2	RSV6Q1	RSV6Q0
XTR18	0	0	0	0	0	0	0	0

[1] Come only into effect for specified channel when Bit ENTE (SCRO, Bit1) is set. Therefore, programming the XTR registers with MuPP µC- S is not possible

TOP Command

Bit	7	6	5	4	3	2	1	0
	0	R	1	1	0	0	LSEL1	LSEL0

TOP Configuration Registers

Bit	7	6	5	4	3	2	1	0
TCR0	VB/2	ICON	TEMP	FAIL	MVA	LSUP	RES	0
TCR1	NMVB/2	NMICON	NMTEMP	NMFAIL	NMMVA	NMLSUP	RLM1	RLM0

COP Command

Bit	7	6	5	4	3	2	1	0
	ICRAM	RW	0	0	0	1	WCRAM1	WCRAM0
	SET2	SET1	SET0	CODE4	CODE3	CODE2	CODE1	CODE0

COPI Command

Bit	7	6	5	4	3	2	1	0
	B	RW	0	0	1	0	LSEL1	LSEL0

CAR Coefficient Set Assignment Registers

Bit	7	6	5	4	3	2	1	0
CAR0	DC1	DC0	AC2	AC1	AC0	0	0	HLOAD
CAR1	TG1.2	TG1.1	TG1.0	TG2.2	TG2.1	TG2.0	0	0

4.1.1 SOP Command

To modify or evaluate the MuSLIC status, individually for each channel, the contents of up to 13 configuration registers SCR0, … SCR10 may be transferred to or from the MuSLIC. This is done by a SOP Command (status operation command).

Bit	7	6	5	4	3	2	1	0
	B	**RW**	**0**	**1**	**LSEL3**	**LSEL2**	**LSEL1**	**LSEL0**

B Broadcast

B = 0 Only one channel (time slot) is programmed

B = 1 All channels (up to 16) are programmed with the same information

RW Read/Write Information: enables reading from the MuSLIC or writing information to the MuSLIC

RW = 0 Write to the MuSLIC

RW = 1 Read from the MuSLIC

LSEL Length select information
This field identifies the selected SOP Register(s)

LSEL 3	LSEL 2	LSEL 1	LSEL 0	
0	0	0	0	SCR0
0	0	0	1	SCR1
0	0	1	0	SCR2
0	0	1	1	SCR3[1)]
0	1	0	0	SCR4
0	1	0	1	SCR5
1	0	1	0	SCR6A, SCR6B
1	0	1	1	SCR7A, SCR7B
1	1	0	0	SCR8
1	1	0	1	SCR9
1	1	1	0	SCR10
0	1	1	1	SCR0 to SCR5
1	0	0	0	STCR0
1	0	0	1	STCR1

[1)] The broadcast function for programming all channels with the same information is not available for register SCR3.

SCR0 Configuration Register 0

Configuration register SCR0 defines the basic feeding modes of the MuSLIC and enables/disables test features:

Bit	7	6	5	4	3	2	1	0
	POLNR	**N/BB**	**LB**	**ETG2**	**ETG1**	**ENO**	**ENTE**	**COR**

NOTE: **= different meaning for MuPP µC-S and MuPP µC-E**

Reset value: 00_H

POLNR Normal or Reverse Polarity (see **Chapter 5.4**)
POLNR = 0 Sets the MuSLIC to Normal Polarity feeding
POLNR = 1 Sets the MuSLIC to Reverse Polarity feeding

N/BB MuSLIC-E is in normal or Boosted Battery mode (see **Chapter 5.4**).
For MuSLIC-S this bit has to be set to zero
N/BB = 0 Normal feeding
N/BB = 1 Changes ternary interface to AHV-SLIC which sets the AHV-SLIC to Boosted Battery mode

LB Handling of Loop Back functions for testing PCM loops.
LB = 0 Normal function
LB = 1 PEB 31666: The desired Loop Back function is enabled (selected with XTR4, XTR5); if no loop is selected with XTR4, XTR5 the PCM-Loop is switched on
PEB 31664: PCM-Loop is switched on

ETG2 Enables programmable Test Tone Generator 2
ETG2 = 0 Test Tone Generator 2 is disabled
ETG2 = 1 Test Tone Generator 2 is enabled

ETG1 Enables programmable Test Tone Generator 1
ETG1 = 0 Test Tone Generator 1 is disabled
ETG1 = 1 Test Tone Generator 1 is enabled

ENO MuSLIC-E: Enables Offset compensation
ENO = 0 No DC offset compensation
ENO = 1 DC offset compensation
Note: For MuSLIC-S this bit has to be set to zero

ENTE MuSLIC-E: Enables Test. For MuSLIC-S this bit has to be set to zero.
ENTE = 0 Normal operation
ENTE = 1 Enables the test selected by the test registers (see **Chapter 7**)

COR Cut Off Receive Path for test reasons. This bit cannot be programmed with MuSLIC-S

COR = 0 Receive Path transmission is available

COR = 1 Receive Path is disabled

SCR1 Configuration Register 1

Configuration register SCR1 defines the meterpulse settings and the soft/hard reversal, linear mode and IO settings.

Bit	7	6	5	4	3	2	1	0
	TTXNO	**TTX12**	**NOSL**	**SOREV**	**SWDCC**	**ACT2**	**QIO2D**	**QIO1D**

NOTE: = **different meaning for MuPP µC-S and MuPP µC-E**

Reset value: 00_H

TTXNO MuSLIC-E: Meterpulses are represented by Teletax (TTX) with 12 or 16 kHz or with reverse polarity. For MuSLIC-S this bit has to be set to 1.

TTXNO = 0 Meterpulses are represented with 12 kHz or 16 kHz

TTXNO = 1 Meterpulses are represented with reverse polarity

TTX12 MuSLIC-E: Teletax-signal with 12 kHz or 16 kHz

TTX12 = 0 16 kHz Teletax-signal

TTX12 = 1 12 kHz Teletax-signal

NOSL MuSLIC-E: No slope means that the ramping of Teletax (TTX) signal is switched off

NOSL = 0 Slope of TTX-signal is smooth

NOSL = 1 Hard switch of TTX-Signal

SOREV Soft Reversal Meterpulses

SOREV = 0 Hard reversal

SOREV = 1 Soft reversal

SWDCC Switch DC Characteristic

SWDCC = 0 DC Standard Characteristic

SWDCC = 1 DC Extended Characteristic

ACT2 Active Mode with power save status of AHV-SLIC

ACT2 = 0 Normal mode

ACT2 = 1 C1, C2 indicates the power save mode for the AHV-SLIC In this case the second negative power supply voltage VBAT2 at the AHV-SLIC is used, allows power saving at short lines

QIO1D Direction for programmable IO - pin of the QAP IO1

QIO1D = 0 Sets the pin IO1 as an input

QIO1D = 1 Sets the pin IO1 as an output

QIO2D Direction for programmable IO - pin of the QAP IO2

QIO2D = 0 Sets the pin IO2 as an input

QIO2D = 1 Sets the pin IO2 as an output

SCR2 Configuration Register 2

Configuration register SCR2 is the mask register. Each bit of TCR0 (Signalling register) can be masked (except the RES bit); that means changes of such a 'masked bit' are not causing a change of the SLCX - bit (see **Page 82**, SCR8).

Bit	7	6	5	4	3	2	1	0
	VB/2M	**ICONM**	**TEMPM**	**FAILM**	**MVAM**	**LSUPM**	**1**	**1**

NOTE: **= not defined for MuSLIC-S**

Reset value: FF_H

VB/2M Mask bit for half battery information

VB/2M = 0 Each change of the VB/2 bit leads to an interrupt (SLCX-bit)

VB/2M = 1 Changes of VB/2 bit are neglected

ICONM Mask bit for constant current information

ICONM = 0 Each change of the ICON bit leads to an interrupt (SLCX-bit)

ICONM = 1 Changes of ICON bit are neglected

TEMPM Mask bit for over temperature information

TEMPM = 0 Each change of the TEMP bit leads to an interrupt (SLCX-bit)

TEMPM = 1 Changes of TEMP bit are neglected

FAILM Mask bit for clock fail information

FAILM = 0 Each change of the FAIL bit leads to an interrupt (SLCX-bit)

FAILM = 1 Changes of FAIL bit are neglected

MVAM Mask bit for internal measurement results
MVAM = 0 Each change of the MVA bit leads to an interrupt (SLCX-bit)
MVAM = 1 Changes of the MVA bit are neglected

LSUPM Mask bit for line supervision
LSUPM = 0 Each change of the LSUP bit leads to an interrupt (SLCX-bit)
LSUPM = 1 Changes of the LSUP bit are neglected

Information about changing half battery- and constant current-information will be neglected on both of the Power Down and the Ringing state.

SCR3 Configuration Register 3

Bit	7	6	5	4	3	2	1	0
	AG6DB	**LIN**	**LAW**	**COR8**	**PCMON**	**MODEM**	**USGAIN**	**AIM**

Reset value: 00_H

AG6DB Switch for analog gain in receive and transmit (digitally compensated)
AG6DB = 0 0 dB gain
AG6DB = 1 + 3.5 dB gain in transmit, – 3.5 dB gain in receive

LIN Linear mode selection (16 bit linear information in voice channel A (upper byte) and B (lower byte)
LIN = 0 PCM-mode is selected
LIN = 1 Linear mode is selected

LAW PCM-law selection
LAW = 0 A-Law is selected
LAW = 1 µ-Law is selected (µ255 PCM)

COR8 Cut off receive (voice only)
COR8 = 0 Normal operation
COR8 = 1 Cut off receive is enabled

PCMON After reset PCM-Highway is switched off (tristate)
PCMON = 0 PCM-Off (tristate)
PCMON = 1 PCM-Active

MODEM This bit changes the roll-off frequency behavior in receive direction. Due to a smoother shape of the digital filters higher modem connect rates are possible.

MODEM = 0 Normal operation

MODEM = 1 Change roll-off frequency behaviour (in compliance with ITU-T Q.552)

USGAIN This bit enables an additional analog gain of 6 dB in transmit direction for improved noise performance. The gain is compensated digitally inside the QAP. So there is no coefficient change necessary whether the bit is used or not. Care has to be taken due to the fact that the maximum input level is reduced by a factor of 2 (6 dB). For an overview about the analog gain combinations possible together with QAP V1.2 or higher see **Table 9**.

USGAIN = 0 Normal operation

USGAIN = 1 Additional 6 dB analog gain; bit has to be set in combination with bit AG6DB (register SCR3, bit 7).

AIM This bit enables an analog impedance loop to ensure system stability for input impedances Z_I > 900 Ohms (especially for 1200 Ohms or 900 Ohms + 2.16 µF). The setting of this bit is calculated within the coefficient software MuSLICOS (version higher than V1.2).
(only available together with QAP V1.2 or higher, not available together with QAP V1.1).

AIM = 0 Normal operation

AIM = 1 Switch on analog impedance loop

Table 9 Analog Gain Combinations with QAP V1.2 or higher

Bit USGAIN (SCR3, bit 1)	Bit AG6DB (SCR3, bit 7)	
0	0	Normal operation; 0 dB analog gain
0	1	3.5 dB analog gain in transmit direction – 3.5 dB analog gain in receive direction
1	0	Not used
1	1	9.5 dB analog gain in transmit direction – 3.5 dB analog gain in receive direction

*Note: The broadcast function realised by a SOP command (see **Chapter 4.1.1**) for programming all MuSLIC channels with the same information is not available for register SCR3 when using the PEB 31666 / PEB 31664 V1.3*

SCR4 and SCR5 Configuration Register

These two registers contain the DC offset bytes. They can be used one by one. Activation is controlled by the ENO bit (SCR0-2).

With CAL (XTR1...) levelmeter result can be read from SCR 4/5

SCR4

Bit	7	6	5	4	3	2	1	0
	LOW Byte of DC-Offset Compensation							

NOTE: = not implemented in MuSLIC-S

Reset value: 00_H

SCR5

Bit	7	6	5	4	3	2	1	0
	HIGH Byte of DC-Offset Compensation							

NOTE: = not implemented in MuSLIC-S

Reset value: 00_H

SCR6A Configuration Register 6

Configuration register SCR6A, sets the receiving time slot and the receiving PCM-highway.

Bit	7	6	5	4	3	2	1	0
	R-WAY	**RS6**	**RS5**	**RS4**	**RS3**	**RS2**	**RS1**	**RS0**

Reset Value: 00_H

R-WAY Selects the PCM-highway for the receiving of PCM-data

R-WAY = 0: PCM-highway A is selected

R-WAY = 1: PCM-highway B is selected

RS[6:0] Selects the time slot (0 to 127) used for receiving the PCM-data

The time slot-number is binary coded.

0 0 0 0 0 0 0: Time slot 0 is selected

0 0 0 0 0 0 1: Time slot 1 is selected

....

1 1 1 1 1 1 0: Time slot 126 is selected

1 1 1 1 1 1 1: Time slot 127 is selected

In case of 16 bit linear mode time slot and PCM-highway for the most significant byte is selected.

SCR6B Configuration Register 6

Configuration register SCR6B, sets the receiving time slot and the receiving PCM-highway in case of 16 bit linear mode for the least significant byte.

Bit	7	6	5	4	3	2	1	0
	R-WAY	**RS6**	**RS5**	**RS4**	**RS3**	**RS2**	**RS1**	**RS0**

Reset Value: 00_H

R-WAY Selects the PCM-highway for receiving of linear data

R-WAY = 0: PCM-highway A is selected

R-WAY = 1: PCM-highway B is selected

RS[6:0] Selects the time slot (0 to 127) used for receiving linear data

The time slot-number is binary coded.

0 0 0 0 0 0 0: Time slot 0 is selected

0 0 0 0 0 0 1: Time slot 1 is selected

....

1 1 1 1 1 1 0: Time slot 126 is selected

1 1 1 1 1 1 1: Time slot 127 is selected

SCR7A Configuration Register 7

Configuration register SCR7A, sets the transmit time slot and the transmit PCM-highway.

Bit	7	6	5	4	3	2	1	0
	X-WAY	**XS6**	**XS5**	**XS4**	**XS3**	**XS2**	**XS1**	**XS0**

Reset Value: 00_H

X-WAY Selects the PCM-highway for transmitting PCM-data

X-WAY = 0: PCM-highway A is selected

X-WAY = 1: PCM-highway B is selected

XS[6:0] Selects the time slot (0 to 127) used for transmitting the PCM-data

The time slot-number is binary coded.

0 0 0 0 0 0 0: Time slot 0 is selected

0 0 0 0 0 0 1: Time slot 1 is selected

....

1 1 1 1 1 1 0: Time slot 126 is selected

1 1 1 1 1 1 1: Time slot 127 is selected

In case of 16 bit linear mode time slot and PCM-highway for the most significant byte is selected.

Note: While programing the transmit time slot assignment, the PCM-highway needs to be switched off for the respective channel (PCMON=1, bit 3 of SCR3).

SCR7B Configuration Register 7

Configuration register SCR7B, sets the transmit time slot and the transmit PCM-highway in case of 16 bit linear mode for the least significant byte.

Bit	7	6	5	4	3	2	1	0
	X-WAY	**XS6**	**XS5**	**XS4**	**XS3**	**XS2**	**XS1**	**XS0**

Reset Value: 00_H

X-WAY Selects the PCM-highway for transmitting linear data

X-WAY = 0: PCM-highway A is selected

X-WAY = 1: PCM-highway B is selected

XS[6:0] Selects the time slot (0 to 127) used for transmitting linear data

The time slot-number is binary coded.

0 0 0 0 0 0 0: Time slot 0 is selected

0 0 0 0 0 0 1: Time slot 1 is selected

....

1 1 1 1 1 1 0: Time slot 126 is selected

1 1 1 1 1 1 1: Time slot 127 is selected

SCR8 Configuration Register 8

Configuration Register SCR8 supplies the most important and time critical informations from the MuSLIC. This register is read only.

Bit	7	6	5	4	3	2	1	0
	QIO2	**QIO1**	**QI1**	**HOOK**	**GNK**	**SLCX**	**0**	**0**

Reset Value: 00_H

SLCX Interrupt bit: Summary output of the whole signalling register (TCR0).
- SLCX = 0 No unmasked bit in the signalling register has toggled.
- SLCX = 1 Any unmasked bit in the signalling register has toggled.

GNK Indication if a ground connection is detected (filtered via the DUPGNK-counter). The function is disabled in Power Down State (GNK is set to 0).
- GNK = 0 No ground connection was detected.
- GNK = 1 Ground connection was detected.

HOOK Indication of the loop condition (filtered via the DUP-counter or 2 x DUP-counter in Power Down State).
- HOOK = 0 Subscriber is On-hook.
- HOOK = 1 Subscriber is Off-hook.

QI1 Logical state of the input pin I1 of the QAP.
- QI1 = 0 The corresponding pin at the digital interface of the QAP is receiving a logic 0.
- QI1 = 1 The corresponding pin at the digital interface of the QAP is receiving a logic 1.

QIO1 Logical state of the programmable input/output pin IO1 of the QAP - even if not programmed as an input pin.[1)]
- QIO1 = 0 The corresponding pin at the digital interface of the QAP is receiving a logic 0.
- QIO1 = 1 The corresponding pin at the digital interface of the QAP is receiving a logic 1.

QIO2 Logical state of the programmable input/output pin IO2 of the QAP - even if not programmed as an input pin.[1)]
- QIO2 = 0 The corresponding pin at the digital interface of the QAP is receiving a logic 0.
- QIO2 = 1 The corresponding pin at the digital interface of the QAP is receiving a logic 1.

1) If the input/output pin is programmed as an output the corresponding bit in the SCR8 register is "1".

The DUP- (DUPGNDK-) counters filter the status-information and the input I1. The counters count down and generate enable signals for the registers if they are zero. Then they start counting again at the programmed value. If a status information or the input signal changes the proper counter is set and continues counting down. There is one DUP counter for VB/2, ICON, LSUP (generating SLCX), the input pin I1 and for HOOK. For filtering the GNK information there is the DUPGNK counter.

In case of a mode change:

1. The actual status of HOOK is fixed and the actual HOOK counter is set
2. The DUP- and DUPGNK-counters are load with the double of the programmed value to avoid any influence of transients
3. In Power down mode the counters are always load with the double of the programmed value

SCR9 Configuration Register 9

Interrupt Mask Register

Bit	7	6	5	4	3	2	1	0
	QIO2M	**QIO1M**	**QI1M**	**HOOKM**	**GNKM**	**1**	**1**	**1**

Reset Value: FF_H

QIO2M

QIO2M = 0	Each change leads to an interrupt
QIO2M = 1	Changes are neglected

QIO1M

QIO1M = 0	Each change leads to an interrupt
QIO1M = 1	Changes are neglected

QI1M

QI1M = 0	Each change leads to an interrupt
QI1M = 1	Changes are neglected

HOOKM

HOOKM = 0	Each change leads to an interrupt
HOOKM = 1	Changes are neglected

GNKM

GNKM = 0	Each change leads to an interrupt
GNKM = 1	Changes are neglected

SCR10 Configuration Register 10

Configuration Register SCR10 covers selection of operating modes for the MuSLIC and sets the values for output pins of the QAP.

Bit	7	6	5	4	3	2	1	0
	QIO2	**QIO1**	**QO1**	**M2**	**M1**	**M0**	**0**	**0**

Reset Value: 00_H

M0, M1, M2 These bits define the mode selection for the MuSLIC; see table below for details see **Chapter 5**)

M2	M1	M0	Description
0	0	0	Power-Down High Impedance (loop open, PDN
1	1	1	Power-Down Resistive (loop open, PDNR)
0	1	0	Active State
1	1	0	Active State with Meterpulses
1	0	0	Ground Start
0	0	1	Ringing State (ring pause)
1	0	1	Ringing State (ring burst on)

Note: In external ringing mode (REXTEN, XR2-7 = 1) when ring burst on (RBO) is detected, the output pin IO1 of the QAP is low active to drive directly the ring relay.

QO1 Value for the fixed output pin O1 of the QAP.

QO1 = 0 The corresponding pin at the digital interface of the QAP is set to a logic 0.

QO1 = 1 The corresponding pin at the digital interface of the QAP is set to a logic 1.

Note: The Output pin O1 of the QAP is tristate after reset and will be enabled by the first SOP command.

QIO1 Value for the programmable input/output pin IO1 of the QAP if programmed as an output pin. If the bit REXTEN (XR2-7) is set to 1 (external ringing) the internally created Ring Burst On Signal (for an external relay driver) is fed to QIO1 (**Chapter 5.5**)

QIO1 = 0 The corresponding pin at the digital interface of the QAP is set to a logic 0.

QIO1 = 1 The corresponding pin at the digital interface of the QAP is set to a logic 1.

QIO2 Value for the programmable input/output pin IO2 of the QAP if programmed as an output pin.

QIO2 = 0 The corresponding pin at the digital interface of the QAP is set to a logic 0.

QIO2 = 1 The corresponding pin at the digital interface of the QAP is set to a logic 1.

STCR0 Test Configuration Register 0

The Test Configuration register STCR0 is used for fuse operation and test only.

Bit	7	6	5	4	3	2	1	0
	FUSE3	**FUSE2**	**FUSE1**	**FUSE0**	**0**	**0**	**0**	**0**

Reset value: 00_H

FUSE0 to FUSE3 Information for fuse operation

STCR1 Test Configuration Register 1

The Test Configuration register STCR1 is used for reserved operations of the PEB 3465 (QAP).

Bit	7	6	5	4	3	2	1	0
	RSV5	**RSV4**	**RSV3**	**RSV2**	**RSV1**	**RSV0**	**0**	**0**

Reset value: 00_H

RSV0 Out of Band AC-DAC

RSV0 = 0 Corner Frequency of ac-dac = 31 kHz

RSV0 = 1 Corner Frequency of ac-dac = 15 kHz

Note: This bit come only into effect if bit ENRSV (XTR8, bit0) is set to 1

RSV1 to RSV5 From PEB 31666 to PEB 3465

4.1.2 XOP Command

To modify or evaluate test configurations, to select special functions, to control the coefficient RAMs, to get information for fusing and ECIC and other common functions up to 15 Bytes maybe transferred to or from the MuSLIC, using the XOP Command (extended operation command).

Bit	7	6	5	4	3	2	1	0
	0	**RW**	**1**	**0**	**LSEL3**	**LSEL2**	**LSEL1**	**LSEL0**

RW Read/Write Information: enables reading from the MuSLIC or writing information to the MuSLIC

RW = 0 Write to the MuSLIC

RW = 1 Read from the MuSLIC

LSEL Length select information.

This field identifies the subsequent data byte(s).

LSEL3	LSEL 2	LSEL 1	LSEL 0	
0	0	0	0	XR0
0	0	0	1	XR1
0	0	1	0	XR2
0	0	1	1	XR3-XR6: AC-RAM + DC-RAM checksum
0	1	0	0	XR3-XR4: AC-RAM checksum
0	1	0	1	XR5-XR6: DC-RAM checksum
0	1	1	0	XR7: ECIC1 (0 to 14)
0	1	1	1	XR8: ECIC2 (15 to 29)
1	1	1	0	XR9
1	0	0	0	XTR0
1	0	0	1	XTR1 and XTR2
1	0	1	0	XTR0 to XTR8
1	0	1	1	Fuse register 0 to fuse register 2
1	1	0	0	Blocktest 1 to blocktest 3
1	1	0	1	XTR15 to XTR18
1	1	1	1	RESERVED

XR0 Extended Operation Register 0

Extended Operation Register 0 defines the four IO-pins of the MuPPµC.

Bit	7	6	5	4	3	2	1	0
	MIO4D	**MIO3D**	**MIO2D**	**MIO1D**	**MIO4**	**MIO3**	**MIO2**	**MIO1**

Reset value: 00_H

MIOiD Direction for programmable IO - pins of the MuPP µC IO1 to IO4
MIOiD = 0 Sets the pin IOi as an input
MIOiD = 1 Sets the pin IOi as an output

MIOi Value of programmable IO - pins of the MuPP µC IO1 to IO4
MIOi = 0 Sets the pin IOi to LOW or if it is read it is LOW
MIOi = 1 Sets the pin IOi to HIGH or if it is read it is HIGH

If the bit REXTEN (XR2-7) is set to 1 (Unbalanced Ringing) the IO1 pin of the MuPP µC is switched to the ring pulse control function. Thus a zero-crossing signal connected to the IO1 (combined with the Ringing Mode, burst on/off) generates a correct switching signal for the ringer relay sent on I/O1-A...D (QAP) of the selected subscriber line (see **Page 82**, **Page 84** and **Chapter 5.5**).

If the bit EX-MCLK (XR2-2) and TST1 pin (No.32) are set to 1 and the IO2 pin is set as an input the MuPP µC is ready for external clocking (32.768 MHz) (the internal PLL is shut down).

If the TST1 pin (No.32) and the bit EX-MCLK (XR2-2) is set to 1 and the IO2 pin is set as an output the 32.768 MHz clock (output of the internal PLL) is fed to the IO2 pin.

XR1 Extended Operation Register 1

Extended Operation Register 1 defines the Data Upstream Persistency Counters.

Bit	7	6	5	4	3	2	1	0
	DUPGNK				DUP			

Reset value: 49_H

DUPGNK To restrict the rate of upstream SCR8-bit changes, deglitching (persistence checking) of the status information from the MuSLIC may be applied. New status information will be transmitted upstream, after it has been stable for N milliseconds. N is binary programmable in the range of 4 to 64 ms in steps of 4 ms, with DUPGNK = 0_H the deglitching time is 4ms.

Reset value is 20 ms.

The GNK bit is influenced.

(Detailed info see SCR8, **Page 82** and **Figure 29**.)

DUP To restrict the rate of upstream SCR8-bit changes, deglitching (persistence checking) of the status information from the MuSLIC may be applied. New status information will be transmitted upstream, after it has been stable for N milliseconds. N is binary programmable in the range of 1 to 16 ms in steps of 1 ms; with DUP = 0_H the deglitching time is 1ms.

Reset value is 10 ms.

The HOOK, SLCX and the QI1-bits are influenced (different counters but same programming).

(Detailed info see SCR8, **Page 82** and **Figure 29**.)

XR2 Extended Operation Register 2

Extended Operation Register 2 defines basic operations for all channels.

Bit	7	6	5	4	3	2	1	0
	REXTEN	**CRSH_A**	**CRSH_B**	**FIXC**	**IDR**	**EX-MCLK**	**FIX-CHAN**	**0**

Reset value: 14_H

REXTEN External Ringing Mode Enabled (see **Chapter 5.5**)
REXTEN = 0 Use internal ringing mode
REXTEN = 1 Use external ringing mode[1)]

CRSH_A Crash[2)] on PCM-highway A (line DXA)
CRSH_A = 0 No crash detected
CRSH_A = 1 Crash detected (bad programming in SCR7A/B-registers)

CRSH_B Crash on PCM-highway B (line DXB)
CRSH_B = 0 No crash detected
CRSH_B = 1 Crash detected (bad programming in SCR7A/B-registers)

FIXC The MuSLIC uses either fixed coefficients or the programmed ones.
FIXC = 0 Programmed coefficients used
FIXC = 1 Fixed coefficients used

IDR Initializes Data RAM
IDR = 0 Normal operation is selected
IDR = 1 Content of Data RAM is set to 0 (for test purposes)

EX-MCLK Possibility to provide the MuSLIC with an external clock (see XR0)
EX-MCLK = 0 Normal operation is selected
EX-MCLK = 1 If the TST1 pin (No. 32) is set to 1 the internal PLL is shut down or internal clock is connected to the pin MIO2, respectively (see XR0)

FIX-CHAN Selection between set programming and channel specific CRAM coefficients (only for AC- and TG-coefficients)
FIX-CHAN = 0 Programming and mapping for the AC/TG-CRAM coefficients will be done in the normal way (COP command, channel mapping by CAR registers)

FIX-CHAN = 1 Each channel can be programmed with his own AC/TG-CRAM coefficients. COP command will be handled as a SOP command (channel specific). CAR0, CAR1 has to be programmed as usual. The mapping for the DC coefficients will be used as programmed but the mapping for the AC/TG CRAM Coefficients will be set to a fixed order.

1) With MuSLIC-S this Bit has to be set to 1 since internal ringing is not supported

2) A crash occurs, if 2 or more channels are programed to transmit (talk) in the same time slot on the same highway. In this case the crash-bit will be set, and transmission will be disabled for all affected channels.

The bit FIX-CHAN switches between set programming and channel specific programming for the AC and TG coefficients. In the channel specific programming mode each channel has its own AC and TG coefficients. If FIX-CHAN is set to 1, programming of the AC and TG CRAM coefficients can be done for 16 channels individually, but the mapping to the channels will be done in a fixed order. The DC coefficients will not be affected.

XR3 TO XR6 Extended Operation Registers 3 to 6

XR3 to XR6 are the checksums of all the coefficient bytes written into the Coefficient RAM (CRAM) of the MuPP µC by the COP-Command. Reading these bytes starts the sum generation. There are two identical blocks of CRAMs (channels 0 to 7 and 8 to 15). Each reading alternates the block access.

XR3

Bit	7	6	5	4	3	2	1	0
	LOW Byte of AC-CRAM-checksum							

XR4

Bit	7	6	5	4	3	2	1	0
	HIGH Byte of AC-CRAM-checksum							

XR5

Bit	7	6	5	4	3	2	1	0
	LOW Byte of DC-CRAM-checksum							

XR6

Bit	7	6	5	4	3	2	1	0
	HIGH Byte of DC-CRAM-checksum							

(Algorithm of defining the checksum: $x^{16} + x^{10} + x^7 + x + 1$)

(With that algorithm you can reach a fault coverage of: $1\text{-}2^{-16}$)

Sum generation is done in the following manner.

AC-CRAM-Checksum

The sequence of the coefficients is:

TG1 TG2	set7
TG1 TG2	set6
...	...
TG1 TG2	set0
TGCSF	
IM1 IM2 IM3 TH1 TH2 TH3 FRX FRR TSTAC AX AR ACCSF	set7
IM1 ... ACCSF	set6
...	...
IM1 ... ACCSF	set0

DC-RAM-Checksum

The sequence of the coefficients is:

TSTTX LPF HOOKL RAMP TSTDC TTX AGC DC RING DCCSF	set3
TSTTX ... DCCSF	set2
TSTTX ... DCCSF	set1
TSTTX ... DCCSF	set0

Using the “checksum fill” Bytes (TGCSF, ACCSF, DCCSF) it is possible to create a fixed set-checksum independent of changed coefficients.

Checksum

To calculate the CRAM checksum the following shift register is implemented.

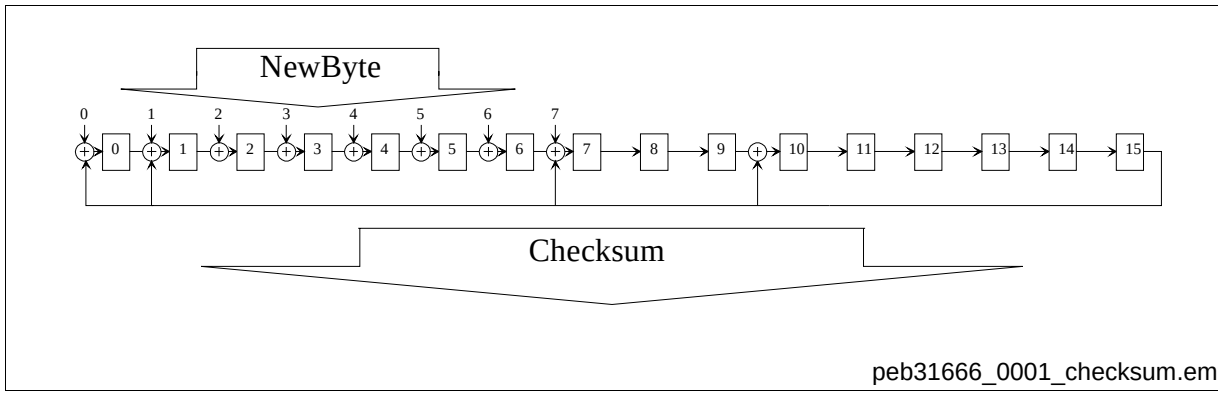


Figure 28 Checksum

Algorithm:

```
unsigned int Checksum, NewByte;
for (i=1;i<BytesPerSet;i++){
if (Checksum >= 0x8000)              // If MSB = 1 -> evaluate checksum with polynom
        Checksum = (((Checksum<<1)^NewByte)&0xffff)^0x0483;
else
        Checksum = (((Checksum<<1)^ NewByte)&0xffff);
}
```

The fillbytes can be used to get a predefined checksum. The following example is given to get the checksum 0x0000 after every set. This is very useful since the sets can be changed without interfering and changing the complete checksum over all sets.

1. calculate the checksum until 1 byte before the 8 fillbytes
   (NOTE: In order to calculate the fill bytes you should take into account that there is a need to have 9 bytes available in order to set a calculated checksum back to 0x0000. The ninth respectively the first byte is located within the CRAM at the following positions:
   AC-Fill bytes:
   Within AR-Filter-Coefficients nibble 14/15.
   DC-Fill bytes:
   Within DC-Test-Coefficients (TSTDC) nibble 14/15.
   TG-Fill bytes:
   Within TG2/Set0 nibble 14/15.

2. the next steps are to feed in 9 bytes that “zero out” after the XOR feedbacks the result of the checksum

Algorithm:

```
for (i = 1;i < 10;i++){
    // take FillByte out of checksum:
    FillByte = (Checksum<<1) & 0xff;

    // If MSB = 1 Checksum is evaluated with polynom
    if ((Checksum & 0x8000) == 0x8000)  FillByte = FillByte ^ 0x83;

    // If MSB = 0 Checksum no feedback
    if ((Checksum & 0x1000) == 0x1000)  FillByte = FillByte ^ 0x80;

    // calculate new Checksum with FillByte
    if (Checksum >= 0x8000)
            Checksum = (((Checksum<<1)^ FillByte)&0xffff)^0x0483;
    else
            Checksum = (((Checksum<<1)^ FillByte)&0xffff);
}
```

XR7 and XR8 Extended Operation Register 7 to 8

Each of these two registers feasibles to read 15 bytes of design/status information generated by an external ASIC.

XR7

Bit	7	6	5	4	3	2	1	0
	ECIC1 (Byte 0 to Byte 14)							

XR8

Bit	7	6	5	4	3	2	1	0
	ECIC2 (Byte 15 to Byte 29)							

XR7 and XR8 shows the data stream of the input pin ID0. If the input pins ID1, ID2 and ID3 = 1, ID0 works as a serial input controlled by EFSC and MCLK.

Note: Valid data is available two EFSC-periods after execution of the ECIC-read command (XOP command).

XR9 Extended Register 9

This register configures the operation of the PCM-interface

Bit	7	6	5	4	3	2	1	0
	C-MODE	**C-S**	**R-S**	**DRV_0**	**Shift**	**PCM-OFFSET**		

Reset value: 00_H

C-MODE Defines the CLK-mode for the PCM-interface

C-Mode = 0: Single clocking is used

C-Mode = 1: Double clocking is used

C-S Transmit Slope

X-S = 0: Transmission starts with rising edge

X-S = 1: Transmission starts with falling edge

R-S Receive Slope

R-S= 0: Data is sampled with falling edge of PCLK

R-S= 1: Data is sampled with rising edge of PCLK

DRV_0 Driving Mode for Bit 0 (only available with single clocking mode)

DRV_0 = 0: Bit 0 is driven the whole PCLK-period

DRV_0 = 1: Bit 0 is driven during the first half of the PCLK-period only

Shift Shifts the access to DXA/B and DRA/B for one PCLK-period

(only available with double clocking mode)

Shift = 0: No shift takes place

Shift = 1: Access to DXA/B and DRA/B is shifted for one PCLK-per.

PCM-OFFSET Offset in number of data-clock periods added to time slot

0 0 0: No offset is added

0 0 1: One data clock period is added

...

1 1 1 Seven data clock periods are added

XTR0 Extended Operation Test Register 0[1)]

Extended Operation Test Register XTR0 defines testing features.

Bit	7	6	5	4	3	2	1	0
	HIT	**HIR**	**ELM**	**SOFTON**	**OPIM8M**	**DLP03**	**DLP5**	**DISPOFI**

Reset value: 00_H

HIT For AHV-SLIC test functions
- HIT = 0 Normal operation
- HIT = 1 Changes AHV-SLIC-interface (C1,C2) which set the TIP wire to high impedance

HIR For AHV-SLIC test functions
- HIR = 0 Normal operation
- HIR= 1 Changes AHV-SLIC-interface (C1,C2) which set the RING wire to high impedance

ELM Enable level meter
- ELM = 0 Normal operation, if LM2PCM = 1 the input to the levelmeter is switched to PCM voice-channel
- ELM = 1 Level meter function is enabled, if LM2PCM = 1 the output of the levelmeter is switched to PCM voice-channel

SOFTON SW-fuses are activated in the PEB 3465
- SOFTON = 0 HW-fuses are activated
- SOFTON = 1 SW-fuses are activated

OPIM8M Open fast digital Impedance Matching Loop (IM8M)
- OPIM8M = 0 Normal operation
- OPIM8M = 1 Opens fast digital IM-Loop ($H_{IM8M} = 0$)

DLP03 Disable LP03-lowpass
- DLP03 = 0 Normal operation
- DLP03 = 1 Disables programmable lowpass ($H_{LP03} = 1$)

DLP5 Disable LP5-lowpass
- DLP5 = 0 Normal operation
- DLP5 = 1 Disables programmable lowpass ($H_{LP5} = 1$)

DISPOFI Disable Postfilter (DC path)
- DISPOFI = 0 Normal operation
- DISPOFI = 1 Disables postfilter

1) The XTR-Registers are not available with the MuSLIC-S

XTR1 Extended Operation Test Register 1

XTR1 controls the level meter functions

Bit	7	6	5	4	3	2	1	0
	CAL	**LMSEL1**	**LMSEL0**	**LMNOTCH**	**LMBP**	**LM2PCM**	**PCM2DC**	**ITIME**

Reset value: 00_H

CAL Enable levelmeter result register

- CAL = 0 Normal operation (offset register - SCR4/SCR5 - is read)
- CAL = 1 Levelmeter result register is read

LMSEL Selects levelmeter and thresholdpairs

LMSEL1	LMSEL0	
0	0	DC-levelmeter thresholdpair 0
0	1	DC-levelmeter thresholdpair 1
1	0	AC-levelmeter
1	1	TTX-levelmeter

LMNOTCH Bandpass or notchfilter function for levelmetering AC

- LMNOTCH = 0 Bandpass function
- LMNOTCH = 1 Notchfilter function

LMBP Activates the bandpass or notchfilter in the AC transmit path

- LMBP = 0 Normal operation
- LMBP = 1 Bandpass/notchfilter enabled

LM2PCM Switches the selected levelmeter signal to the PCM voice-channel

- LM2PCM = 0 Normal operation
- LM2PCM = 1 Switches the selected levelmetersignal to the PCM voice-channel

PCM2DC switches the receive PCM voice-channel to DC-output

- PCM2DC = 0 Normal operation
- PCM2DC = 1 Switches the receive PCM voice-channel to DC-output

ITIME Integration time of AC and TTX levelmeter

- ITIME = 0 16 ms integration time
- ITIME = 1 256 ms integration time

XTR2 Extended Operation Test Register 2

Extended Operation Test Register XTR2 defines testing features (see **Chapter 7**).

Bit	7	6	5	4	3	2	1	0
	RING-ON	**DDCC**	**DCAD16**	**ERAMP**	**ERECT**	**AC-ADCPD**	**AC-DACPD**	**AFE-OFF**

Reset value: 00_H

RING-ON Interrupt DC-characteristic and enables the ringing offset
- RING-ON = 0 Normal operation
- RING-ON = 1 Opens DC-loop (HDCC = 0) and enables the ringing offset

DDCC Disable DC-characteristic
- DDCC = 0 Normal operation
- DDCC = 1 Bridges DC-loop (H_{DCC} = 1)

DCAD16 DC gain of 16 in AD direction
- DCAD16 = 0 Normal operation
- DCAD16 = 1 Gain of 16

ERAMP Enable ramping generator
- ERAMP = 0 Ramping generator off
- ERAMP = 1 Ramping generator on

ERECT Enable rectifier in DC-levelmeter
- ERECT = 0 Normal operation (HRECT = 1)
- ERECT = 1 Enables rectifier

AC-ADCPD ADC is set to power down (transmit path is opened)
- AC-ADCPD = 0 Normal operation
- AC-ADCPD = 1 Transmit path is inactive

AC-DACPD DAC is set to power down (receive path is opened)
- AC-DACPD = 0 Normal operation
- AC-DACPD = 1 Receive path is inactive

AFE-OFF Analog front end is activated or deactivated
- AFE-OFF = 0 Normal operation
- AFE-OFF = 1 The analog front end is deactivated

XTR3 Extended Operation Test Register 3

Extended Operation Test Register XTR3 defines the basic MuSLIC settings which enable / disable the programmable digital filters.

Bit	7	6	5	4	3	2	1	0
	DHP-X	**DHP-R**	**TH**	**FRX**	**FRR**	**AX**	**AR**	**IM**

Reset value: 00_H

DHP-X Disable transmit highpass for test reasons
- DHP-X = 0 Transmit highpass filter is enabled
- DHP-X = 1 Transmit highpass filter is disabled

DHP-R Disable receive highpass for test reasons
- DHP-R = 0 Receive highpass filter is enabled
- DHP-R = 1 Receive highpass filter is disabled

TH[1)] Set transhybrid balancing filter - together with the bit FIXC (XR2,bit 4).
- For FIXC = 1: The TH-filter is set to H_{TH} = for Z_{BRD};
- For FIXC = 0:
- TH = 0 TH-filter is disabled
- TH = 1 TH-filter is enabled (use programmed values)

FRX[1)] Enable FRX-(Frequency Response Transmit) filter
- For FIXC = 0:
- FRX = 0 FRX-filter is disabled (H_{FRX} = 1)
- FRX = 1 FRX-filter is enabled (use programmed values)

FRR[1)] Enable FRR-(Frequency Response Receive) filter
- For FIXC = 0:
- FRR = 0 FRR-filter is disabled (H_{FRR} = 1)
- FRR = 1 FRR-filter is enabled (use programmed values)

AX[1)] Set AX- (Amplification/Attenuation Transmit) filter
- For FIXC = 0:
- AX = 0 AX-filter is set to default value (H_{AX} = 10 dB)
- AX = 1 AX-filter is enabled (use programmed values)

AR[1)] Set AR- (Amplification/Attenuation Receive) filter
- For FIXC = 0:
- AR = 0 AR-filter is set to default value (H_{AR} = – 15.11 dB)
- AR = 1 AR-filter is enabled (use programmed values)

IM[1)] Activates or deactivates the 64 kHz filter

IM = 0 64 kHz filter is deactivated (H_{IM} = 0)

IM = 1 64 kHz filter is activated

1) For MuSLIC-S these filters are always enabled; depending on bit FIXC (XR2, bit 4) the default settings or the programmed coefficients are used.

XTR4 Extended Operation Test Register 4

Extended Operation Test Register XTR4 defines testing features.

Bit	7	6	5	4	3	2	1	0
	DLB-8M	**DLB-64K**	**DLB-32K**	**DLB-PCM**	**ALB-8M**	**0**	**0**	**DCHOLD**

Reset value: 00_H

DLB-8M AC digital loop: 8 MHz in/output is short cut

DLB-8M = 0 Normal operation

DLB-8M = 1 8 MHz in/output is short cut

DLB-64K AC digital loop: 64 kHz in/output is short cut

DLB-64K = 0 Normal operation

DLB-64K = 1 64 kHz in/output is short cut

DLB-32K AC digital loop: 32 kHz in/output is short cut

DLB-32K = 0 Normal operation

DLB-32K = 1 32 kHz in/output is short cut

DLB-PCM AC digital loop: PCM in/output is short cut

DLB-PCM = 0 Normal operation

DLB-PCM = 1 PCM in/output is short cut

ALB-8M AC analog loop: 8 MHz in/output is short cut

ALB-8M = 0 Normal operation

ALB-8M = 1 8 MHz short cut

DCHOLD Holds the current DC-output

DCHOLD = 0 Normal operation

DCHOLD = 1 DC-output is held

XTR5 Extended Operation Test Register 5

XTR5 defines testing functions

Bit	7	6	5	4	3	2	1	0
	DC-DLB	**DC-ALBIT**	**0**	**DC-ALBIL**	**DC-ALBV**	**DCLMU2**	**DCLMU1**	**DCLMU0**

Reset value: 00_H

DC-DLB DC digital loop: 1 MHz in/output is short cut
DC-DLB = 0 Normal operation
DC-DLB = 1 1 MHz in/output is short cut

DC-ALBIT DC analog loop: IT is switched to DCP/DCN
DC_ALBIT = 0 Normal operation
DC_ALBIT = 1 IT is switched to DCP/DCN

DC-ALBIL DC analog loop: IL is switched to DCP/DCN
DC_ALBIL = 0 Normal operation
DC_ALBIL = 1 IL is switched to DCP/DCN

DC-ALBV DC analog loop: VA, VB, VBIM, VDDIM is switched to DCP/DCN
DC_ALBV = 0 Normal operation
DC_ALBV = 1 VA, VB, VBIM, VDDIM is switched to DCP/DCN

DCLMU Selects the signal switched to the DC-levelmeter

DCLMU2	DCLMU1	DCLMU0	
0	0	0	IT
0	1	0	IL
1	0	0	VA
1	0	1	VB
1	1	0	VBIM
1	1	1	VDDIM

XTR6 Extended Operation Test Register 6

XTR6 defines testing functions

Bit	7	6	5	4	3	2	1	0
	TTXL	**GAINBB**	**NOAGC**	**ILITMUX**	**COT16**	**DITOFF**	**AXG0**	**ARG0**

Reset value: 00_H

TTXL Enables current measurement for TTX
TTXL = 0 Normal operation
TTXL = 1, IM = 0 and OPIM8M = 1 enables TTX current measurement

GAINBB This bit enables an additional DC-gain of about 4 dB (factor of 1.6) inside the QAP in receive direction. Especially for test purposes in HIR/HIT mode it enables the use of the full voltage range of the AHV-SLIC.
GAINBB = 0 Normal operation
GAINBB = 1 Additional DC-gain is set

NOAGC Disable automatic gain control for TTX
NOAGC = 0 Normal operation
NOAGC = 1 Disable automatic gain control

ILITMUX IL changes to IT and vice versa
ILITMUX = 0 Normal operation
ILITMUX = 1 IL changes to IT and vice versa

COT16 Cut off transmit path
COT16 = 0 Normal operation
COT16 = 1 Cut off transmit path

DITOFF Disables the dither for noiseshapers. Obsolete for QAP V1.2 or higher.
DITOFF = 0 Normal operation
DITOFF = 1 Dither disabled

AXG0 0 dB gain for transmit path
AXG0 = 0 Normal operation
AXG0 = 1 0 dB gain for transmit path

ARG0 0 dB gain for receive path
ARG0 = 0 Normal operation
ARG0 = 1 0 dB gain for receive path

Table 10 Important Factors for the calculation of voltages and slopes in different modes by using MuSLICOS

For all values: "Active" selected in SCR10 and SCR0.ENTE=1	Factor with PEB31666 V1.3 and XTR6.GAINBB=0 or PEB 31666 V1.2	Factor with PEB31666 V1.3 and XTR6.GAINBB=1
SCR0.N/BB=0	0.625	1
SCR0.N/BB=1	1	1
HIR (high impedance ring) or HIT (high impedance tip) and SCR0.N/BB=1	0.3125	0.5
HIR (high impedance ring) or HIT (high impedance tip) and SCR0.N/BB=0 behaves like SCR0.N/BB=1	0.3125	0.5

XTR7 Extended Operation Test Register 7

XTR7 informs how many PEB 3465 are connected to the PEB 31666 and controls the level meter functions

Bit	7	6	5	4	3	2	1	0
	QDETQ4	**QDETQ3**	**QDETQ2**	**QDETQ1**	**0**	**0**	**CALMUX1**	**CALMUX0**

Reset value: 00_H

QDETQi Informs about PEB 3465 connection

QDETQi = 0 There is no PEB 3465 connected to the i-th interface

QDETQi = 1 There is a PEB 3465 connected to the i-th interface

Note: This information is available after the first AFSC-pulse

CALMUX Selects levelmeter source read by SCR4/SCR5 if CAL = 1 (Bit 7 of XTR1)

CALMUX1	CALMUX0	
0	0	DC-levelmeter thresholdpair 0
0	1	DC-levelmeter thresholdpair 1
1	0	AC-levelmeter
1	1	TTX-levelmeter

XTR8 Extended Operation Test Register 8

XTR8 enables Reserved Registers

Bit	7	6	5	4	3	2	1	0
	0	**0**	**0**	**0**	**0**	**0**	**0**	**ENRSV**

Reset value: 00_H

ENRSV Enables Reserved Registers (STCR1, XTR15 to XTR18)
ENRSV = 0 Normal operation
ENRSV = 1 Reserved registers are enabled

Note: In contrast to the other XTR-Registers it is possible to use bit ENRSV without setting bit ENTE (SCR0, bit1) to 1.

XTR9 to XTR11 Extended Operation Test Register 9 to 11 (for internal use only)

These bytes are used for the fuse operation of the PEB 3465.

XTR9

Bit	7	6	5	4	3	2	1	0
	0				**Fuse 0 QAP 1**	**Fuse 0 QAP 2**	**Fuse 0 QAP 3**	**Fuse 0 QAP 4**

Reset value: 00_H

XTR10

Bit	7	6	5	4	3	2	1	0
	Fuse 1 QAP 1	**Fuse 1 QAP 2**	**Fuse 1 QAP 3**	**Fuse 1 QAP 4**	**Fuse 2 QAP 1**	**Fuse 2 QAP 2**	**Fuse 2 QAP 3**	**Fuse 2 QAP 4**

Reset value: 00_H

XTR11

Bit	7	6	5	4	3	2	1	0
	Fuse 3 QAP 1	**Fuse 3 QAP 2**	**Fuse 3 QAP 3**	**Fuse 3 QAP 4**	**Fuse 4 QAP 1**	**Fuse 4 QAP 2**	**Fuse 4 QAP 3**	**Fuse 4 QAP 4**

Reset value: 00_H

XTR12 to XTR14 Extended Operation Test Register 12 to 14 (for internal use only)

XTR12 to XTR14 are reserved for the internal blocktest function.

Reset value: 00_H

Note: In order to allow operation of the internal block tests, the TEST pin of the MuPP PEB 31666 (pin 32) must be connected to high input voltage.

XTR15 to XTR17 Extended Operation Test Register 15 to 17

XTR15 to XTR17 are reserved for transfer of information from the PEB 31666 to the PEB 3465.

Reset value: 00_H

XTR18 Extended Operation Test Register 18

XTR18 is reserved for future use.

Reset value (always returned in current version): 00_H

4.1.3 TOP Command

With the TOP Command the TCR0 and TCR1 registers can be read. Each channel has its own registers addressed by the time slot or by address

Bit	7	6	5	4	3	2	1	0
	0	**R**	**1**	**1**	**0**	**0**	**LSEL1**	**LSEL0**

R Read information: enables reading from the MuSLIC

R = 0 No operation

R = 1 Read from MuSLIC

LSEL Length select information

This field identifies the selected TCR Register(s) and the handling of interrupts too.

LSEL 1	LSEL 0	
0	0	TCR0 (reset of the interrupt)
0	1	TCR1 (not masked interrupts are not affected)
1	1	TCR0 and TCR1 (reset of the interrupt)

TCR0 Configuration Register 0

TCR0 is the signalling register. It indicates status information of each channel. If there is any change of one or more bits it is indicated via the SCLX bit in the SCR8-channel. Each bit, except the RES bit, can be masked by the SCR2 Register (see also **Figure 29**).

Bit	7	6	5	4	3	2	1	0
	VB/2	**ICON**	**TEMP**	**FAIL**	**MVA**	**LSUP**	**RES**	**0**

Note: = **not defined with MuSLIC-S**

Reset value: 02_H

VB/2 Programable threshold for detecting the AHV-SLIC-feeding-voltage interrupt masked in Power Denial and Ringing State
VB/2 = 0 Line voltage smaller than threshold
VB/2 = 1 Line voltage larger than threshold

ICON Current limitation information, interrupt masked in Power Denial and Ringing State
ICON = 0 Resistive Feeding
ICON = 1 Constant Current Feeding

TEMP Temperature alarm of the AHV-SLIC which is signalled through the AHV-SLIC Interface (see **Chapter 3.4**)
TEMP = 0 Normal temperature
TEMP = 1 Temperature alarm from AHV-SLIC detected

FAIL MCLK or FSC Fail: Not the right count of clock cycles between two frame syncs
FAIL = 0 No clock fails are detected
FAIL = 1 Clock fails are detected
The FAIL bit is not influenced by the DUP-counter (each failure is reported).

MVA Internal measurement results shown in the TCR1-0 and TCR1-1 are valid or not valid (see **Chapter 7**)
MVA = 0 The level metering results are not valid
MVA = 1 The level metering results are valid

LSUP Line Supervision (of broken line)
LSUP = 0 The transversal current is lower than the programmed level
LSUP = 1 The transversal current is higher than the programmed level

RES Reset status

RES = 0	No Reset has occurred
RES = 1	Reset has occurred via RESET-pin or via Power on reset

Any change of these bits (except the FAIL bit: only the positive going is reported) is signalled via the interrupt-bit (SLCX) in the SCR8-register. There are two types of generating an interrupt:

– Each toggling of a non-masked TCR0-bit combined with a DUP-counter
– Toggling of the non-masked TEMP or MVA-bit and positive going FAIL bit (no filtering by the DUP-counter)

The status information is stored in the TCR0-register and an interrupt is generated but only if there isn't a not-handled interrupt.

Reading the TCR0-register gives the frozen interrupt status, clears the interrupt and enables the signalling of a further interrupt but not until after at least two 8 kHz frames.

Note: The HOOK and the GNK signalling are directly filtered by their own DUP(GNK)-counters and these results are directly put into the register SCR8 (see ***Page 82****).*

TCR1 Configuration Register 1

TCR1 indicates interrupt information and level meter results of one channel.

Bit	7	6	5	4	3	2	1	0
	NMVB/2	**NMICON**	**NMTEMP**	**NMFAIL**	**NMMVA**	**NMLSUP**	**RLM1**	**RLM0**

NOTE: **= not defined with MuSLIC-S**

Reset value: 00_H

NMVB/2 to NMLSUP Not masked signalling information. (The meaning of each bit is the same as described above.)
Reading this register won't affect any stored information.

RLM1 and RLM0 Result levelmetering

RLM1	RLM0	
0	0	below both levels
x	1	above level 0
1	x	above level 1

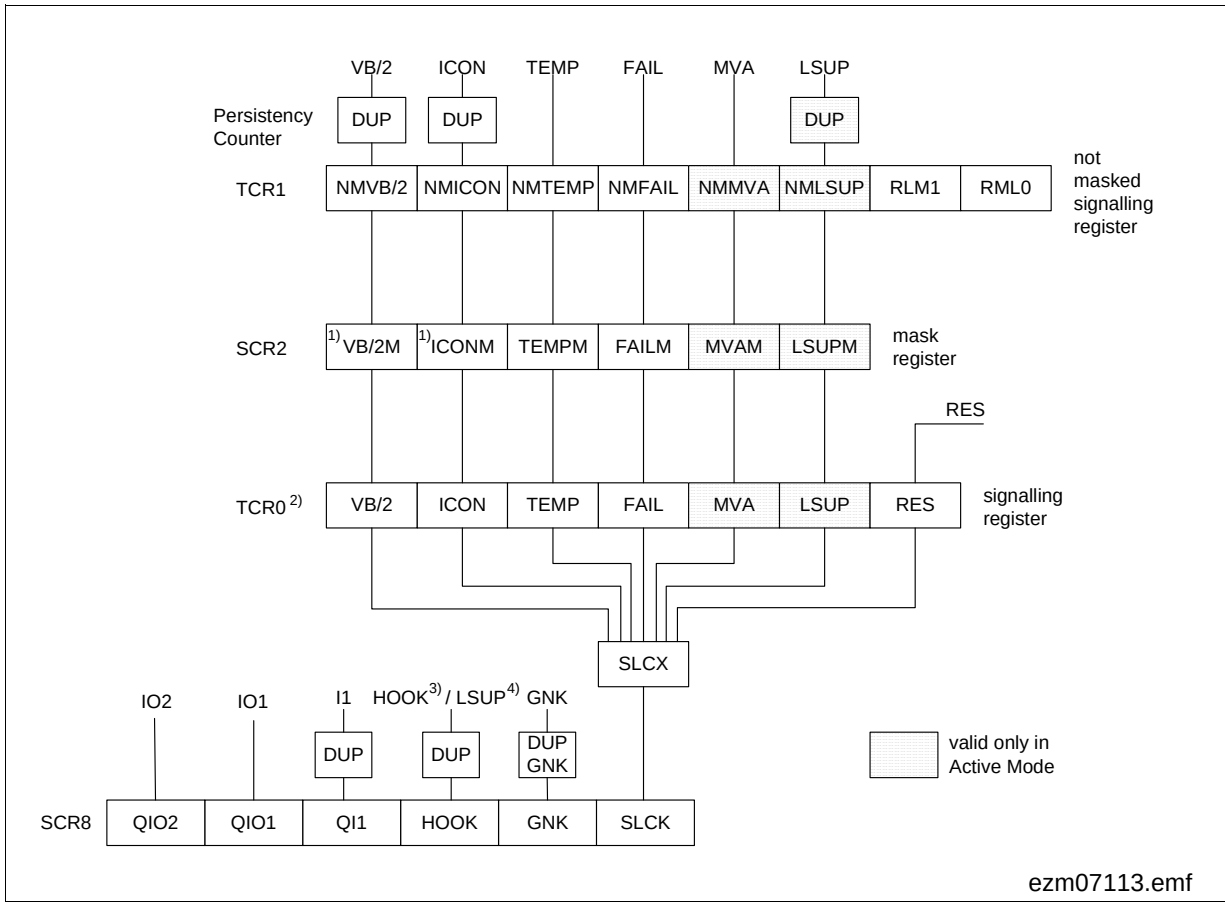


Figure 29 Interrupt Logic (Block Structure)

1) In Power Down and Ringing Mode changes of VB/2 and ICON are masked.

2) TCR0 is locked if one of the signals changes and is enabled after reading.
Each change of TCR0 sets the interrupt bit SLCX to 1.
Reading TCR0 sets SLCX to 0 but not before two 8 kHz frames.
A take over of the signal FAIL from TCR1 to TCR0 cleares this signal in TCR1.

3) In Power Down Mode the persistency counter 2 x DUP is used.

4) Realized in Ground Start Mode.

4.1.4 COP Command

With a COP command coefficients for the programmable filters can be written to or read from the MuSLIC.

(Filter optimizing to different applications is supported by the software package MuSLICOS.)

The coefficients are gathered to 8 and 4 SETs respectively. So an optimum is reached between supplying each channel, handling and memory space. **Figure 30** gives an overview of the Coefficient RAM (CRAM) structure.

To assign a SET to a channel the COPI command is used.

In channel specific programming mode (FIX-CHAN = 1 in XR2) the COP command will be handled as a channel specific SOP command.

Bit	7	6	5	4	3	2	1	0
	ICRAM	**RW**	**0**	**0**	**0**	**1**	**WCRAM1**	**WCRAM0**

Bit	7	6	5	4	3	2	1	0
	SET2	**SET1**	**SET0**	**CODE 4**	**CODE 3**	**CODE 2**	**CODE 1**	**CODE 0**

ICRAM Initialize CRAM

ICRAM = 0 Only one coefficient is programmed (destination is coded in the following byte) (no influence of WCRAM1 and WCRAM0)

ICRAM = 1 The whole AC- or DC-CRAM is written with the information of the following byte

RW Read/Write

RW = 0 Subsequent data is written to the MuSLIC

RW = 1 Read data from the MuSLIC

WCRAM1 and WCRAM0 Write to CRAM (only valid in combination with ICRAM=1)

WCRAM1	WCRAM0	
0	0	No write
0	1	AC-CRAM
1	0	DC-CRAM
1	1	AC-CRAM and DC-CRAM

SET Includes the number of coefficient set

SET2	SET1	SET0	
0	0	0	SET 0
0	0	1	SET 1
0	1	0	SET 2
0	1	1	SET 3
1	0	0	SET 4
1	0	1	SET 5
1	1	0	SET 6
1	1	1	SET 7

SET 0 to SET 7 For the 8 sets of AC-coefficients and the 8 sets of Tone Generator 1 and 2

SET 0 to SET 3 For the 4 sets of DC-coefficients

CODE Includes the number of following bytes and filter-addresses[1)]

CODE4	CODE3	CODE2	CODE1	CODE0		
0	0	0	0	0	TH-Filter coefficients (part 1)	(followed by 8 bytes of data)
0	0	0	0	1	TH-Filter coefficients (part 2)	(followed by 8 bytes of data)
0	0	0	1	0	TH-Filter coefficients (part 3)	(followed by 8 bytes of data)
0	0	0	1	1	FRX-filter coefficients	(followed by 8 bytes of data)
0	0	1	0	0	FRR-filter coefficients	(followed by 8 bytes of data)
0	0	1	0	1	AX-filter coefficients	(followed by 8 bytes of data)
0	0	1	1	0	AR-filter coefficients	(followed by 8 bytes of data)
0	0	1	1	1	TG1-filter coefficients	(followed by 8 bytes of data)
0	1	0	0	0	TG2-filter coefficients	(followed by 8 bytes of data)
0	1	0	0	1	AC test coefficients	(followed by 8 bytes of data)
0	1	0	1	0	IM-filter coefficients (part 3)	(followed by 8 bytes of data)
0	1	0	1	1	IM-filter coefficients (part 1)	(followed by 8 bytes of data)
0	1	1	0	0	IM-filter coefficients (part 2)	(followed by 8 bytes of data)
0	1	1	0	1	TG CSF (checksum fill)	(followed by 8 bytes of data)
0	1	1	1	0	AC CSF (checksum fill)	(followed by 8 bytes of data)
1	0	0	0	0	TTX test coefficients	(followed by 8 bytes of data)
1	0	0	0	1	TTX coefficients	(followed by 8 bytes of data)
1	0	0	1	0	AGC coefficients	(followed by 8 bytes of data)
1	0	0	1	1	LP-filter coefficients	(followed by 8 bytes of data)
1	0	1	0	0	Hook level coefficients	(followed by 8 bytes of data)
1	0	1	0	1	DC test coefficients	(followed by 8 bytes of data)
1	0	1	1	0	Ringing coefficients	(followed by 8 bytes of data)
1	0	1	1	1	DC-characteristic coefficients	(followed by 8 bytes of data)
1	1	0	0	0	Ramp generator, Ringer delay coefficients	(followed by 8 bytes of data)
1	1	0	0	1	DC CSF (checksum fill)	(followed by 8 bytes of data)

1) For generating a correct checksum all not used bits must be set to 0.

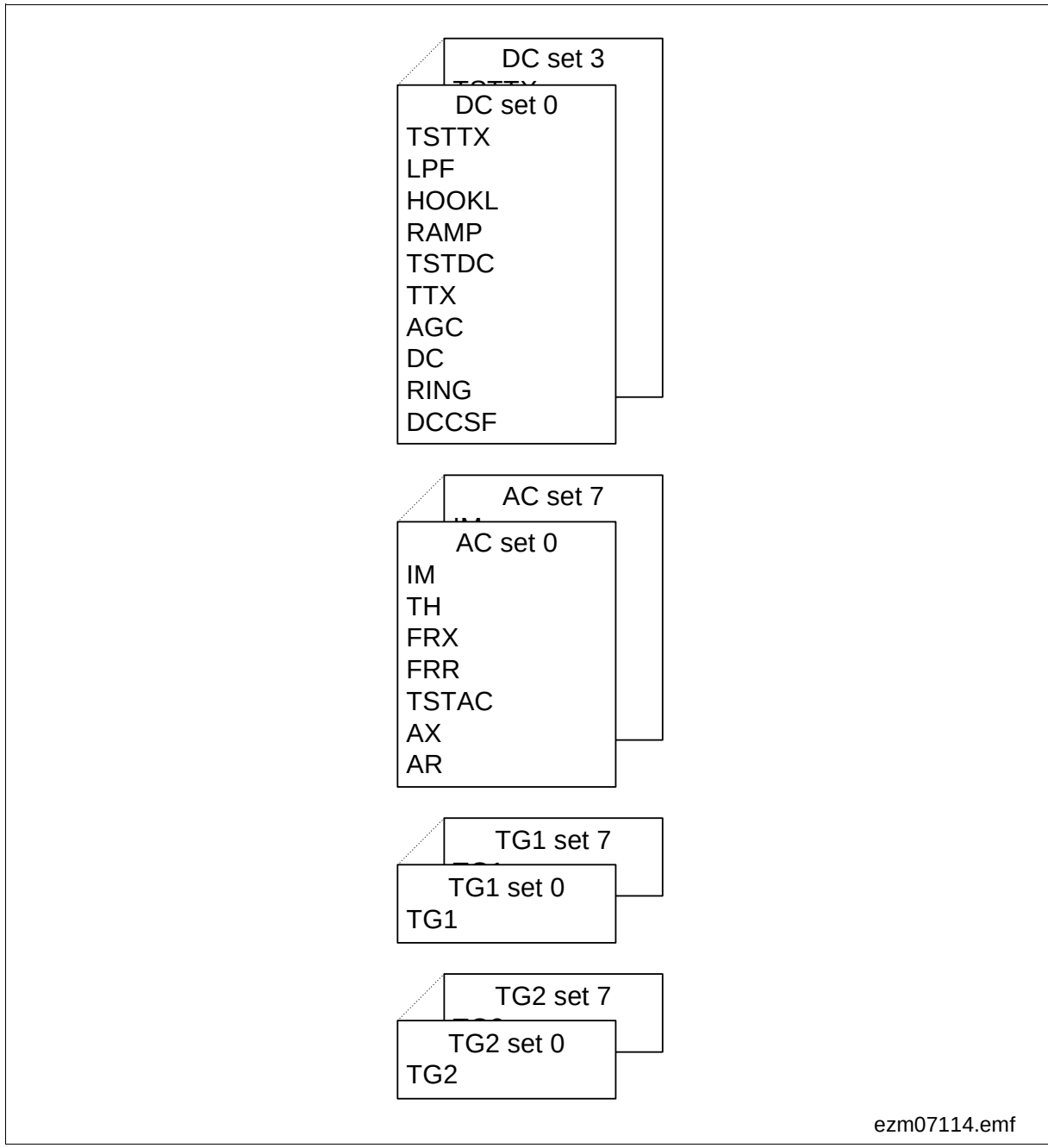


Figure 30 Overview of Coefficient Sets (FIX-CHAN = 0 in XR2)

In case of channel specific programming mode (FIX-CHAN = 1 in XR2) the AC- and TG-coefficients can be selected individually for all channels. In this mode 16 sets are available for AC, TG1 and TG2.

4.1.5 COPI Command

The COPI command allows to assign the sets of the Coefficient RAMs to a selected channel (given by the time slot or by address).

Bit	7	6	5	4	3	2	1	0
	B	**RW**	**0**	**0**	**1**	**0**	**LSEL1**	**LSEL0**

B Broadcast

B = 0	Only one channel (time slot) is programmed
B = 1	All channels (up to 16) are programmed with the same information

RW Read/ Write

RW = 0	Subsequent data is written to the MuSLIC
RW = 1	Set assignment is read

LSEL Length select information.
This field identifies the subsequent data byte(s).

LSEL 1	LSEL 0	
0	0	CAR0
0	1	CAR1
1	1	CAR0 and CAR1

In channel specific programming mode (FIX-CHAN = 1 in XR2) the assignment of AC and TG coefficients is ignored.

CAR0 Coefficient set Assignment Register 0

CAR0 indicates AC and DC coefficients set assignment.

Bit	7	6	5	4	3	2	1	0
	DC1	**DC0**	**AC2**	**AC1**	**AC0**	**0**	**0**	**HLOAD**

Reset value: 00_H

DC

DC1	DC0	
0	0	DC coefficient set 0
0	1	DC coefficient set 1
1	0	DC coefficient set 2
1	1	DC coefficient set 3

AC

AC2	AC1	AC0	
0	0	0	AC coefficient set 0
0	0	1	AC coefficient set 1
0	1	0	AC coefficient set 2
0	1	1	AC coefficient set 3
1	0	0	AC coefficient set 4
1	0	1	AC coefficient set 5
1	1	0	AC coefficient set 6
1	1	1	AC coefficient set 7

HLOAD Hook for load

HLOAD = 0 Normal operation

HLOAD = 1 Load is activated (LP03 will be preset; for normal operation this bit should not be used)

CAR1 Coefficient set Assignment Register 1

CAR1 indicates Tone Generator coefficients set assignment.

Bit	7	6	5	4	3	2	1	0
	TG1.2	**TG1.1**	**TG1.0**	**TG2.2**	**TG2.1**	**TG2.0**	**0**	**0**

Reset value: 00_H

TG1

TG1.2	TG1.1	TG1.0	
0	0	0	Tone Generator 1 set 0
0	0	1	Tone Generator 1 set 1
0	1	0	Tone Generator 1 set 2
0	1	1	Tone Generator 1 set 3
1	0	0	Tone Generator 1 set 4
1	0	1	Tone Generator 1 set 5
1	1	0	Tone Generator 1 set 6
1	1	1	Tone Generator 1 set 7

TG2

TG2.2	TG2.1	TG2.0	
0	0	0	Tone Generator 2 set 0
0	0	1	Tone Generator 2 set 1
0	1	0	Tone Generator 2 set 2
0	1	1	Tone Generator 2 set 3
1	0	0	Tone Generator 2 set 4
1	0	1	Tone Generator 2 set 5
1	1	0	Tone Generator 2 set 6
1	1	1	Tone Generator 2 set 7

5 Operating Modes

The MuSLIC supports 4 different operating modes: Power Down (PDown), Active, Ringing and Ground Start which are controlled via the lower 3 bits of the Configuration Register SCR10:

M2 (SCR10-4)	M1 (SCR10-3)	M0 (SCR10-2)	Description
0	0	0	Power-Down High Impedance (PDNH)
1	1	1	Power-Down Resistive (PDNR)
0	1	0	Active State
1	1	0	Active State with meterpulses
0	0	1	Ringing State (ring pause)
1	0	1	Ringing State (ring burst on)
1	0	0	Ground Start
0	1	1	Must not be used

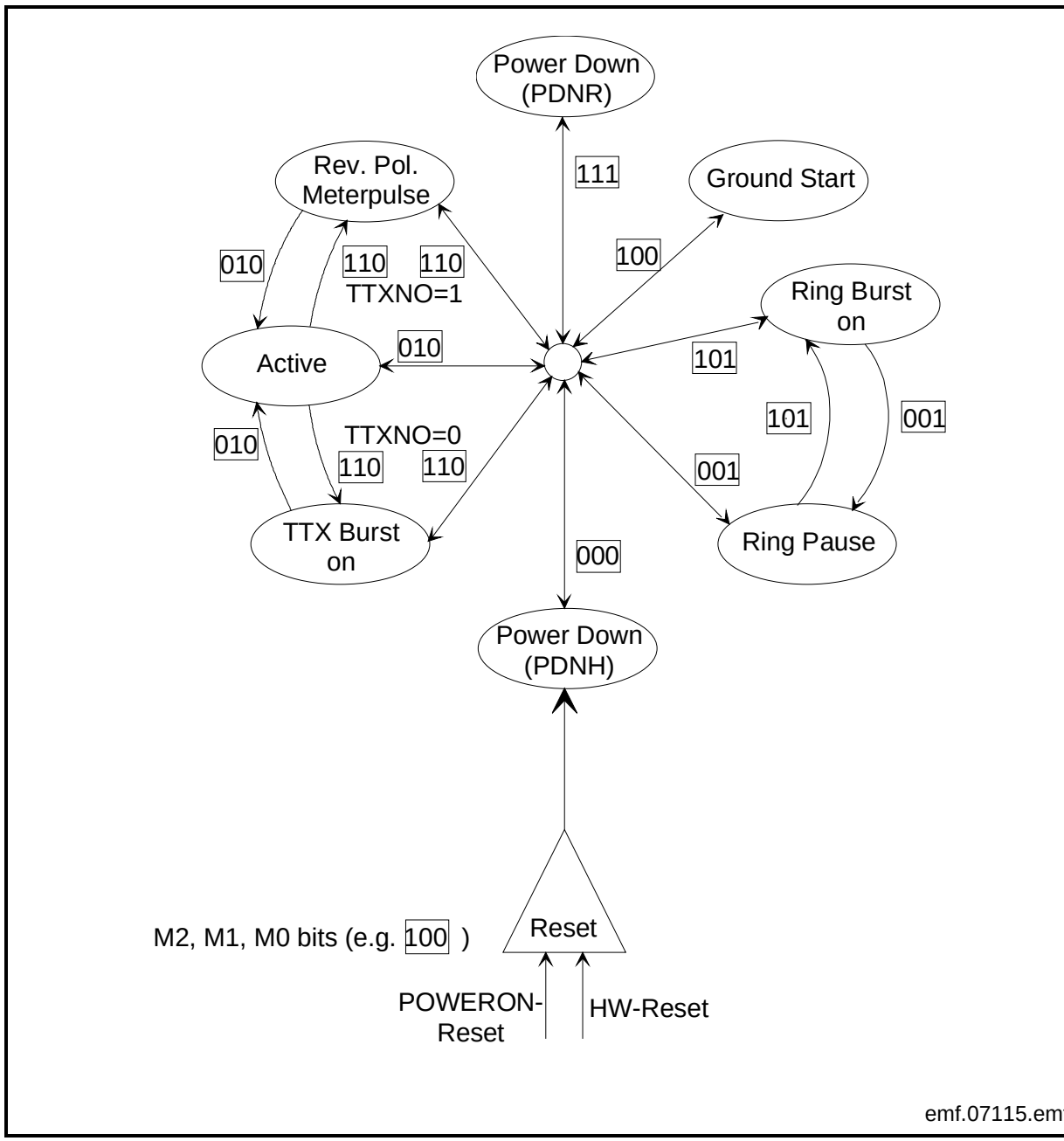


Figure 31 Operating Modes

Table 11 Operating Modes MuSLIC-E

MuSLIC Mode	Configuration Register (MuPP µC)										AHV-SLIC Interface			QAP
	M2 SCR10 Bit 4	M1 SCR10 Bit 3	M0 SCR10 Bit 2	IO2[1] SCR10, Bit6	N/BB SCR0 Bit 6	ACT2 SCR1 Bit 2	GAINBB[2] XTR6 Bit 6	HIR[2] XTR0 Bit 6	HIT[2] XTR0 Bit 7	Load	C1	C2	C3[1]	Boost-factor[3]
Power-Down High Impedance (PDNH) {+ 5k}	0	0	0	{IO2}	X	X	X	X	X	X	M	L	{IO2}	0
Power-Down Resistive (PDNR)	1	1	1	X	X	X	X	X	X	X	L	M	X	0
Active State (ACT) {+ 5k}	0	1	0	{IO2}	0	0	0	0	0	0	H	M	{IO2}	0
Active State reduced battery (ACT2) {+ 5k}	0	1	0	{IO2}	0	1	0	0	0	0	H	L	{IO2}	0
Active State (load) {+ 5k}	0	1	0	{IO2}	0	0	0	0	0	1	L	L	{IO2}	0
Active State red. Batt (load) {+ 5k}	0	1	0	{IO2}	0	1	0	0	0	1	L	L	{IO2}	0
Active Boost State 50mA (BB-50)	0	1	0	0	1	X	X	0	0	X	M	M	0	1
Active Boost State 100mA (BB-100)	0	1	0	1	1	X	X	0	0	X	M	M	1	1
Active State with Meterpulses (ACT)	1	1	0	{IO2}	0	0	0	0	0	0	H	M	{IO2}	0
Active State with Meterpulses red. Batt. (ACT2)	1	1	0	{IO2}	0	1	0	0	0	0	H	L	{IO2}	0
Active State, Meterpulses (load) {+ 5k}	1	1	0	{IO2}	0	0	0	0	0	1	L	L	{IO2}	0
Active State, Meterpulses, red. Batt. (load) {+ 5k}	1	1	0	{IO2}	0	1	0	0	0	1	L	L	{IO2}	0
Active Boost State with Meterpulses 50mA (BB-50)	1	1	0	0	1	X	X	0	0	X	M	M	0	1
Active Boost State with Meterpulses 100mA (BB-100)	1	1	0	1	1	X	X	0	0	X	M	M	1	1
High Impedance Ring (HIR) {+ GAINBB} {+ 5k}	X	1	0	{IO2}	X	X	{GAINBB}	1	0	X	L	H	{IO2}	{GAINBB}
High Impedance Tip (HIT) {+ GAINBB} {+ 5k}	X	1	0	{IO2}	X	X	{GAINBB}	0	1	X	M	H	{IO2}	{GAINBB}
High Impedance Ring/Tip (HIRT) {+ GAINBB} {+ 5k}	X	1	0	{IO2}	X	X	{GAINBB}	1	1	X	H	H	{IO2}	{GAINBB}
High Impedance Ring (HIR) {+ GAINBB} {+ 5k}	X	0	1	{IO2}	X	X	{GAINBB}	1	0	X	L	H	{IO2}	{GAINBB}
High Impedance Tip (HIT) {+ GAINBB} {+ 5k}	X	0	1	{IO2}	X	X	{GAINBB}	0	1	X	M	H	{IO2}	{GAINBB}
High Impedance Ring/Tip (HIRT) {+ GAINBB} {+ 5k}	X	0	1	{IO2}	X	X	{GAINBB}	1	1	X	H	H	{IO2}	{GAINBB}
High Impedance Ring (HIR) {+ GAINBB} {+ 5k}	1	0	0	{IO2}	X	X	{GAINBB}	1	0	X	L	H	{IO2}	{GAINBB}
High Impedance Tip (HIT) {+ GAINBB} {+ 5k}	1	0	0	{IO2}	X	X	{GAINBB}	0	1	X	M	H	{IO2}	{GAINBB}
High Impedance Ring/Tip (HIRT) {+ GAINBB} {+ 5k}	1	0	0	{IO2}	X	X	{GAINBB}	1	1	X	H	H	{IO2}	{GAINBB}

Table 11 Operating Modes MuSLIC-E (Continued)

MuSLIC Mode	Configuration Register (MuPP µC)										AHV-SLIC Interface			QAP
	M2 SCR10 Bit 4	M1 SCR10 Bit 3	M0 SCR10 Bit 2	IO2[1] SCR10, Bit6	N/BB SCR0 Bit 6	ACT2 SCR1 Bit 2	GAINBB[2] XTR6 Bit 6	HIR[2] XTR0 Bit 6	HIT[2] XTR0 Bit 7	Load	C1	C2	C3[1]	Boost-factor[3]
Ground Start {+ GAINBB} {+ 5k}	1	0	0	{IO2}	X	X	{GAINBB}	X	X	X	M	H	{IO2}	{GAINBB}
Ringing State (ring pause) 50mA	0	0	1	0	X	X	X	0	0	X	M	M	0	1
Ringing State (ring burst on) 50mA	1	0	1	0	X	X	X	0	0	X	M	M	0	1
Ringing State (ring pause) 100mA	0	0	1	1	X	X	X	0	0	X	M	M	1	1
Ringing State (ring burst on) 100mA	1	0	1	1	X	X	X	0	0	X	M	M	1	1
must not be used	0	1	0	X	0	X	1	0	0	X	H	M	X	1
must not be used	1	1	0	X	0	X	1	0	0	X	L	L	X	1
must not be used	0	1	1	X	X	X	0	X	X	X	M	L	X	0

Transient state - this state occurs for 2ms after a change from any powerdown mode (PDNH or PDNR) to an active mode (ACT, ACT2)

1) *It is assumed that the resp. IO2 Pin of the QAP is connected together with the resp. C3 Pin of the AHV-SLIC*

2) *These Bits are masked with Bit ENTE (SCR0, Bit1); come only into effect if ENTE is set to 1*

3) *Analog dc-gain in QAP, see also* ***Table 10****.*

Note: {IO2} means that it can be either 0 or 1, but all {IOM2} in one row are of the same logical state; if it is 1, the additional explanation in the first column is valid {+5k}
{GAINBB} means that it can be either 0 or 1, but all {GAINBB} in one row are of the same logical state; if it is 1, the additional explanation in the first column is valid {+GAINBB}

5.1 Reset Behaviour

The MuSLIC has 2 different reset sources that are internally connected.

- The **Reset pin**,
  which work asynchronously to the external clocks.
- **Power On Reset**
  If internal VDD rises above typ. 2.33 V the MuPP µC is reset by Power On Reset.

Both sources set the MuSLIC to the basic setting modes (see below).

The pin RESET of the MuPP µC and the QAP has a Schmitt-Trigger input to reduce the sensitivity for spikes. In addition the pin RESET has a spike rejection. All spikes smaller than 50 ns are neglected. The pin RESET can be driven to 1 for an unlimited time but at least 2 µs is recommended.

In the MuPP µC a reset activates the reset routine - but only if the MCLK is present - which lasts at least two 2 kHz periods for setting the default values. After this time and if an external reset is not active (RESET = 0) the MuPP µC starts the normal (default) operation at the beginning of the next 8 kHz frame (FSC).
The PCM and the µC-interface are reset. Running communication is stopped.

In the QAP a reset works asynchronously and no reset routine is necessary.
The normal (default) operation of the QAP starts at the beginning of a 2 kHz frame (AFSC) as soon as the external reset (RESET = 0) is released.

5.2 Basic Setting Modes

After initiating a reset in the MuPP µC (by the reset pin or power on reset), the reset bit (TCR0 bit1 = RES) is set to one and the SLCX-interrupt (SCR8) is activated. Reading the TCR0 register clears the interrupt and the RES-bit.

After resetting the MuPP µC, the MuSLIC is switched automatically to its basic settings in which internal default values for all filters and parameters (AC and DC) are used. All subscriber lines are switched to high impedance state, no supervision can be done (MuSLIC is set to Power Down High Impedance state). The MuSLIC can be programmed or configured via the µC interface

Actions initialized by a reset:

- All configuration registers are set to their default values (note that the Coefficient RAM is **not** reset)
- AC- and DC-loop use the default values and not the programmed ones (see below)
- All bits of the Signalling Register TCR0 are masked and reset to 0 without the RES-bit
- The SCR8 bits are set to 0 except SLCX, SLCX is set to 1 (the IO's are set to Input pins)
- The RES-bit (TCR0, bit1) is set to 1 to indicate that a reset has taken place
- INTR is set to 1 (Intel-Mode) or 0 (Motorola-Mode) due to the Power on Reset bit (TCR0, bit 1)
- The µC interface is ready for receiving data
- Outputs of PCM interface (TCA, TCB, DXA, DXB) are switched to high impedance, AFSC, ADCL, ADD1, ADD2 to zero
- C1 and C2 represent PDNH mode
- Boosted Battery is reset to normal feeding
- Reverse polarity is reset to normal polarity
- A-Law is chosen

Table 12 Default DC Values (FIXC (XR2 bit 4) = 1)

DC			
I_{Lim}	24	mA	Limit for constant current
V_{Lim}	38	V	Voltage of limit between constant current and resistive char.
V_{const}	40	V	Constant voltage
BoostGain	1.3		Additional gain in Boosted Battery Mode
R_{FS}	375	Ω	Feeding resistance (excluding the external fuse resistors)
f_{Ring}	25	Hz	Ring frequency
A_{Ring}	62	Vrms	Ring rms-value at Ring/Tip wire
DC $Offset_{Ring}$	22	V	Ring offset
f_{RingLP}	75	Hz	Corner frequency of ring-lowpass

Table 12 Default DC Values (Continued)(FIXC (XR2 bit 4) = 1) (Continued)

Off-hookPD	2	mA	Power-Down current for off-hook detection
Off-hookAct	8	mA	Off-hook detection in Active with 2 mA hysteresis
Off-hookRing	5	mA	DC-Current for off-hook detection in Ringing Mode
LineSup	5	mA	Current for line-supervision
Levelmeter1	8	mA	First levelmeter threshold
Levelmeter2	12	mA	Second levelmeter threshold
Levelmeter3	21	mA	Third levelmeter threshold
Levelmeter4	25	mA	Fourth levelmeter threshold
GKD1	17	mA	First threshold-current for Ground Key Detection
GKD2	40	mA	Second threshold-current for Ground Key Detection
RingTip	52	V	Threshold at Ring/Tip wire
DC-Lowpass	0.3/20	Hz	DC-lowpass set to 0.3 and 20 Hz respectively
ConstRamp	300	V/s	Slope of the ramp while testing
$delay_{Ring}$	0	ms	Delay of ring burst
SRend1	1/128		Soft-reversal threshold 1 (referred to the input of the ramp generator)
SRend2	1/512		Soft-reversal threshold 2 (referred to the input of the ramp generator)
SRduration	ca. 80	ms	Duration of a Soft-Reversal-sequence
DUP	10	ms	Data Upstream Persistency Counter is set to 10 ms
DUPGNK	20	ms	Data Upstream Persistency Counter for GNK is set to 20 ms

Table 13 Default AC Values

AC			
IM-Filter	900	Ω	Approximately 900 Ω Real Input Impedance
TH-Filter	TH_{BRD}		Approximately BRD-Impedance for Balanced Network
AX	10	dB	Attenuation Transmit (this means about 0 dB)
AR	– 15.11	dB	Attenuation Receive (this means about – 7 dB)
ATTX	4	Vrms	Teletax Generator Amplitude at Ring / Tip wire at AHV-SLIC
f_{TTX}	16	kHz	Teletax Generator frequency;
TG1	1008	Hz	Tone Generator 1 and AC -levelmeter Bandpass (– 14 dBm0)
TG2	2000	Hz	Tone Generator 2 (+ 2 dB compared to TG1)

5.3 Power Down (PDown) and Standby

SCR10: (M0/M1/M2=0/0/0,1/1/1)

After a Reset (including the Power On Reset) or programing the SCR10-Byte (SCR10-4 .. SCR10, bit 4 ... bit 2) the MuSLIC is set to Power Down State (in case of Reset Power-Down High Impedance). In Power Down all functions which are not necessary are disabled to minimize power consumption. This can be done for all the channels or only for the not active ones. While the interface is fully working - including programmability of the registers with SOP or XOP commands and the Coefficient RAM (COP commands) - the rest of the MuSLIC is turned off.
In case of Power-Down Resistive supervision of the line remains active. Therefore Power-Down resistive is the proper standby mode of MuSLIC in on-hook state for most applications. The change of the line state is reported via the HOOK-bit in SCR8. To avoid spurious off-hook indications caused by longitudinal induction the HOOK-bit is low pass filtered (programmable with the DUP-counter).

In Power Down Mode the AHV-SLIC can be set into two different modes:

1. PDNR, the resistive mode which provides a connection of 5 kΩ from TIP and RING to BGND and VBAT, respectively. Supervision of the line remains active.
2. PDNH, offers high impedance at TIP and RING, no hook-detection or supervision is present

5.4 Active Mode (Act)

SCR10: (M0/M1/M2=0/1/0,0/1/1)

In Active Mode (“Conversation State”) both AC-and DC-loop are fully working. The output voltage at the QAP (DCP, DCN) is controlled via the IT input pin in such a way, that it behaves like a constant current source which automatically turns into a programmable resistive feeding source due to the DC-characteristic values.

The ternary AHV-SLIC interface is set to one of the active modes.

Polarity

The MuSLIC supports either normal or reverse polarity which is set by the POLNR-bit (SCR0, Bit 7). A 180° phase shift of the DC-loop is done. The performance and the functionality is not be influenced by that.

Boosted Battery

To feed subscriber lines with enhanced loop resistance the MuSLIC-E supports the Boosted Battery mode. The AHV-SLIC interface pins (C1, C2) are set to Boosted Battery (BB) mode and the maximum DC output voltage is extended to 140 V.

Meterpulses

The MuSLIC supports two different kinds of meterpulses: Meterpulses with 12/16 kHz (Teletax Metering) and with polarity reversal. The decision between these two types is made by the bit TTXNO (SCR1, bit 7). If the bit TTXNO is set to 1 then the meterpulse is reversal. If the bit TTXNO is set to 0, Teletax Metering is used.

Metering with Polarity Reversal:

At a mode change from Active State to Active State with meterpulses the MuSLIC performs a phase shift in the DC-feeding, influenced by the bit SOREV (SCR1, Bit 4).

SOREV = 0: an immediate reversal („hard reversal“) is performed

SOREV = 1: a soft (silent) reversal is performed (transition time programmable by CRAM-coefficients, default value 80 ms)

Teletax Metering Injection (not available with MuSLIC-S):

For countries with Teletax Metering the MuSLIC-E provides either a 12 or 16 kHz signal which is selectable by the bit TTX12 (SCR1, bit 6)[1]. The amplitude of this Teletax signal is programmable up to 10 Vrms at the Ring/Tip wire of the AHV-SLIC. The MuSLIC filters the Teletax pulses in transmit direction, too. The slope of the pulses are internally shaped so that the noise during switching and transmission is less than 1 mV. With the bit NOSL (SCR1-5) the slope can be switched off. In that case the switching noise is not defined (for signalling only).

1) Note, that the right Teletax coefficient set (via COP-command) must be provided, too.

5.5 Ringing Mode

SCR10: (M0/M1/M2=1/0/0,1/0/1)

The MuSLIC generally supports balanced and unbalanced ringing.
If the MuSLIC is set to Ringing Mode, the AC-loop is turned off and the DC-loop is automatically opened.

Balanced Ringing (not available with MuSLIC-S)

The sine wave of the ringing is generated in the MuPP µC. The frequency and the amplitude are free programmable between 16 and 70 Hz and up to 85 Vrms at the Ring/ Tip wire, respectively. The DC offset voltage is programmable. If the Ring Burst On command is sent to the MuPP µC via SCR10 the begin („ring burst on“) and the end („ring pause“) of the ring burst is automatically synchronized at the voltage zero crossing. If the DC-current at the IT-pin exceeds the programmed value, Off-hook is detected within 2 periods of the ringing frequency and the Ring Burst is switched off. If Off-hook is detected the MuSLIC remains in the ringing pause mode (no evaluation of the DUP-Counter is performed).

Unbalanced Ringing

The ringing voltage is generated by an external ring generator. To connect this generator to the Ring/Tip wires usually relays have to be used. For controlling the relays the MuSLIC offers the following functions:

If the REXTEN bit (XR2 bit 7) is set to 1 the IO1 pin of the MuPP µC will be an input for the zero crossing signal. QAP pins I/O1-A...D are controlled by the SCR10, bit 4 (M2 bit) and offers a zero crossed ring burst on/off control signal.

– Improved Support of External Ringing Delay

Ring delay coefficients are used to compensate the delay of the ring relay. This is important to guarantee that the ring generator is disconnencted from the line at zero crossing of the ringing signal. When ring burst on (RBO) is detected, the output pin IO1 of the QAP is low active to drive directly the ring relay.

5.6 Ground Start

SCR10: (M0/M1/M2=0/0/1)

Changing into the Ground Start mode by programming the SCR10 (M2 = 1, M1 and M0 = 0) the active mode is chosen and the Ternary SLIC-interface is set to high impedance of the Tip output (HIT: C1 = VOM, C2 = VOH).

5.7 Changing Modes

The DUP counter responsible for filtering the hook status is loaded with the double of the programmed value if any change between the modes PDN, Active or Ringing or if one of the following crossovers occurs:

reverse	<---->	normal polarity
ground start on	<---->	off
PDNR on	<---->	off
FIXC, HLOAD, RESET on	<---->	off

6 Transmission Characteristics

The figures in this data sheet are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) needs a complete knowledge of MuSLIC analog environment. Unless otherwise stated, the transmission characteristics parameters are guaranteed within the test conditions and a temperature range of T_A = 0 to 70 °C. The functionality of MuSLIC is guaranteed for T_A = – 40 to 85 °C.

Test Conditions

T_A = 25 °C;

$V_{DDI} = V_{DDA} = V_{DDB} = V_{DDC} = V_{DDD}$ = 5 V ± 5%; V_{SS} = – 5 V ± 10%;

V_{DD} = 3.3 V ± 5%

GNDI = GNDA = GNDB = GNDC = GNDD = 0 V

H_{IM}, H_{TH}, H_{FRX}, H_{FRR}, AR, AX will be defined to meet the 0 dBm0 specification.

f = 1004 Hz; 0 dBm0; A-Law;

A 0 dBm0 AC signal in transmit direction is equivalent to 2 × 0.775 Vrms and in Receive direction equivalent to 0.775 Vrms (referred to 600 Ω).

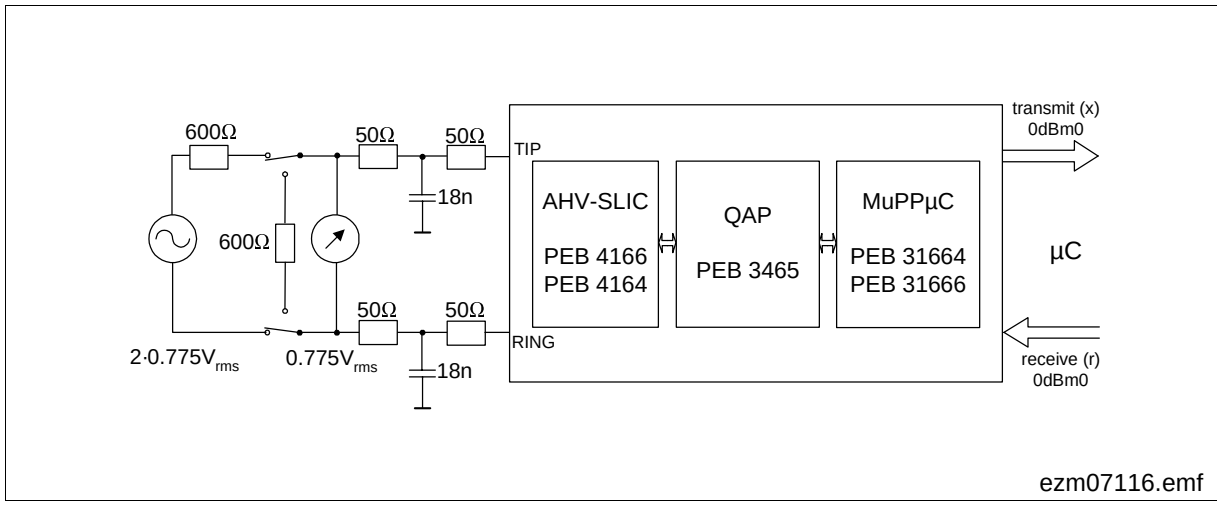


Figure 32 Transmission Characteristics

$0\ dBm0|_{MuSLIC} = 0\ dBm0|_{600\ \Omega}$ = 0.775 Vrms for receive direction.

$0\ dBm0|_{MuSLIC} = 0\ dBm0|_{600\ \Omega}$ = 0.775 Vrms for transmit direction.

Note: To meet the typical values of all programmable parameters (marked with [1]) listed in the following tables it is necessary to calculate the coefficients by using MuSLICOS.

6.1 Transmission Values

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
2-Wire Port						($2 \times 100\ \Omega$ R_p incl.)
Transmission performance						
Overload level	V_{TR}	2.3	–	–	Vrms	300 Hz to 4 kHz
Return loss (2-wire)	R_L	17	–	–	dB	300 Hz to 500 Hz
	R_L	22	–	–	dB	500 Hz to 2 kHz
	R_L	22	–	–	dB	2 kHz to 3.4 kHz
Insertion loss						
Transmit gain	G_t	– 0.3	–	0.3	dB	0 dBm0, 1 kHz
Receive gain	G_r	– 0.3	–	0.3	dB	0 dBm0, 1 kHz
Insertion loss versus frequency						relative to 1 kHz
Transmit gain	G_t[1)]	see **Chapter 6.2**				0 dBm0, 0.3 to 3.4 kHz
Receive gain	G_r[1)]	see **Chapter 6.2**				0 dBm0, 0.3 to 3.4 kHz
Gain/Loss programmability						
Transmit absolute – 3 ...+ 3 dBr step size	T_X[1)]	–	–	1/16	dB	voice band
Receive absolute 0 … – 12 dBr step size	R_X[1)]	–	–	1/16	dB	voice band

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Gain linearity						relative to 1 kHz, – 10 dBm0
Transmit gain	G_t [1)]	see **Chapter 6.3**				– 55 dBm0 to + 3 dBm0
Receive gain	G_r [1)]	see **Chapter 6.3**				– 55 dBm0 to + 3 dBm0
Absolute group delay distortion		see **Chapter 6.4**				
Overload compression A/A	OC	see **Chapter 6.5**				
Longitudinal balance						
MuSLIC, -E, -S	L-T	52	53	–	dB	300 Hz to 3.4 kHz
MuSLIC-E2, -S2	L-T	58	63	–	dB	at 1020 Hz
Transversal to longitudinal	T-L	46	–	–	dB	300 Hz to 4 kHz
Longitudinal signal generation	4-L	46	–	–	dB	300 Hz to 4 kHz

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Out-of-band Noise						single frequency inband – 25 dBm0
Transversal	V_{TR}	–	–	– 50	dBm	12 kHz to 200 kHz
Longitudinal	V_{TR}	–	–	– 50	dBm	12 kHz to 200 kHz
Metering injection[1)]						
Impulse noise during switching	V_{TR}	–	–	1	mV	psophometrically weighted
Metering signal	V_{TTXRL}[1)]	4.5	4.85	5.2	Vrms	12/16 kHz, R_L = 200 Ω (see **Figure 33**)
At 2-, 4-wire interface	V_{tx}	–	–	1	mV	psophometrically weighted
Harmonic distortion		–	–	5	%	
Ringing injection						
Transfer gain error	G_{rng}	– 0.5	±0.3	0.5	dB	Z_L = 1200 Ω
Ringing injection	V_{TR}[1)]	60	63	66	Vrms	16 Hz to 50 Hz (without load)
Superimposed DC voltage	V_{rdc}[1)]	20	22	24	V	R_L = 10 kΩ
Harmonic distortion	THD	–	–	5	%	Z_L = 1 kΩ || 6 µF
Ring trip function[1)]						
Detection time and delay after		12 ms	–	2	periods	
The ringing to off-hook status		–	–	2	periods	

[1)] not available in MuSLIC-S

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
2-wire Port and PCM Side						
Total harmonic distortion						
2- to 4-wire	T_{hd4}	–	–	– 46	dB	– 7 dBm0, 0.3 to 3.4 kHz
4- to 2-wire	T_{hd2}	–	–	– 46	dB	– 7 dBm0, 0.3 to 3.4 kHz
Idle Channel Noise						
2-wire port (receive)						psophometric
A-Law	V_{TR}	–	–	– 70	dBmp	(idle code $_{+}$0)
						C-message
µ-Law	V_{TR}	–	–	20	dBrnc	(idle code $_{+}$0)
PCM side (transmit)						
A-Law	N_{TP}	–	–	– 67	dBmp	psophometric (V_{IN} = 0)
µ-Law	N_{TC}	–	–	20	dBrnc	C - message (V_{IN} = 0)
Signal to total distortion ratio						
Input connection: L_i = 0 dBr	S/D	see **Chapter 6.6**				– 45 dBm0 to 0 dBm0
Output connection: L_o = – 7 dBr	S/D	see **Chapter 6.6**				– 45 dBm0 to 0 dBm0

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Battery Feeding						V_{BAT} = – 68 V, V_H = + 52 V
Power Down Mode (PDNR)						
TIP to V_{BGND}, RING to V_{BAT} resistance	R_S	4.2	5	5.8	kΩ	
Active Mode						without calibration
I_{loop} accuracy	I_L [1]	23 [2]	25	27 [2]	mA	I_{lim2} = 25 mA
I_{loop} accuracy	I_L [1]	27 [2]	30	33 [2]	mA	I_{lim3} = 30 mA
I_{loop} accuracy	I_L [1]	41 [2]	45	49 [2]	mA	I_{lim4} = 45 mA
Current limitation AHV-SLIC	I_{max}	90	–	120	mA	wire to ground
Transition time	T_{off}	0.5	–	1.5	ms	On- to Off-hook
Boost Battery Mode						
Loop current						same as active state
Output voltage	V_{TR} [1]	78	–	86	V	I_{line} = 20 mA
Indication thresholds						
Off-hook indication						
Off-hook current	I_{det} [1]	7	9	11	mA	
Hysteresis		–	2	–	mA	
Ground Key indication						
Ground Key current	I_{det} [1]	10	17	24	mA	
Ring trip indication						
Current threshold 1	I_{det} [1]	6	7	8	mA	short line + bat. charging

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power supply rejection ratio						V_{ripple} = 100 mVpp
VDD referred to AGND	PSRR	40	–	–	dB	50 Hz to 4 kHz
VSS referred to AGND	PSRR	40	–	–	dB	50 Hz to 4 kHz
VBAT referred to AGND	PSRR	40	–	–	dB	50 Hz to 4 kHz
VBAT2 referred to AGND		40	–	–	dB	50 Hz to 4 kHz
VH referred to AGND	PSRR	40	–	–	dB	50 Hz to 4 kHz
BGND referred to AGND	PSRR	40	–	–	dB	50 Hz to 4 kHz

1) Programmable parameter.

2) An offset calibration has to be performed in order to guarantee these min/max values.

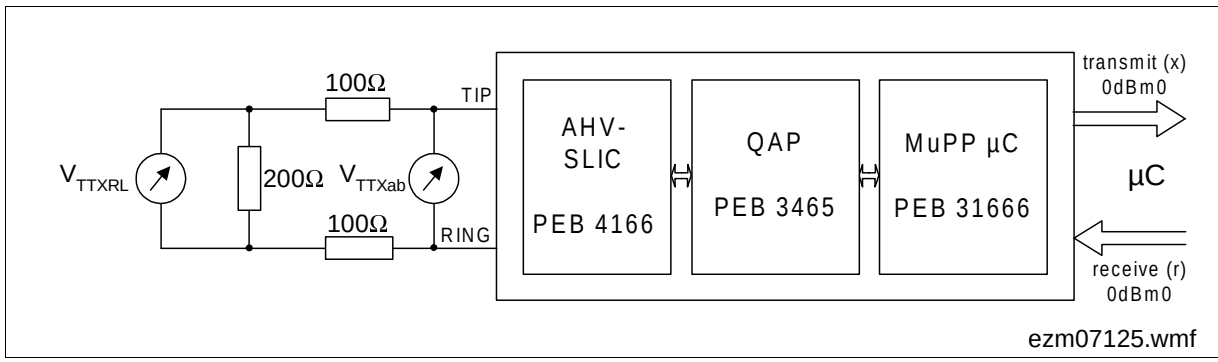


Figure 33 Voltage Amplitude of Teletax Metering

6.2 Frequency Response

Transmit: reference frequency 1 kHz, signal level – 10 dBm0, H_{FRX} = 1

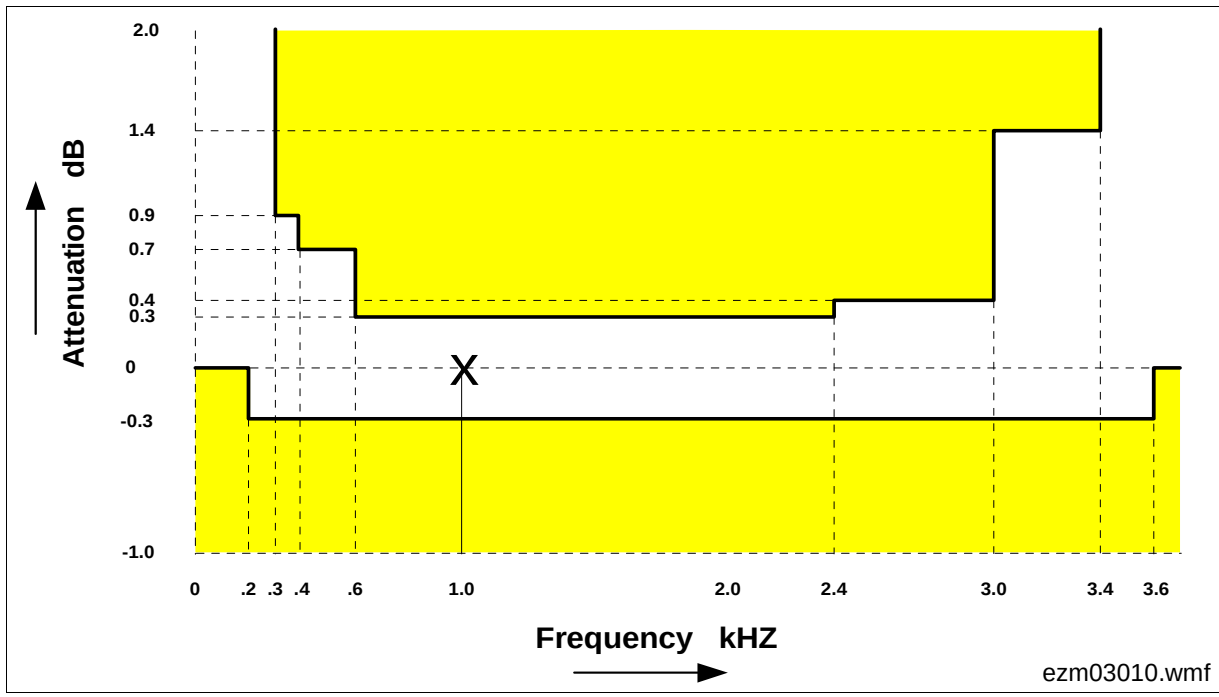


Figure 34 Frequency Response Transmit

Receive: reference frequency 1 kHz, signal level – 10 dBm0, H_{FRR} = 1

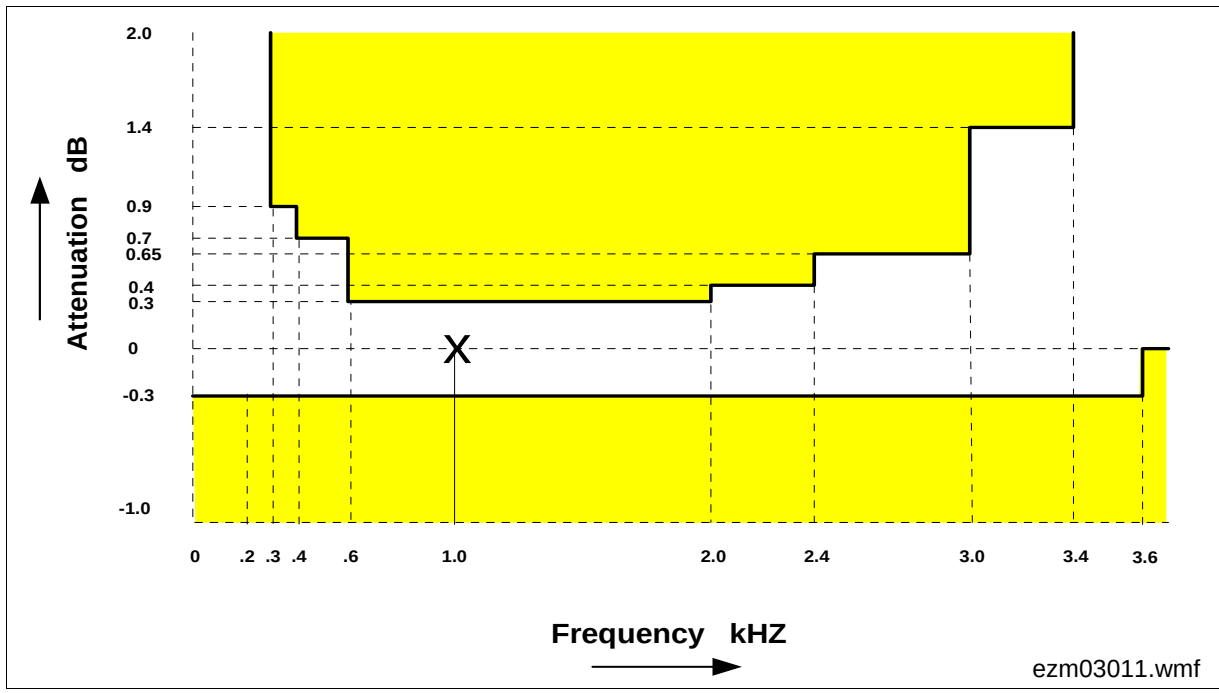


Figure 35 Frequency Response Receive

6.3 Gain Tracking (Receive and Transmit)

The gain deviations stay within the limits in the figures below.

measured with sine wave *f* = 1004 Hz
reference level is – 10 dBm0.

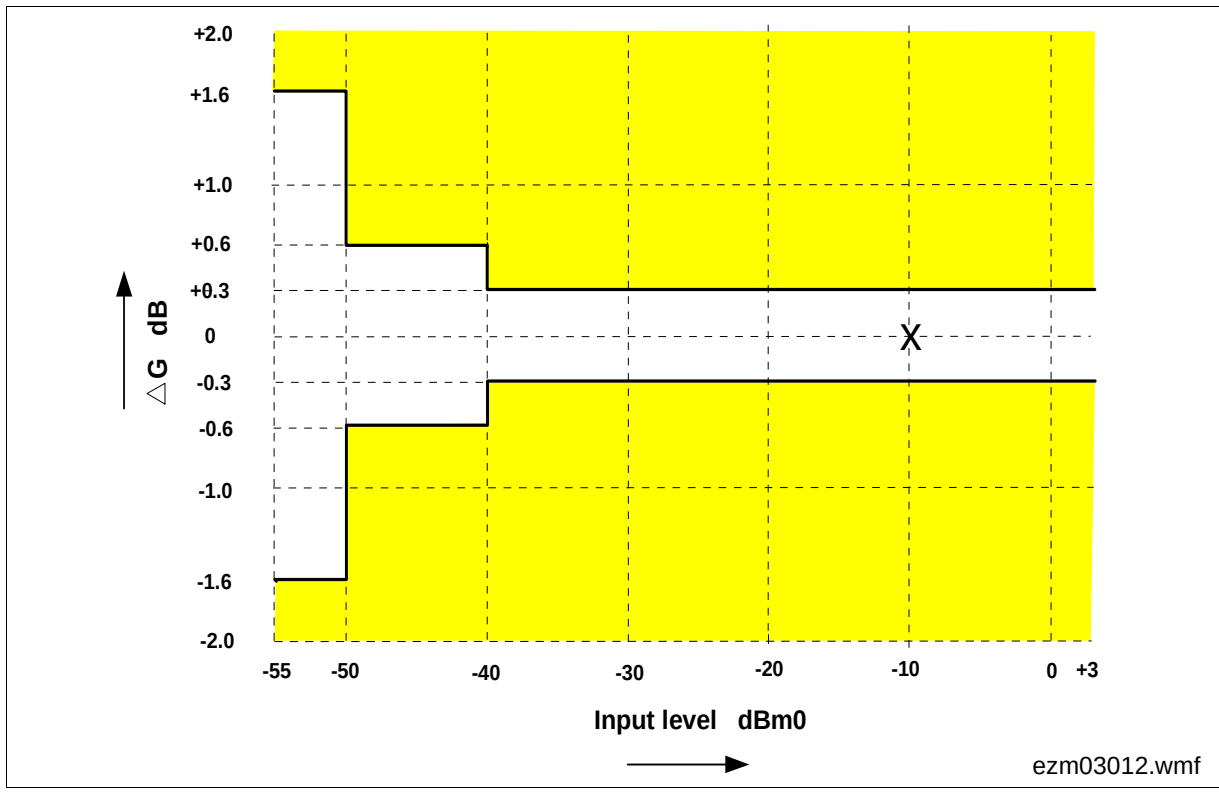


Figure 36 Gain Tracking (Receive and Transmit)

6.4 Group Delay

Maximum delays when the QAP and the MuPP µC are operating with $H_{TH} = H_{IM} = 0$ and $H_{FRR} = H_{FRX} = 1$ including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

Group Delay deviations stay within the limits in the figures below.

Group Delay absolute values: Signal level – 10 dBm0, f_{Test}@T_{Gmin}

Table 14 Group Delay

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Transmit delay	D_{XA}	–	527.5	–	µs	f = 1.5 kHz
Receive delay	D_{RA}	–	437.5	–	µs	f = 1.5 kHz

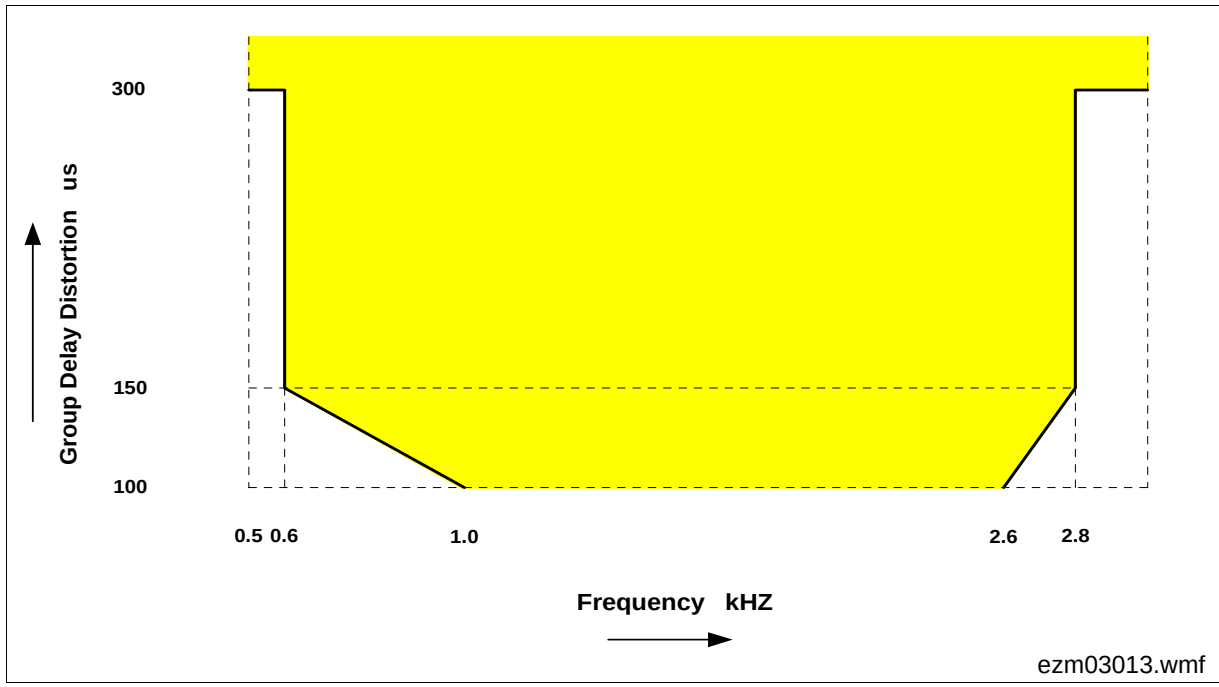


Figure 37 Group Delay Distortion (Receive and Transmit)

6.5 Overload Compression

measured with sine wave *f* = 1004 Hz

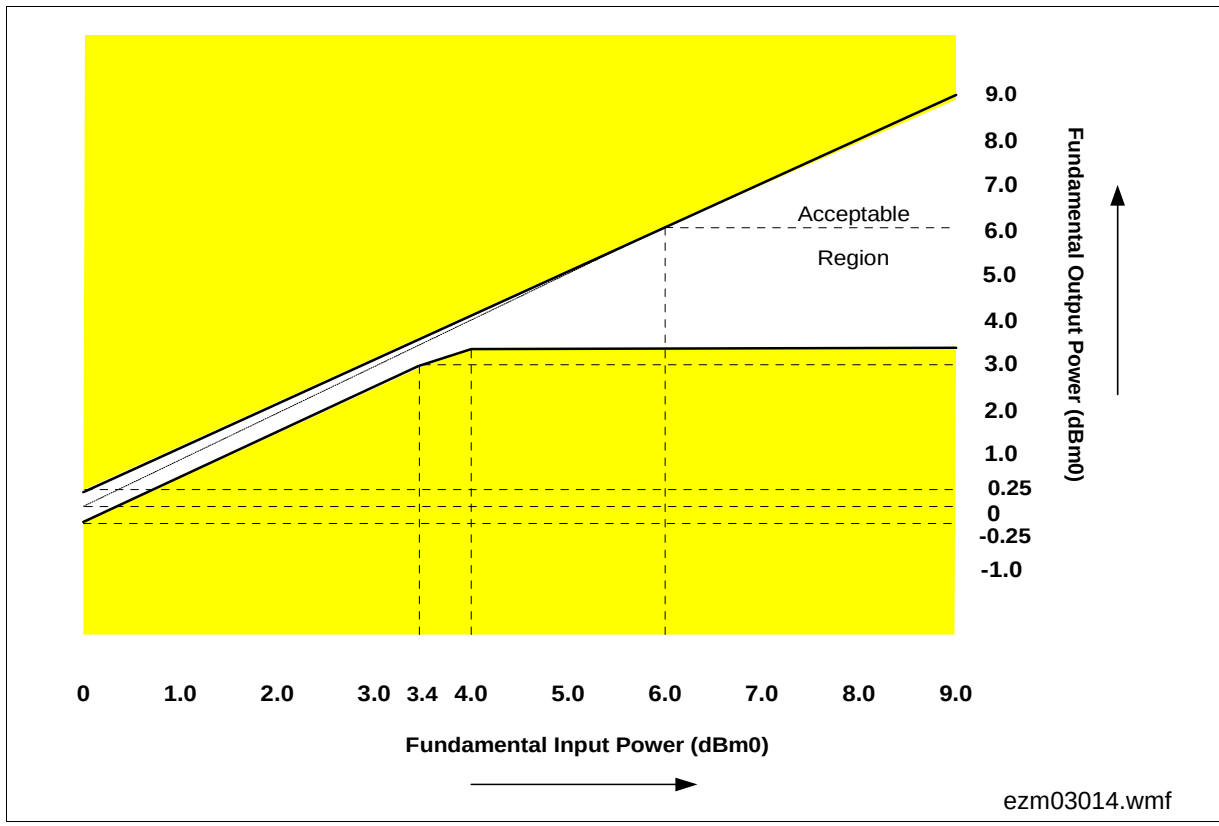


Figure 38 Overload Compression Transmit

6.6 Total Distortion

The signal to distortion ratio exceeds the limits in the following figure:

Receive: measured with sine wave *f* = 1004 Hz. (C-message weighted for µ-law, psophometrically weighted for A–law). The mean relative level is – 7 dBr.

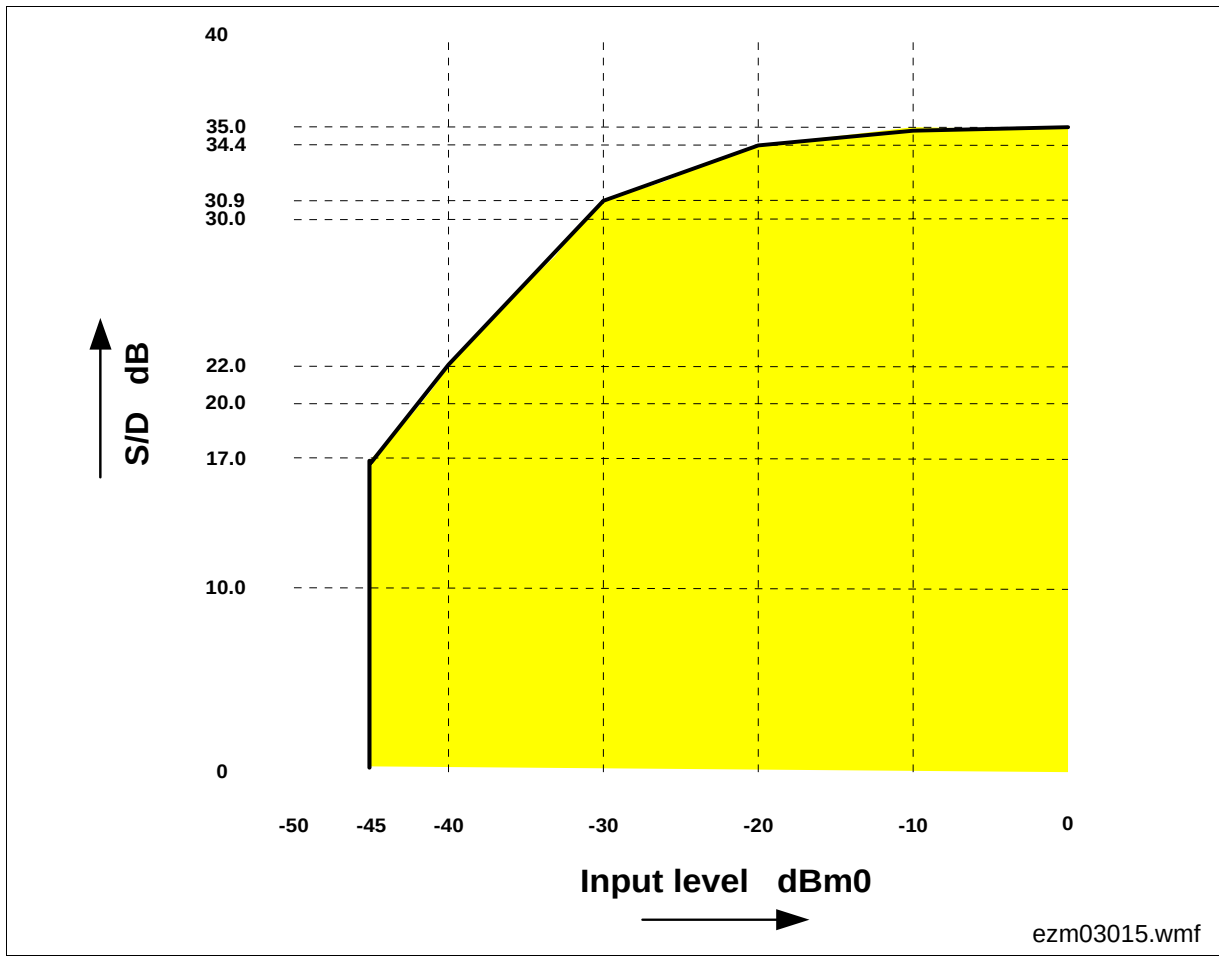


Figure 39 Total Distortion Receive AR = 7 dBr

Transmit: measured with sine wave f = 1004 Hz. (C-message weighted for µ-law, psophometrically weighted for A-law). The mean relative level is 0 dBr.

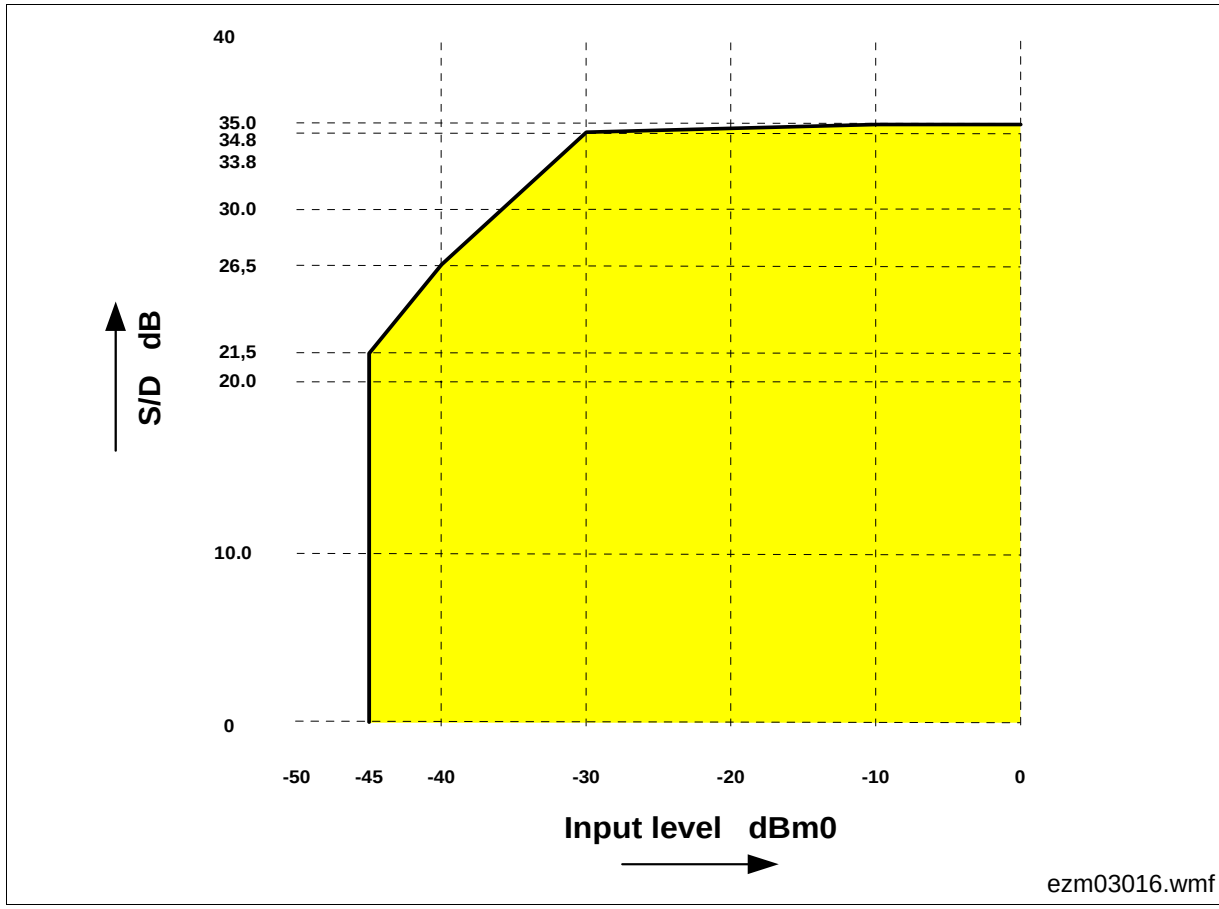
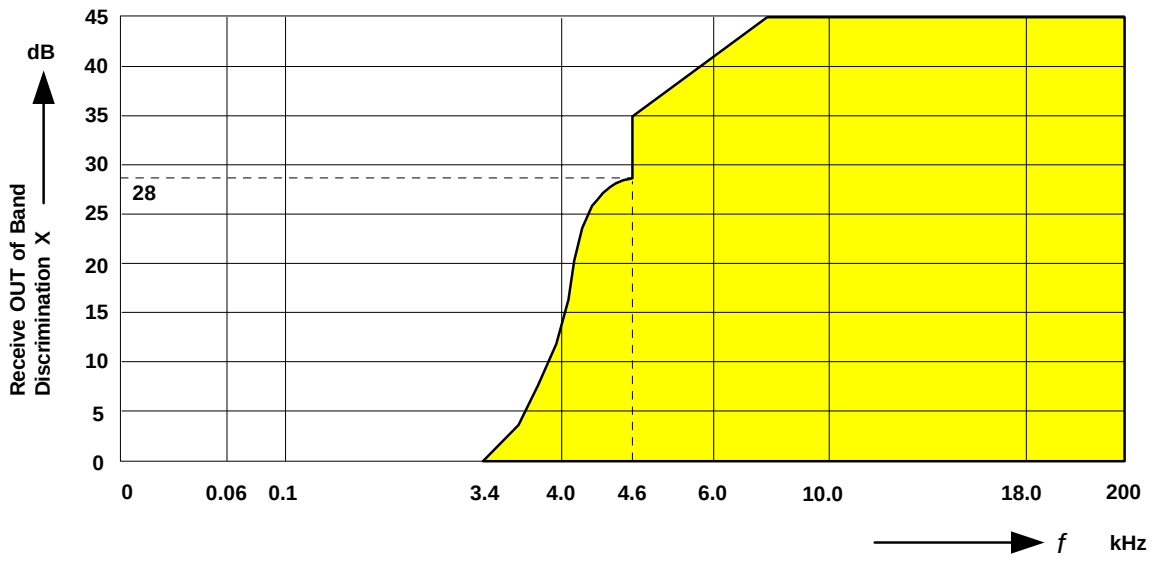


Figure 40 **Total Distortion Transmit** AX = 0 dBr

6.7 Out-of-Band Signals at Analog Output (Receive)

With a 0 dBm0 sine wave with frequency *f* (300 Hz to 3.4 kHz) applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.



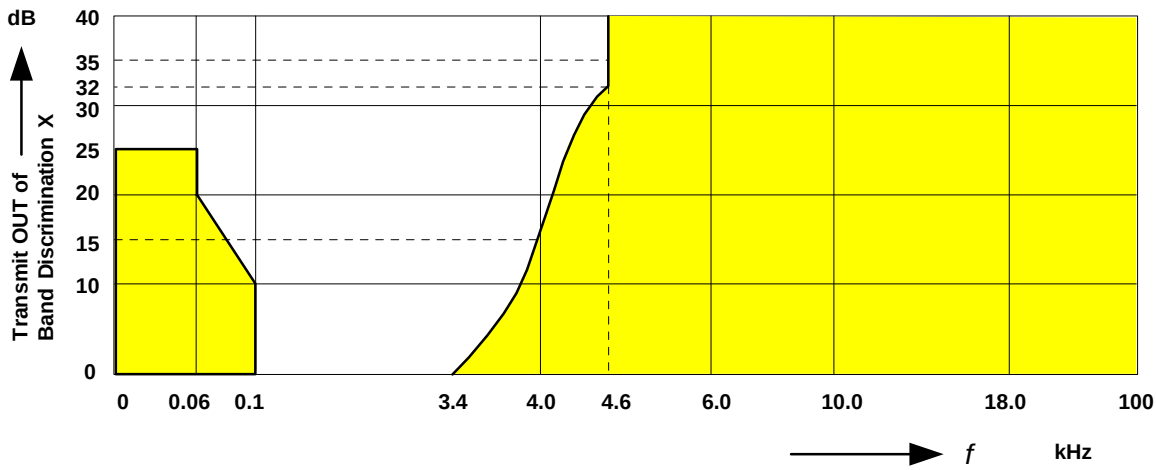
$$3.4 \ldots 4.6\ \text{kHz: } X = -14\left(\sin\left(\pi\frac{4000-f}{1200}\right) - 1\right)$$

itd09762.emf

Figure 41 Out-of-Band Signals at Analog Output (Receive)

6.8 Out-of-Band Signals at Analog Input (Transmit)

With a 0 dBm0 out-of-band sine wave signal with frequency *f* (< 100 Hz or 3.4 kHz to 100 kHz) applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog input. [1)]



$$3.4 \ldots 4.0\ \text{kHz}: X = -14\left(\sin\left(\pi\frac{4000-f}{1200}\right) - 1\right)$$

$$4.0 \ldots 4.6\dot{}\ \text{kHz}: X = -18\left(\sin\left(\pi\frac{4000-f}{1200}\right) - \frac{7}{9}\right)$$

itd09763.emf

Figure 42 Out-of-Band Signals at Analog Input (Transmit)

1) Poles at 12 kHz ± 150 Hz respectively 16 kHz ± 150 Hz and harmonics will be provided

6.9 Out-of-Band Ringing Distortion

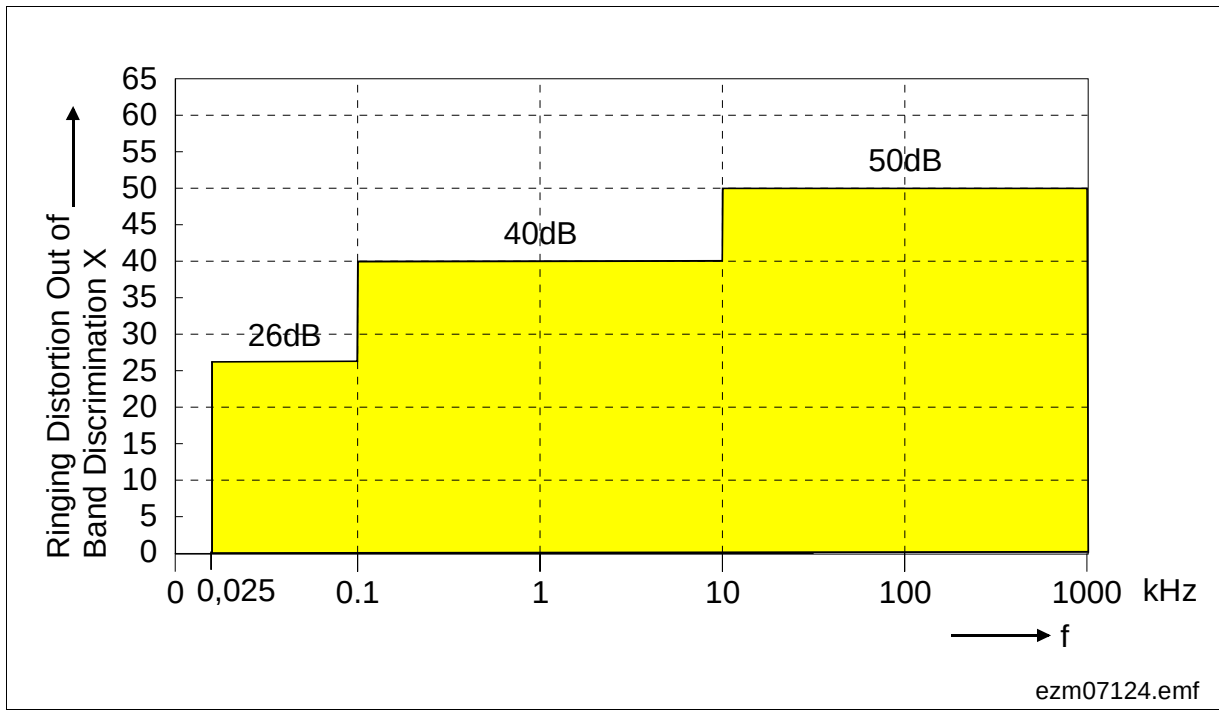


Figure 43 Out-of-Band Ringing Distortion

6.10 Terminal Balance Return Loss

The quality of Transhybrid-Balancing is very sensitive to deviations in gain and group delay – deviations inherent to the MuSLIC A/D- and D/A-converters as well as to all external components used on a line card.

Measurement of MuSLIC transhybrid-loss: A 0dBm0 sine wave signal with a frequency in the range between 300 – 3400 Hz is applied to the digital input.

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below.

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	typ.		
Transhybrid Loss at 500 Hz	THL_{500}	33	50	dB	
Transhybrid Loss at 2500 Hz	THL_{2500}	29	44	dB	
Transhybrid Loss at 3000 Hz	THL_{3000}	27	42	dB	

7 Test Features[1)]

Note: Test functions are not available with MuSLIC-S

Table 15 Levelmeter-Function

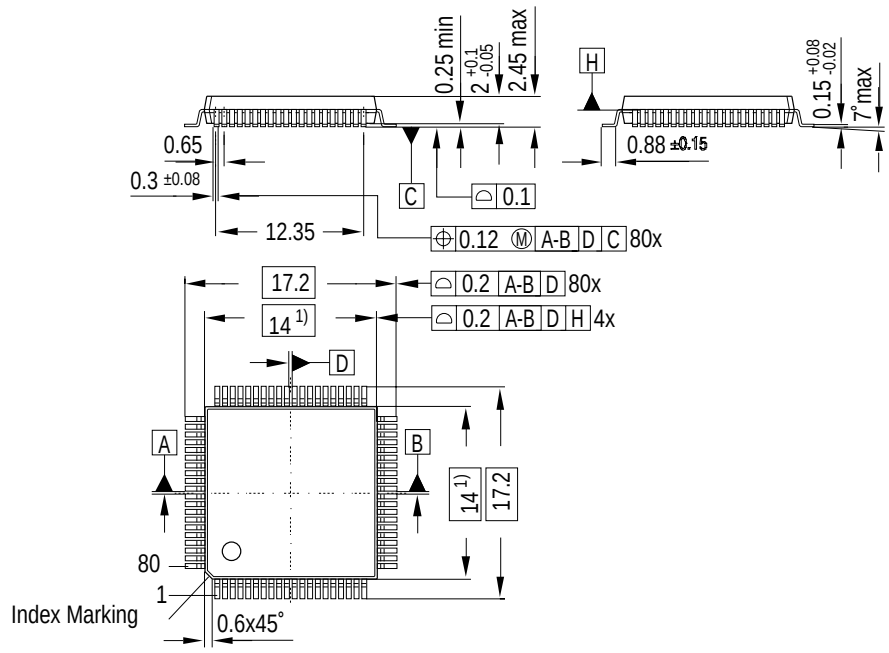
No.	Test	Result	Loops	Settings	Switches	Description
1.	Level metering AC	PCM MVA, RLM0/1	AC Loop	ITIME LMBP LMNOTCH LM2PCM LMSEL0/1 ELM	ENTE on ELM on	After programming the settings and release with the ENTE the levelmetering will be started by ELM = 1. The end of measurement is shown by MVA, RLM0/1 and the result can be sent to the corresponding-voice channel. ITIME determines the Integration time either 16 ms or 256 ms.
2.	Level metering DC	PCM MVA, RLM0/1	DC Loop	LP03, LP5, DISPOFI, PCM2DC DCAD16 ERAMP ERECT LM2PCM LMSEL0/1 ELM f_{RING}	ENTE on ELM on	After programming the settings and release with the ENTE the levelmetering will be started by ELM = 1. The measurement time is programmable using the ring generator. The end of measurement is shown by MVA, RLM0/1 and the result can be sent to the corresponding-voice channel. Includes measurement of Offset, and Ringer Capacitance.
3.	Level metering TTX	PCM MVA, RLM0/1	DC Loop	ELM TTXL LMSEL0/1 LM2PCM PCM2DC	ENTE on ELM on	After programming the settings and release with the ENTE the levelmetering will be started by ELM = 1. The measurement time is programmable by ITIME either 16 ms or 256 ms. The end of measurement is shown by MVA, RLM0/1 and the result can be sent to the corresponding-voice channel. By setting TTXL and correct programming of the IM-Filters the TTX current is measured directly.

1) For detaild information about Line and Board Testing please refer to the Application Note "Line Testing with MuSLIC"

8 Package Outlines

8.1 PEB 3465 (QAP)

P-MQFP-80-1
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusions of 0.25 max per side

gpm05249.ps

Figure 44 Package Outline: PEB 3465 (QAP)

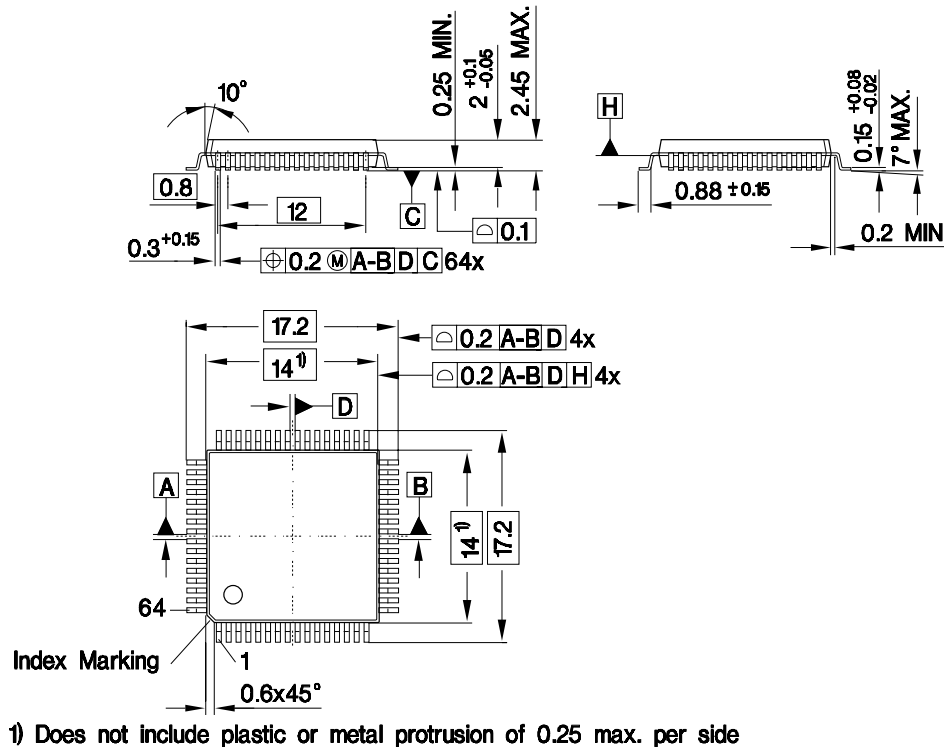
Sorts of Packing
Package outlines for tubes, trays etc. are contained in our data book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

8.2 PEB 31666 / PEB 31664 (MuPP µC)

P-MQFP-64-1
(Plastic Metric Quad Flat Package)



gpm05250.ps

Figure 45 Package Outline: PEB 31666 / PEB 31664 (MuPP µC)

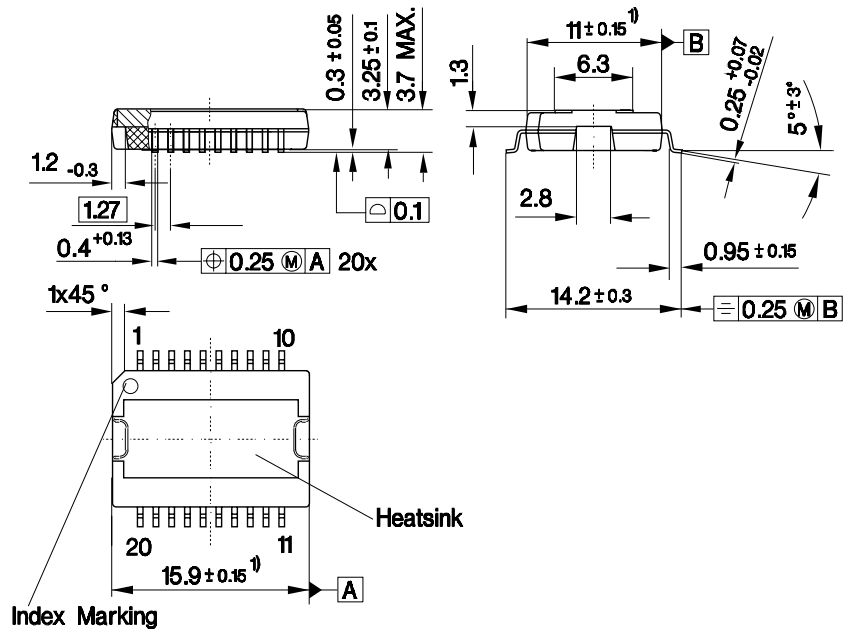
Sorts of Packing
Package outlines for tubes, trays etc. are contained in our data book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

8.3 PEB 4166 / PEB 4164 (AHV-SLIC)

P-DSO-20-5
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side

gpm05755.ps

Figure 46 Package Outline: PEB 4166 / PEB 4164 (AHV-SLIC)

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our data book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

9 Glossary

ACT	Active Mode
ADC	Analog Digital Converter
AGR	Attenuation Receive
AGX	Attenuation Transmit
AHV-SLIC	Advanced High Voltage Subscriber Line Interface Circuit
AR	Attenuation Receive
ASIC	Application Specific Integrated Circuit
AX	Attenuation Transmit
BB	Boosted Battery
C1, C2, C3	Digital Interface between QAP and AHV-SLIC
CMP	Compander
CODEC	Coder Decoder
COMP	Comparator (Testloops, Levelmetering)
COP	Coefficient Operation
CRAM	Coefficient RAM
DAC	Digital Analog Converter
DTAG	Deutsche Telecom AG
DCCHAR	DC Characteristic block
DD	Data Downstream
DSP	Digital Signal Processor
DU	Data Upstream
DUP	Data Upstream Persistency Counter
DUPGNK	Data Upstream Persistency Counter for GNK
EXP	Expander
FRR	Frequency Response Receive Filter
FRX	Frequency Response Transmit Filter
FSC	Frame Sync.
GNK	Ground Key
I1	Fixed Input Pin
IL	Longitudinal Current Input
IO	User Programmable I/O Pin
IT	Transversal Current Input (for AC and DC)

ITAC	Transversal Current Input (for AC)
LP03	Low Pass 0.3 Hz
LP5	Low Pass 5 Hz
LSSGR	Local area transport access Switching System Generic Requirements
MCLK	Master Clock
MuPPµC	Multi Channel Processor for POTS
MuSLIC	Multi Channel Subscriber Line Interface Circuit
MuSLICOS	MuSLIC Oriented Software
O1	Fixed Output Pin
PCM	Pulse Code Modulation
PDN	Power Down
PDN	PDN Pin (Sets the AHV-SLIC to Power Down)
POTS	Plain Old Telephone Service
PREFI	Antialiasing Pre Filter
QAP	Quad Analog POTS
RB	Ring Burst
RES	Reset
RNG	Ring Generator
RREF	External Resistor to GNDA
SCR	Status Configuration Register
SLIC	Subscriber Line Interface Circuit
SLXC	Summary Line Card Outputs
SOP	Status Operation
STCR	Status Test Configuration Register
TCR	Transfer Configuration Register
TST1	Test Pin
TG	Tone Generator
TH	Transhybrid Balancing
THFIX	Transhybrid Balancing Filter (fixed)
TOP	Transfer Operation
TS	Time Slot

TTX	Teletax
VBIM	Battery Image Input
VB/2	Half Battery Voltage Input (programmable Voltage threshold, see also SCR2, bit 7)
X	Transmit Filter (programmable)

Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

http://www.infineon.com

Published by Infineon Technologies AG