

TBB1004

Twin Built in Biasing Circuit MOS FET IC VHF/UHF RF Amplifier

REJ03G0842-1100

Rev.11.00

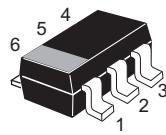
Aug 22, 2006

Features

- Small SMD package CMPAK-6 built in twin BBFET; To reduce using parts cost & PC board space.
- Suitable for World Standard Tuner RF amplifier.
- Very useful for total tuner cost reduction.
- Withstanding to ESD; Built in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; CMPAK-6

Outline

RENESAS Package code: PTSP0006JA-A
(Package name: CMPAK-6)



1. Drain(1)
2. Source
3. Gate-1(1)
4. Gate-1(2)
5. Gate-2
6. Drain(2)

Notes: 1. Marking is "DM".
2. TBB1004 is individual type number of RENESAS TWIN BBFET.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DS}	6	V
Gate1 to source voltage	V _{G1S}	+6 -0	V
Gate2 to source voltage	V _{G2S}	+6 -0	V
Drain current	I _D	30	mA
Channel power dissipation	P _{ch} ³	250	mW
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Note: 3. Value on the glass epoxy board (49mm × 38mm × 1mm).

Electrical Characteristics

(Ta = 25°C)

The below specification are applicable for UHF unit (FET1)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	V _{(BR)DSS}	6	—	—	V	I _D = 200 μA, V _{G1S} = V _{G2S} = 0
Gate1 to source breakdown voltage	V _{(BR)G1SS}	+6	—	—	V	I _{G1} = +10 μA, V _{G2S} = V _{DS} = 0
Gate2 to source breakdown voltage	V _{(BR)G2SS}	+6	—	—	V	I _{G2} = +10 μA, V _{G1S} = V _{DS} = 0
Gate1 to source cutoff current	I _{G1SS}	—	—	+100	nA	V _{G1S} = +5 V, V _{G2S} = V _{DS} = 0
Gate2 to source cutoff current	I _{G2SS}	—	—	+100	nA	V _{G2S} = +5 V, V _{G1S} = V _{DS} = 0
Gate1 to source cutoff voltage	V _{G1S(off)}	0.5	0.7	1.0	V	V _{DS} = 5 V, V _{G2S} = 4 V I _D = 100 μA
Gate2 to source cutoff voltage	V _{G2S(off)}	0.5	0.7	1.0	V	V _{DS} = 5 V, V _{G1S} = 5 V I _D = 100 μA
Drain current	I _{D(op)}	13	17	21	mA	V _{DS} = 5 V, V _{G1} = 5 V V _{G2S} = 4 V, R _G = 100 kΩ
Forward transfer admittance	y _{fs}	21	26	31	mS	V _{DS} = 5 V, V _{G1} = 5 V, V _{G2S} = 4 V R _G = 100 kΩ, f = 1 kHz
Input capacitance	C _{iss}	1.4	1.8	2.2	pF	V _{DS} = 5 V, V _{G1} = 5 V
Output capacitance	C _{oss}	1.0	1.4	1.8	pF	V _{G2S} = 4 V, R _G = 100 kΩ
Reverse transfer capacitance	C _{rss}	—	0.02	0.04	pF	f = 1 MHz
Power gain	PG	16	21	—	dB	V _{DS} = V _{G1} = 5 V, V _{G2S} = 4 V
Noise figure	NF	—	1.7	2.5	dB	R _G = 100 kΩ, f = 900 MHz Z _i = S ₁₁ [*] , Z _o = S ₂₂ ^{*(:PG)} Z _i = S ₁₁ opt (:NF)

Electrical Characteristics (cont.)

(Ta = 25°C)

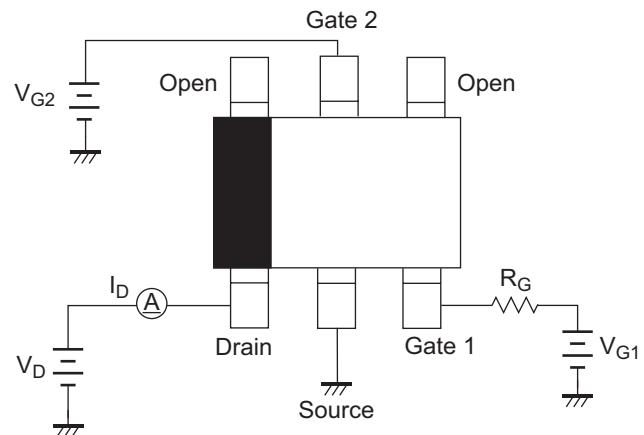
The below specification are applicable for VHF unit (FET2)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200 \mu A, V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10 \mu A, V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	$I_{G2} = +10 \mu A, V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +5 V, V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	$V_{G2S} = +5 V, V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.75	1.0	V	$V_{DS} = 5 V, V_{G2S} = 4 V$ $I_D = 100 \mu A$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.75	1.0	V	$V_{DS} = 5 V, V_{G1S} = 5 V$ $I_D = 100 \mu A$
Drain current	$I_{D(op)}$	16	20	24	mA	$V_{DS} = 5 V, V_{G1} = 5 V$ $V_{G2S} = 4 V, R_G = 100 k\Omega$
Forward transfer admittance	$ y_{fs} $	27	32	37	mS	$V_{DS} = 5 V, V_{G1} = 5 V, V_{G2S} = 4 V$ $R_G = 100 k\Omega, f = 1 kHz$
Input capacitance	C_{iss}	2.3	2.7	3.1	pF	$V_{DS} = 5 V, V_{G1} = 5 V$
Output capacitance	C_{oss}	1.4	1.8	2.2	pF	$V_{G2S} = 4 V, R_G = 100 k\Omega$
Reverse transfer capacitance	C_{rss}	—	0.03	0.05	pF	$f = 1 MHz$
Power gain	PG	24	29	—	dB	$V_{DS} = V_{G1} = 5 V, V_{G2S} = 4 V$
Noise figure	NF	—	1.2	1.7	dB	$R_G = 100 k\Omega, f = 200 MHz$

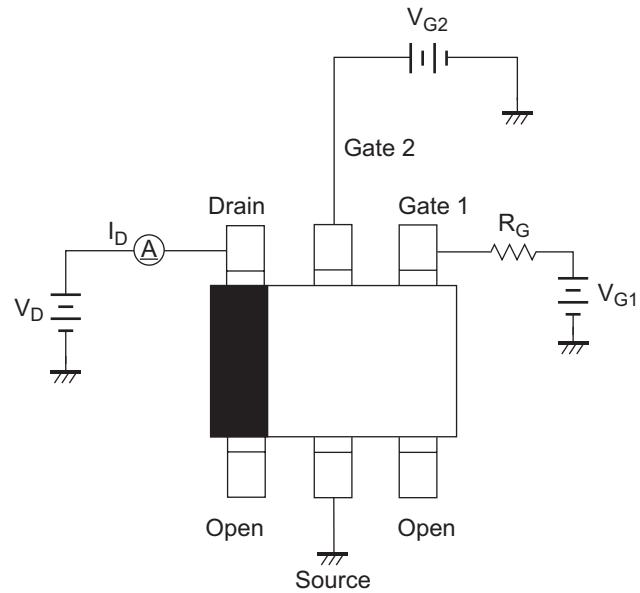
Test Circuits

- DC Biasing Circuit for Operating Characteristic Items ($I_{D(\text{op})}$, $|y_{fs}|$, C_{iss} , C_{oss} , C_{rss} , NF, PG)

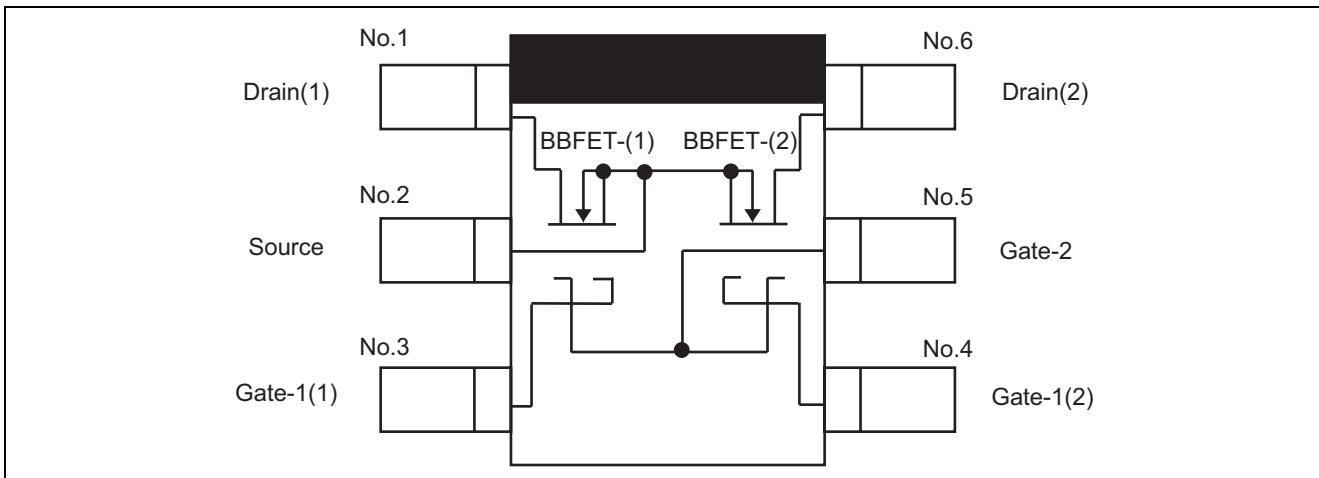
Measurement of FET1



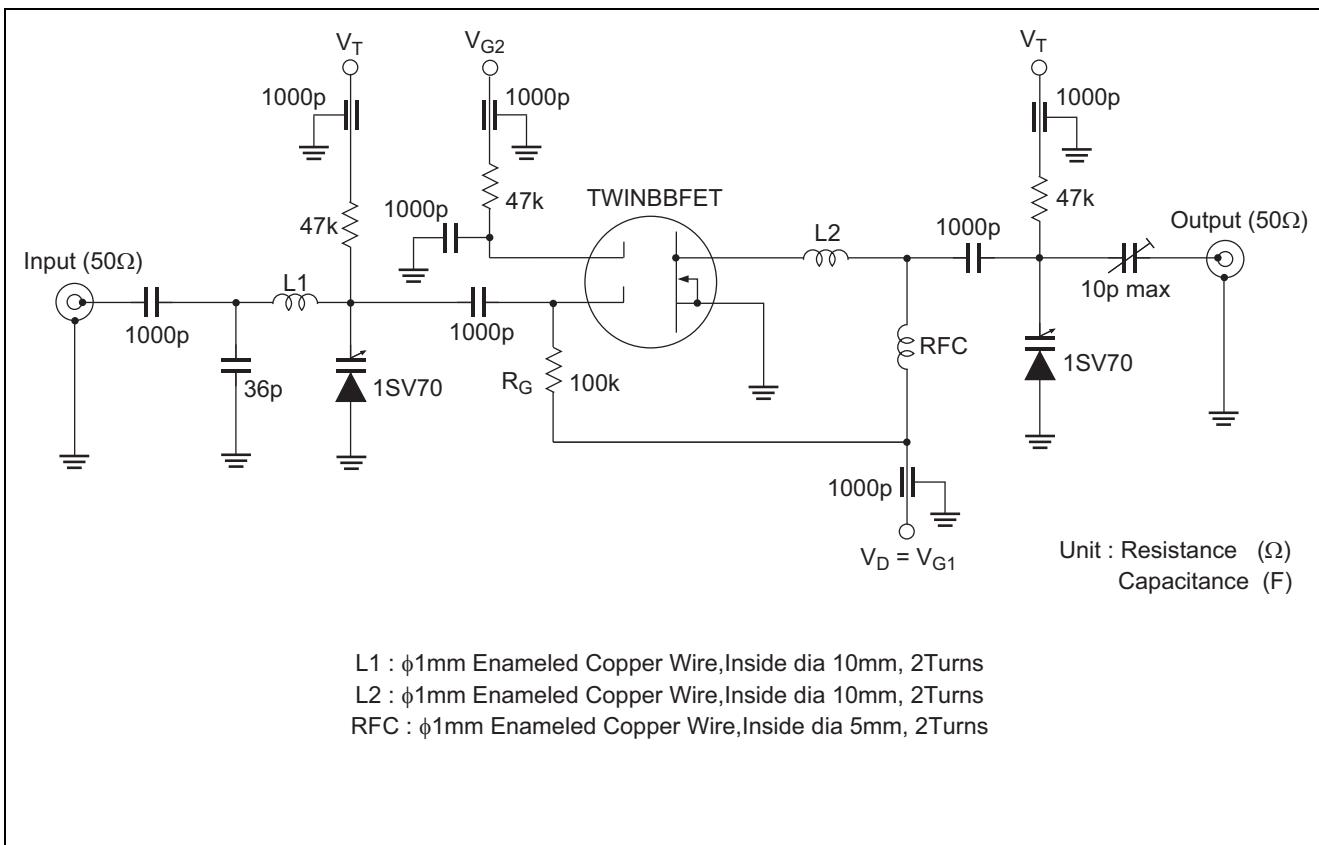
Measurement of FET2

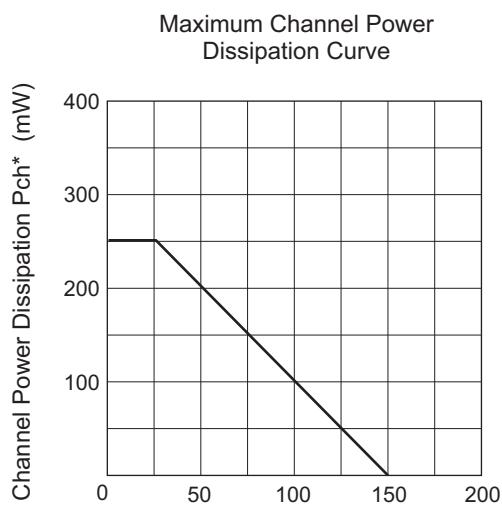


- **Equivalent Circuit**

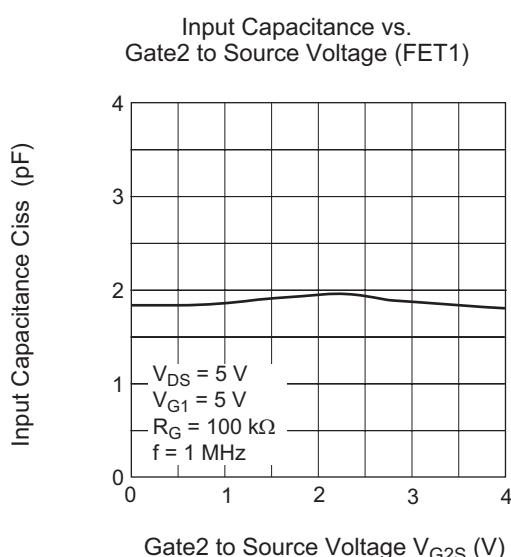
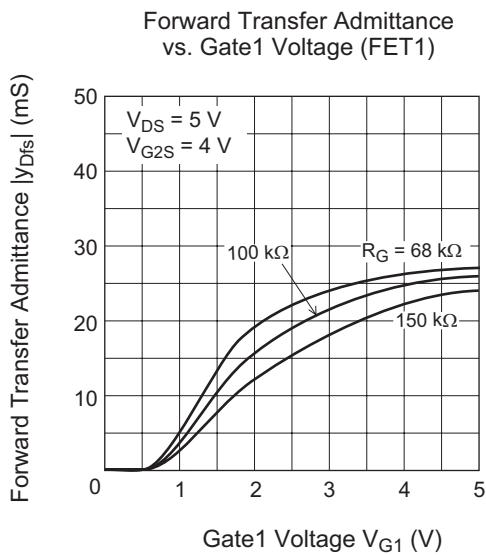
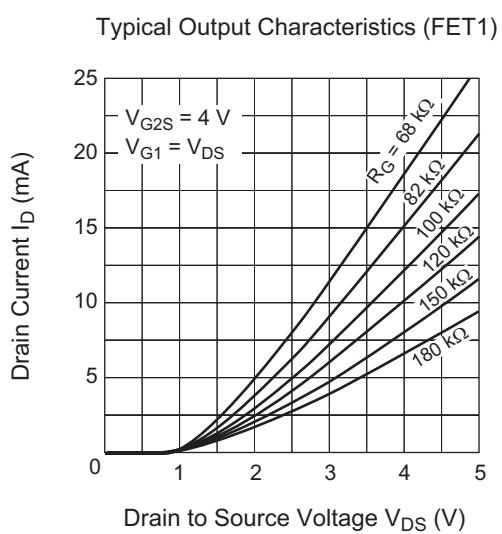
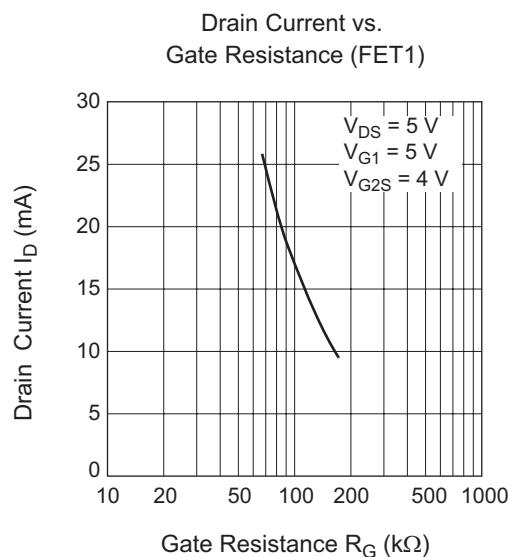
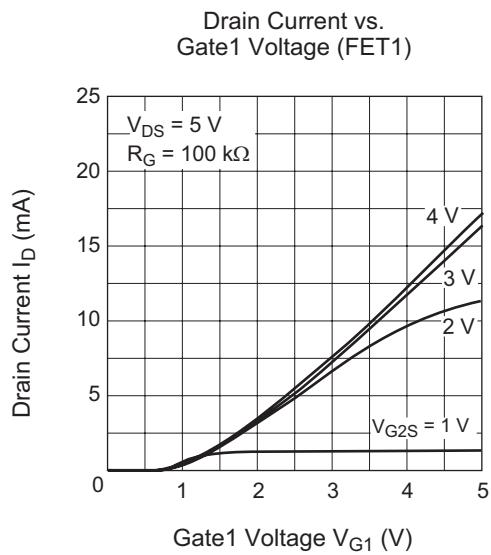


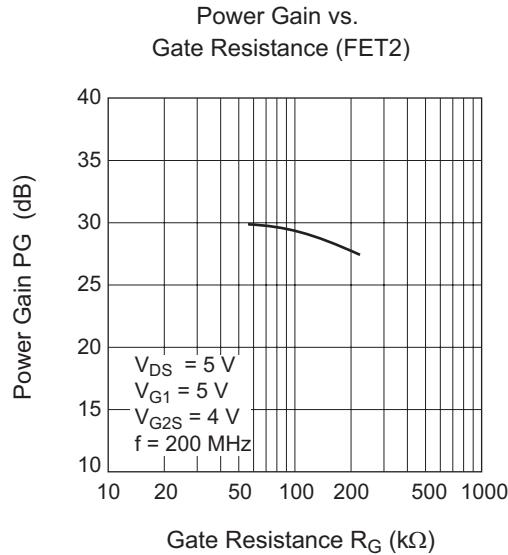
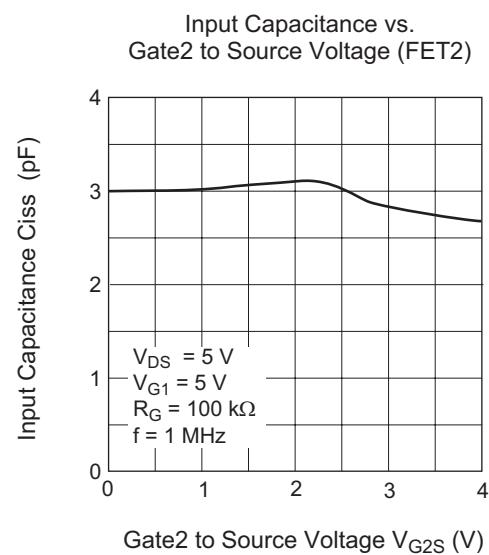
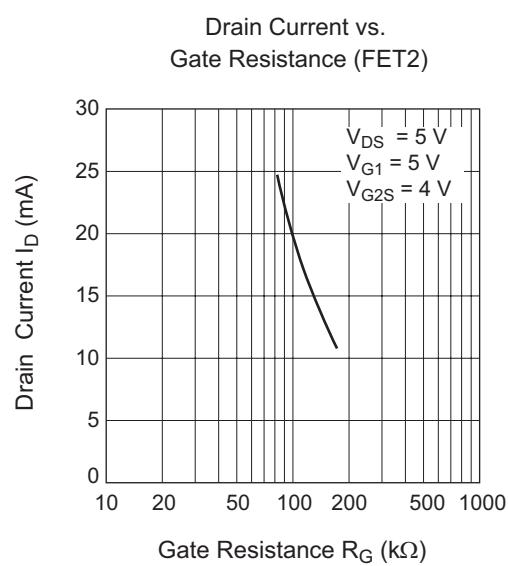
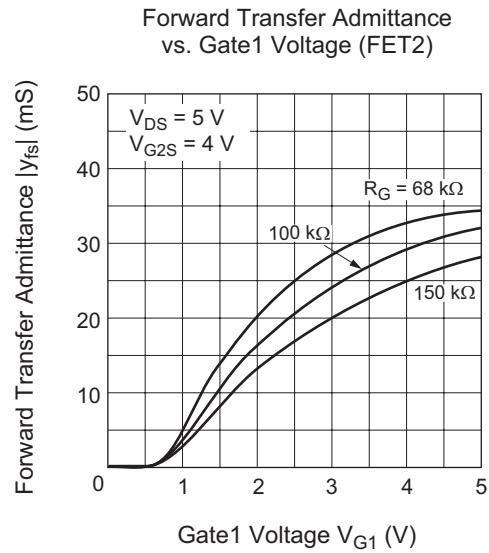
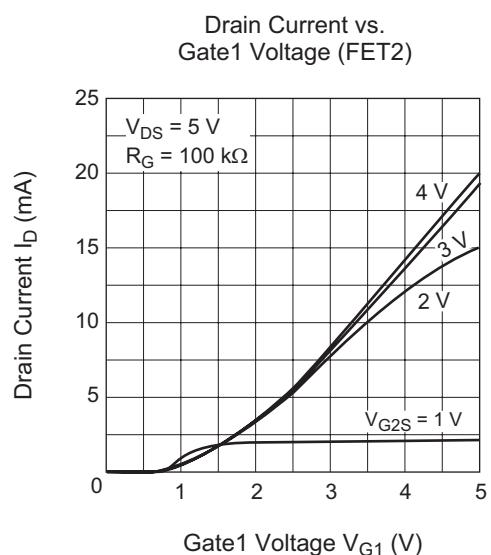
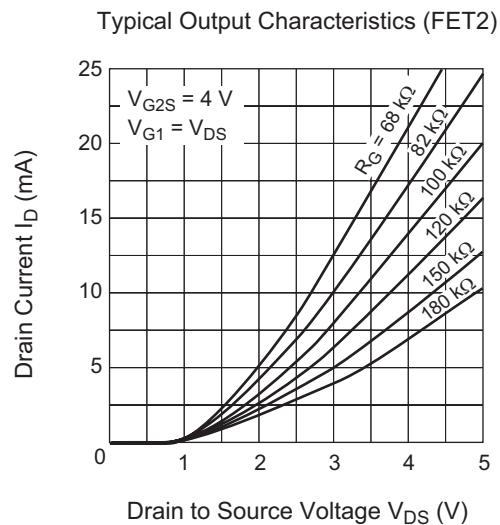
- **200 MHz Power Gain, Noise Figure Test Circuit**

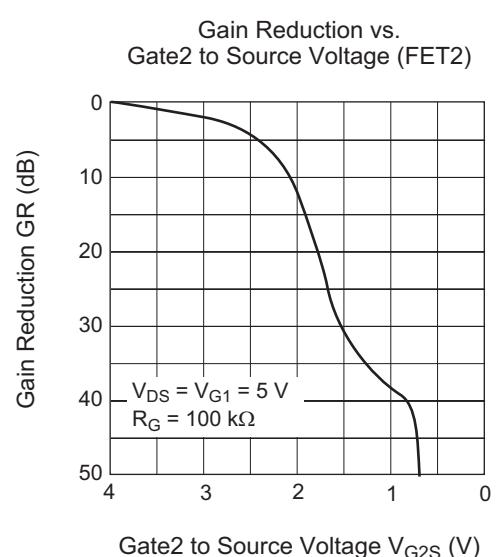
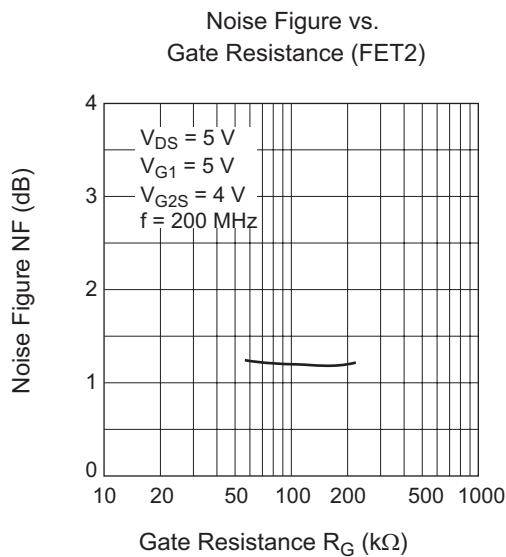




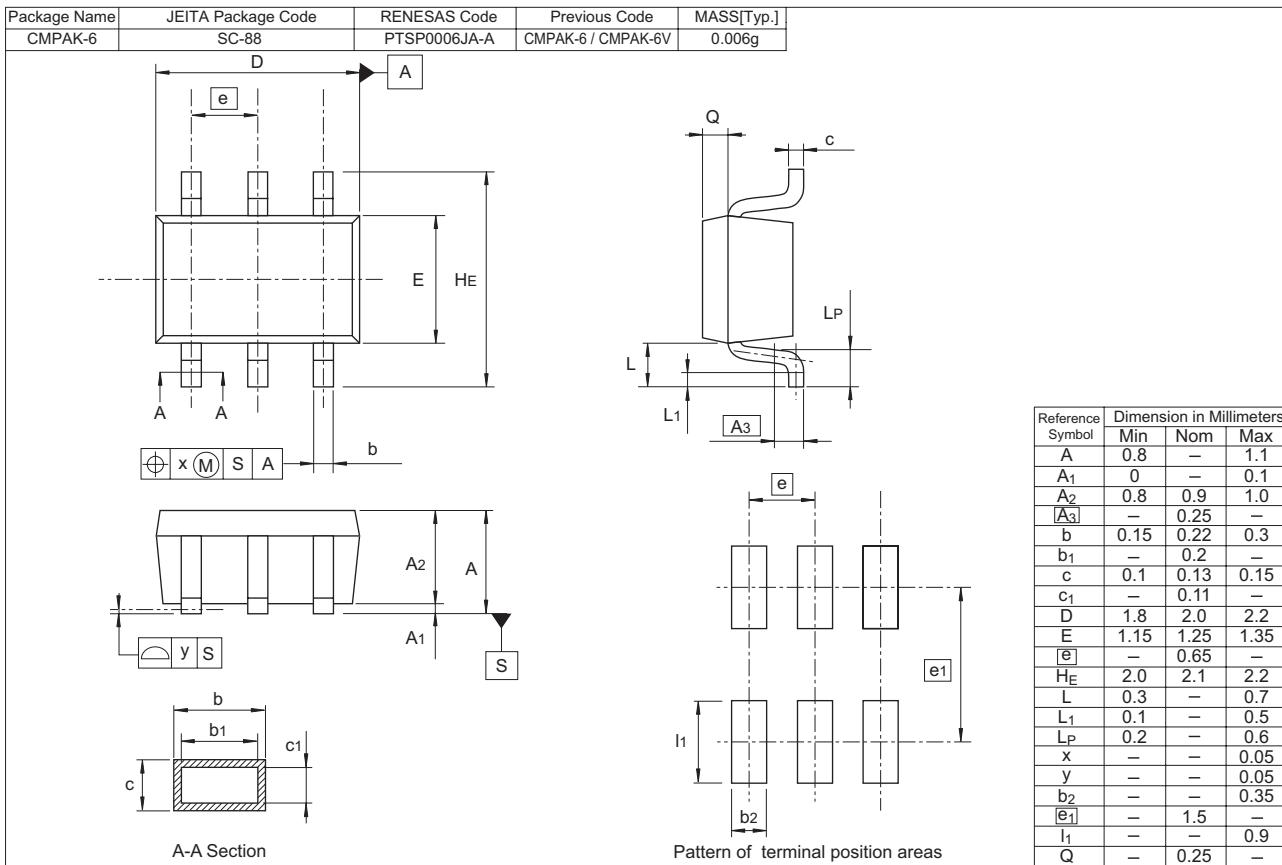
Ambient Temperature T_a (°C)
* Value on the glass epoxy board (49mm × 38mm × 1mm)







Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
TBB1004DMTL-E	3000	Ø 178 mm Reel, 8 mm Emboss Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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