Preliminary

SAB 82289 Bus Arbiter for SAB 80286 Processors

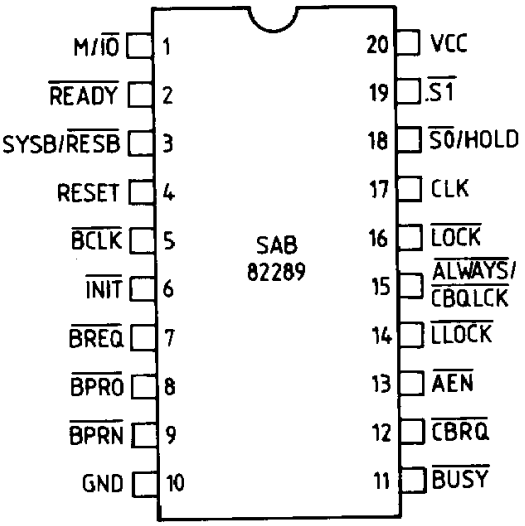
SAB 82289-6 up to 12 MHz

- Supports multimaster system bus arbitration protocol
- Synchronizes SAB 80286 processor with multimaster bus
- Compatible with IEEE 796 standard bus (Multibus®)

SAB 82289 up to 16 MHz

- Three modes of bus release operation for flexible system configuration
- Supports parallel, serial and rotating priority resolving schemes

Pin Configuration



Pin Names

S0/HOLD	Status S0/Hold Input
S1, M/IO	Status Inputs
BUSY	Busy Input/Output
READY	Ready Input
SYSB/RESB	System/Resident Bus
RESET	Processor Reset
BCLK	Bus Clock
INIT	Initialize
BREQ	Bus Request
BPRO	Bus Priority Out
BPRN	Bus Priority In
CLK	System Clock
AEN	Address Enable
ALWAYS/ CBQLCK	Always Release/ Common Bus Request Lock
LLOCK	Level Lock
CBRQ	Common Bus Request
LOCK	Bus Lock
VCC	+5 V
GND	Ground (0 V)

The SAB 82289 Bus Arbiter is a 5 V, 20-pin MYMOS component for use in multiple bus master SAB 80286 systems. The SAB 82289 provides a compact solution to system bus arbitration for the SAB 80286 CPU.

The complete IEEE 796 Standard bus arbitration protocol is supported. Three modes of bus release operation support a number of bus usage models.

Multibus® is a registered trademark of Intel Corporation.

Pin Definitions and Functions

Symbol	Pin	Input (I) Output (O)	Function
M/$\overline{IO}$, $\overline{S1}$	1, 19	I	STATUS INPUTS are the status input signal pins from the SAB 80286 processor. The arbiter decodes these inputs together with the $\overline{S0}$/HOLD input to initiate bus request and surrender actions. A bus cycle is started when either $\overline{S1}$ or $\overline{S0}$ is sampled low at the falling edge of CLK. The SAB 80286's $\overline{S1}$ and M/$\overline{IO}$ pins meet the setup and hold time requirements of these pins. SAB 80286 Bus Cycle Status Encoding M/$\overline{IO}$ | $\overline{S1}$ | $\overline{S0}$/HOLD | Type of Bus Cycle 0 | 0 | 0 | Interrupt acknowledge 0 | 0 | 1 | I/O read 0 | 1 | 0 | I/O write 0 | 1 | 1 | None, bus idle 1 | 0 | 0 | Halt or shutdown 1 | 0 | 1 | Memory read 1 | 1 | 0 | Memory write 1 | 1 | 1 | None, bus idle When supporting the HOLD output of another bus master, the $\overline{S1}$ and M/$\overline{IO}$ pins must be held high during TS, the Status Cycle, for proper operation.
$\overline{READY}$	2	I	$\overline{READY}$ is an active-low signal which indicates the end of the bus cycle. The SAB 80286 halt or shutdown cycle does not require $\overline{READY}$ to terminate the bus cycle. Setup and hold times for this pin must be met for proper operation.
SYSB/$\overline{RESB}$	3	I	SYSTEM BUS/$\overline{RESIDENT\ BUS}$ is an input signal which determines whether the multimaster system bus is required for the current bus cycle. The signal can originate from address mapping circuitry such as a decoder or PROM attached to the processor address and status pins. The arbiter will request or retain control of the multimaster system bus when the SYSB/$\overline{RESB}$ pin is sampled high at the end of the TS bus state. During an interrupt acknowledge cycle, this input is sampled on every falling edge of CLK starting at the end of the TS state until either SYSB/$\overline{RESB}$ is sampled high or the bus cycle is terminated by the $\overline{READY}$ signal. Setup and hold times for this pin must be met for proper operation.
RESET	4	I	PROCESSOR RESET is an active-high input synchronous to the system clock (CLK). RESET is the processsor initialization and an indication to the arbiter to release the multimaster bus and clear any pending request.
$\overline{BCLK}$	5	I	$\overline{BUS\ CLOCK}$ is the multimaster system bus clock to which the multimaster bus interface signals are synchronized. $\overline{BCLK}$ can be asynchronous to CLK.
$\overline{INIT}$	6	I	$\overline{INITIALIZE}$ is an active-low Multibus signal used to reset all arbiters on the Multibus system. It will cause the release of the multimaster bus, but will not clear the pending bus master request so that the arbiter can again request the multimaster bus. No arbiters have the use of the multimaster bus immediately after initialization. $\overline{INIT}$ is an asynchronous signal to CLK.

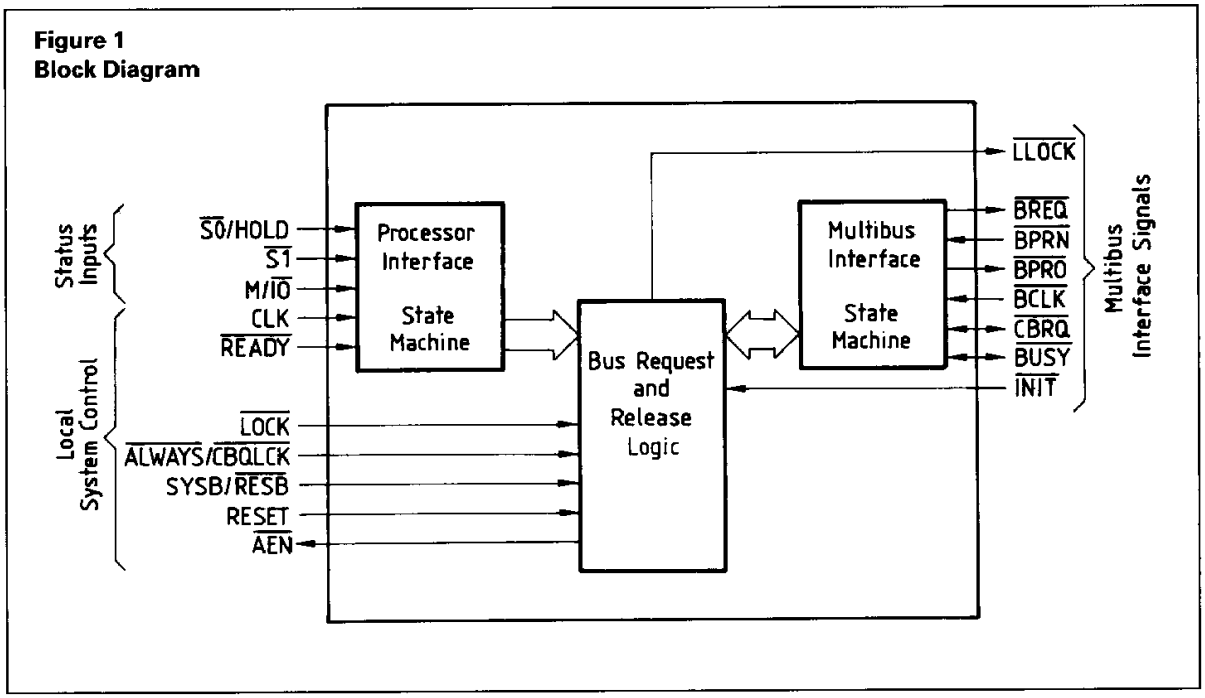
Pin Definitions and Functions (continued)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{BREQ}}$	7	O	$\overline{\text{BUS REQUEST}}$ is an active-low output signal used in the parallel and rotating priority resolving schemes. The arbiter activates $\overline{\text{BREQ}}$ to request the use of the multimaster system bus. The arbiter holds $\overline{\text{BREQ}}$ active as long as it is requesting or has possession of the multimaster system bus.
$\overline{\text{BPRO}}$	8	O	$\overline{\text{BUS PRIORITY OUT}}$ is an active-low output signal used in serial priority resolving scheme. $\overline{\text{BPRO}}$ is connected to $\overline{\text{BPRN}}$ of the next lower priority arbiter to grant or revoke priority from that arbiter.
$\overline{\text{BPRN}}$	9	I	$\overline{\text{BUS PRIORITY IN}}$ is an active-low input indicating that this arbiter has the highest priority of any arbiter requesting the system bus. $\overline{\text{BPRN}}$ high signals the arbiter that a higher priority arbiter is requesting or has possession of the system bus. Setup and hold times for this pin must be met for proper operation.
$\overline{\text{BUSY}}$	11	I/O (open-drain)	$\overline{\text{BUSY}}$ is a Multibus signal which is asserted when the system bus is in use. $\overline{\text{BUSY}}$ is an open drain input/output requiring an external pullup resistor. As an input $\overline{\text{BUSY}}$ asserted indicates when the Multibus is in use. Setup and hold times must be met for proper operation. As an output $\overline{\text{BUSY}}$ is asserted to signal when this arbiter has taken control of the Multibus.
$\overline{\text{CBRQ}}$	12	I/O (open-drain)	$\overline{\text{COMMON BUS REQUEST}}$ is a Multibus signal that indicates when an arbiter is requesting the Multibus. This pin is an open-drain input/output requiring an external pullup resistor. As an input $\overline{\text{CBRQ}}$ indicates that another arbiter is requesting the multimaster system bus. The input function of this pin is enabled by the $\overline{\text{CBQLCK}}$ signal. Setup and hold times for this pin must be met for proper operation. As an output $\overline{\text{CBRQ}}$ is asserted to indicate that this arbiter is requesting the Multibus. The arbiter pulls $\overline{\text{CBRQ}}$ low when it issues $\overline{\text{BREQ}}$. The arbiter releases $\overline{\text{CBRQ}}$ when it obtains the Multibus.
$\overline{\text{AEN}}$	13	O	$\overline{\text{ADDRESS ENABLE}}$ is the output of the arbiter which goes directly to the processor's address latches, the SAB 82288 bus controller and the SAB 82284 clock generator. $\overline{\text{AEN}}$ asserted causes the bus controller and address latches to enable their output drivers. $\overline{\text{AEN}}$ also drives the clock generator's $\overline{\text{ARDYEN}}$ input to enable its asynchronous ready input ($\overline{\text{ARDY}}$). $\overline{\text{AEN}}$ can also be used as an active-low hold acknowledge to a bus master other than the SAB 80286. It signals to the bus master that control of the system bus has been relinquished when $\overline{\text{AEN}}$ is inactive (high). Note that $\overline{\text{AEN}}$ goes active relative to $\overline{\text{BCLK}}$ and goes inactive relative to CLK.

Pin Definitions and Functions (continued)

Symbol	Pin	Input (I) Output (O)	Function
$\overline{\text{LLOCK}}$	14	O	$\overline{\text{LEVEL LOCK}}$ is an active-low output signal decoded from the processor $\overline{\text{LOCK}}$ signal. $\overline{\text{LLOCK}}$ can be used as Multibus $\overline{\text{LOCK}}$ when buffered with a tri-state buffer enabled by the $\overline{\text{AEN}}$ signal. $\overline{\text{LLOCK}}$ will be cleared by RESET but not by $\overline{\text{INIT}}$.
$\overline{\text{ALWAYS}}$/ $\overline{\text{CBQLCK}}$	15	I	$\overline{\text{ALWAYS RELEASE}}$ or $\overline{\text{COMMON BUS REQUEST LOCK}}$ can be programmed at processor reset to be either the ALWAYS RELEASE ($\overline{\text{ALWAYS}}$) strapping option or the COMMON BUS REQUEST LOCK ($\overline{\text{CBQLCK}}$) control input. Setup and hold times for this pin must be met for proper programming. When this pin is low during the falling edge of processor reset ($\overline{\text{ALWAYS}}$ option) the arbiter is programmed to surrender the multimaster system bus after each bus transfer cycle. The SAB 82289 will remain in the ALWAYS RELEASE mode until it is reprogrammed during the next processor reset. The bus arbiter is programmed to support the COMMON BUS REQUEST LOCK function by forcing this input pin high during the falling edge of the processor reset. $\overline{\text{CBQLCK}}$ itself is an active-low signal which when active prevents the arbiter from surrendering the multimaster system bus to a common bus request through the $\overline{\text{CBRQ}}$ input pin.
$\overline{\text{LOCK}}$	16	I	$\overline{\text{LOCK}}$ is a processor-generated signal which when asserted (low) prevents the arbiter from surrendering the multimaster system bus to any other bus arbiter, regardless of its priority. $\overline{\text{LOCK}}$ is sampled by the arbiter at the end of the TS (status) bus state. Setup and hold times for this pin must be met for proper operation.
CLK	17	I	SYSTEM CLOCK accepts the CLK signal from the SAB 82284 clock generator chip as the timing reference for the bus arbiter and processor interface signals.
$\overline{\text{S0}}$/HOLD	18	I	STATUS INPUT $\overline{\text{S0}}$ or HOLD is either the $\overline{\text{S0}}$ status signal from the SAB 80286 or the HOLD signal from some other bus master. The function of this input is established during the processor reset of the SAB 82289 bus arbiter. The SAB 80286 $\overline{\text{S0}}$ pin meets the setup and hold time requirements of this pin. The $\overline{\text{S0}}$ pin function is selected by forcing this input high during the falling edge of processor reset if the SAB 82289 is used to support an SAB 80286 processor, the $\overline{\text{S0}}$ output of the processor will be high during reset. In supporting the SAB 80286 processor, the SAB 82289 decodes the $\overline{\text{S0}}$ pin together with the other status input $\overline{\text{S1}}$ and M/$\overline{\text{IO}}$ to determine the beginning of a processor bus cycle and initiate bus request and surrender actions. The HOLD function of the $\overline{\text{S0}}$/HOLD pin is selected by holding this input low during the falling edge of processor reset. When supporting a bus master other than SAB 80286 the SAB 82289 monitors the HOLD signal to initiate bus request and surrender actions.
VCC	20	–	POWER SUPPLY (+5V)
GND	10	–	GROUND (0V)

Figure 1
Block Diagram



Functional Description

The SAB 82289 bus arbiter in conjunction with the SAB 82288 bus controller and the SAB 82284 clock generator interfaces the SAB 80286 processor or some other bus master to a multimaster system bus. The arbiter multiplexes a processor to a multimaster system bus. It avoids contention with other bus masters.

The SAB 82289 has two separate state machines which communicate through bus request and release logic. The processor interface state machine is synchronous with the local system clock (CLK) and the multimaster system bus interface state machine is synchronous with the bus clock ($\overline{BCLK}$).

The SAB 82289 performs all signaling to request, obtain, and release the system bus. External logic is used to determine which bus cycles require the system bus and to resolve priorities of simultaneous requests for control of the system bus.

SAB 82289 with SAB 80286

In a SAB 80286 system using a SAB 82289 bus arbiter, the SAB 80286 processor is unaware of the arbiter's existence and issues commands as though it had exclusive use of a multimaster system bus, such as Multibus. If the processor cycle requires Multibus access, the arbiter requests control of the Multibus. Until the request is granted the SAB 82289 keeps $\overline{AEN}$ disabled to prevent the SAB 82288 bus controller and the address latches from accessing the Multibus. $\overline{AEN}$ inactive also disasserts the asynchronous ready enable ($\overline{ARDYEN}$) input of the SAB 82284 clock chip so that the system bus will appear as "NOT READY" to the SAB 80286 processor.

Once the SAB 82289 bus arbiter has acquired the bus, it will assert $\overline{AEN}$ allowing the SAB 82288 bus controller and the address latches to access the system bus and asserting the $\overline{ARDYEN}$ input of the SAB 82284 clock chip.

Typically, once the data transfer command has been issued by the SAB 82288 and the data transfer has taken place, a transfer acknowledge ($\overline{XACK}$) signal is returned to the processor on the multimaster system bus to indicate "READY" from the accessed slave device. The processor remains in a series of "wait states" (repeated TC states) until the addressed device responds with $\overline{XACK}$ asserted signal to the SAB 82284's $\overline{ARDY}$ input and the SAB 82284 asserts $\overline{READY}$ to the processor. The processor then completes its bus cycle.

SAB 82289 with Other Bus Masters

When supporting other bus masters, the $\overline{S0}$/HOLD and $\overline{READY}$ pins of the bus arbiter can be connected to the "hold" pin of that master. The inverted $\overline{AEN}$ signal from the SAB 82289 can be used as the hold acknowledge (HLDA) input for the other bus master.

The bus master sends a HOLD signal to the bus arbiter when it needs the system bus for a memory access. If the arbiter currently controls the system bus, $\overline{AEN}$ will be active. Otherwise $\overline{AEN}$ will be inactive and the arbiter will request control of the system bus. The bus master will have to wait until the SAB 82289 has asserted $\overline{AEN}$ (low) before it starts its bus cycle.

When the bus master no longer requires the Multibus it will have to inactivate the HOLD signal. The arbiter interprets the Multibus access as a single bus cycle which is terminated by HOLD going inactive (low). Thus the arbiter will not release the Multibus to any other bus master during a bus access cycle.

Processor Cycle Definition

Any SAB 80286 system which gains access to the Multibus through the SAB 82289 bus arbiter uses an internal clock which is one half the frequency of the system clock (CLK) (see figure 2). Knowledge of the phase of the local bus master internal clock is required for proper SAB 82289 control of the SAB 80286 interface to Multibus. The local bus master informs the bus arbiter of its internal clock phase when it asserts the status signals. The SAB 80286's $\overline{S0}$ and $\overline{S1}$ status signals are always first asserted in phase 1 of the local bus master's internal clock.

Bus State Definition

The SAB 82289 bus arbiter has three processor bus states (see figure 3): idle (TI), status (TS), command (TC). Each bus state is two CLK cycles long. Bus state phases correspond to the internal CPU clock phases.

Figure 2
CLK Relationship to Internal Processor Phase, and Bus T-States

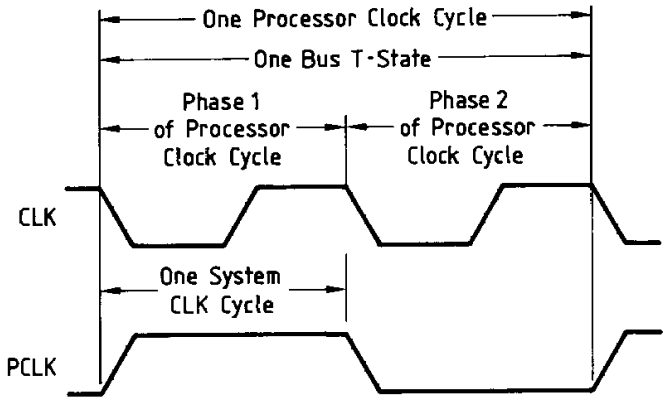
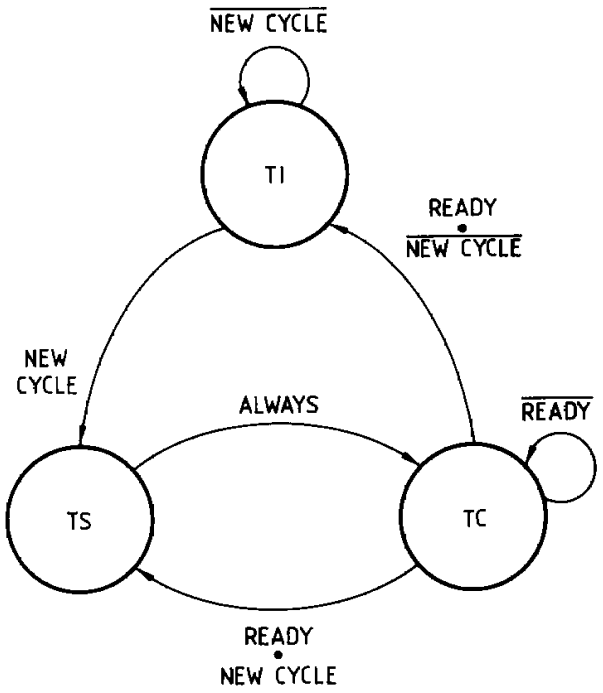


Figure 3
SAB 82289 Processor Bus States



Bus Cycle Definition

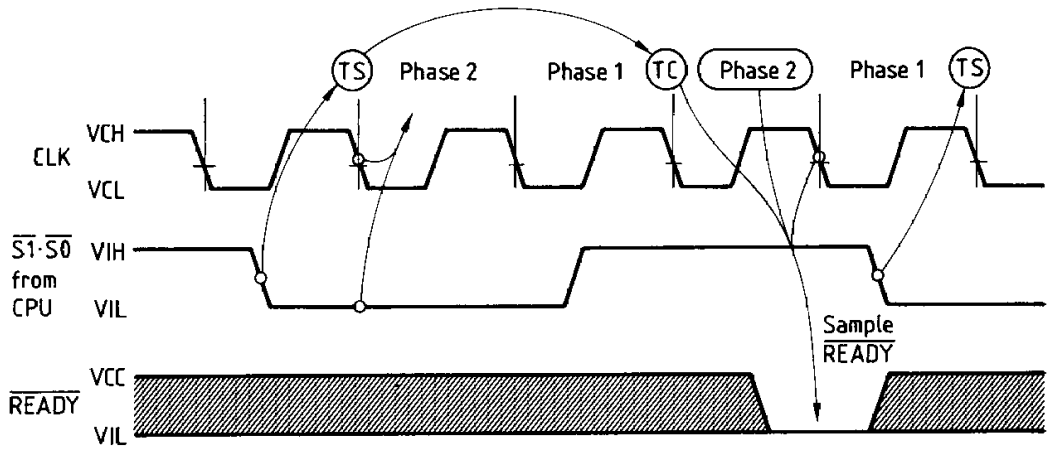
The $\overline{S1}$ and $\overline{S0}$ status inputs are sampled by the SAB 82289 on the falling edge of CLK and signal the start of a bus cycle by going active (low). The TS bus state is defined to be the two CLK cycles during which either $\overline{S1}$ or $\overline{S0}$ is active (see figure 4). When either $\overline{S1}$ or $\overline{S0}$ is sampled low, the next CLK cycle is considered the second phase of the associated processor clock cycle.

The arbiter enters the TC bus state after the TS state. The shortest bus cycle may have one TS state and one TC state. Longer bus cycles are formed by repeating TC states. A repeated TC bus state is called a wait state.

The $\overline{READY}$ input determines whether the current TC bus state is to be repeated. The $\overline{READY}$ input has the same timing and effect for all bus cycles. $\overline{READY}$ is sampled at the end of each TC bus state to see if it is active. If sampled high, the TC bus state is repeated. This is called inserting a wait state.

When $\overline{READY}$ is sampled low, the current bus cycle is terminated. Note that the bus arbiter may enter the TS bus state directly from TC if the status lines are sampled active (low) at the next falling edge of CLK (see figure 4). If neither of the status lines is sampled active at that time the SAB 82289 will enter the TI bus state. The TI bus state will be repeated until the status inputs are sampled active.

Figure 4
SAB 80286 Bus Cycle Definition (without Wait States)



Arbitration between Bus Masters

The Multibus protocol allows multiple processing elements to compete with each other to access common system resources. Since the local SAB 80286 processor does not have exclusive use of the system bus, if the Multibus is "BUSY" the SAB 80286 processor will have to wait before it can access the system bus.

The SAB 82289 bus arbiter provides an integrated solution for controlling access to a multimaster system bus. The bus arbiter allows both higher and lower priority bus masters to acquire the system bus depending on which release mode is used. In general higher priority masters obtain the bus immediately after any lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus or the proper surrender conditions exist. The SAB 82289 handles this arbitration in a manner completely transparent to the bus master (e.g. SAB 80286 processor).

At the end of each transfer, the arbiter may retain or release the system bus. This decision is controlled by the processor state, bus arbitration inputs and arbiter strapping options (see releasing the Multibus, ahead).

Priority Resolving Techniques

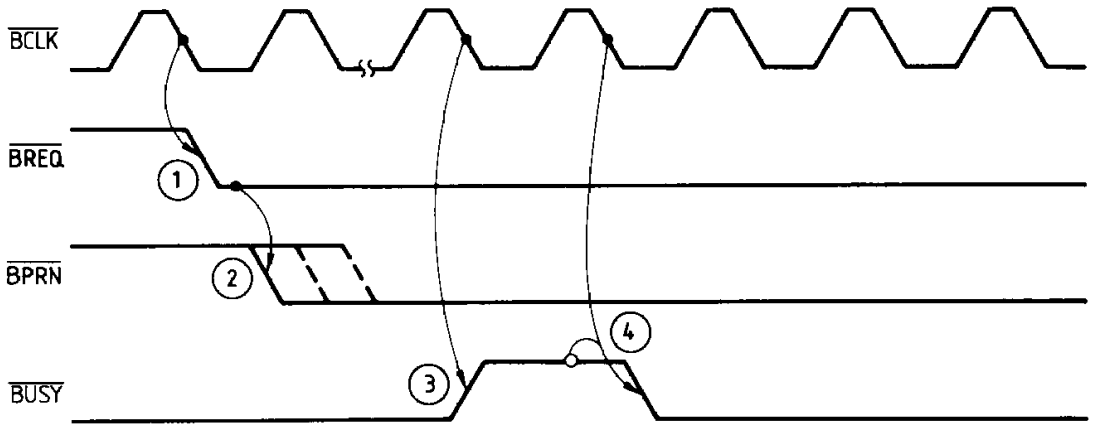
Some means of resolving priority between bus masters requesting the multimaster bus simultaneously must be provided. The SAB 82289 bus arbiter supports parallel, serial and rotating system bus priority resolving techniques. All of these techniques are based on the concept that, at a given time, one bus master will have priority above all the others.

An individual arbiter is the highest priority arbiter requesting the Multibus when its $\overline{\text{BPRN}}$ input is asserted (low). The highest priority requesting arbiter cannot immediately seize the system bus. It must wait until the present bus transaction is completed. Upon completing its current transaction the present bus owner surrenders the bus by releasing $\overline{\text{BUSY}}$.

$\overline{\text{BUSY}}$ is an active-low "wired OR" Multibus signal connecting all bus arbiters on the system bus. When $\overline{\text{BUSY}}$ goes inactive, the arbiter which has requested the system bus and presently has bus priority ($\overline{\text{BPRN}}$ low), seizes the bus by pulling $\overline{\text{BUSY}}$ low (see waveform in figure 5).

The generation of a multimaster bus request ($\overline{\text{BREQ}}$) is controlled by the type of bus cycle and the SYSB/$\overline{\text{RESB}}$ input. Whenever the processor signals the status for memory read, memory write, I/O read,

Figure 5
Bus Exchange Timing for the Multibus



(1) Higher Priority Bus Arbiter Requests the Multimaster System Bus
(2) Attains Priority. (Does not Yet Own Bus).
(3) Lower Priority Bus Arbiter Releases $\overline{\text{BUSY}}$.
(4) Higher Priority Bus Arbiter then Acquires the Bus and Pulls $\overline{\text{BUSY}}$ Low.

I/O write or interrupt acknowledge cycle, and SYSB/$\overline{\text{RESB}}$ is high at the end of TS, a bus request is generated.

When the status inputs indicate an interrupt acknowledge bus cycle, the arbiter allows external logic to decide (through the SYSB/$\overline{\text{RESB}}$ input) whether the interrupt acknowledge cycle should use the Multibus.

Figure 6 shows how SYSB/$\overline{\text{RESB}}$ is repeatedly sampled until it is sampled high or the bus cycle is terminated. If the bus cycle is completed ($\overline{\text{READY}}$ is sampled low) before SYSB/$\overline{\text{RESB}}$ is sampled high, the arbiter will not request the Multibus.

The SAB 82289 bus arbiter does not generate a separate $\overline{\text{BREQ}}$ for each bus cycle. Instead the SAB 82289 generates $\overline{\text{BREQ}}$ when it requests the bus and holds $\overline{\text{BREQ}}$ active during the time that it has possession of the bus. Note that all multimaster system bus requests (via $\overline{\text{BREQ}}$) are synchronized to the system bus clock ($\overline{\text{BCLK}}$).

Figure 6
Bus Request Timing During an Interrupt Acknowledge Cycle

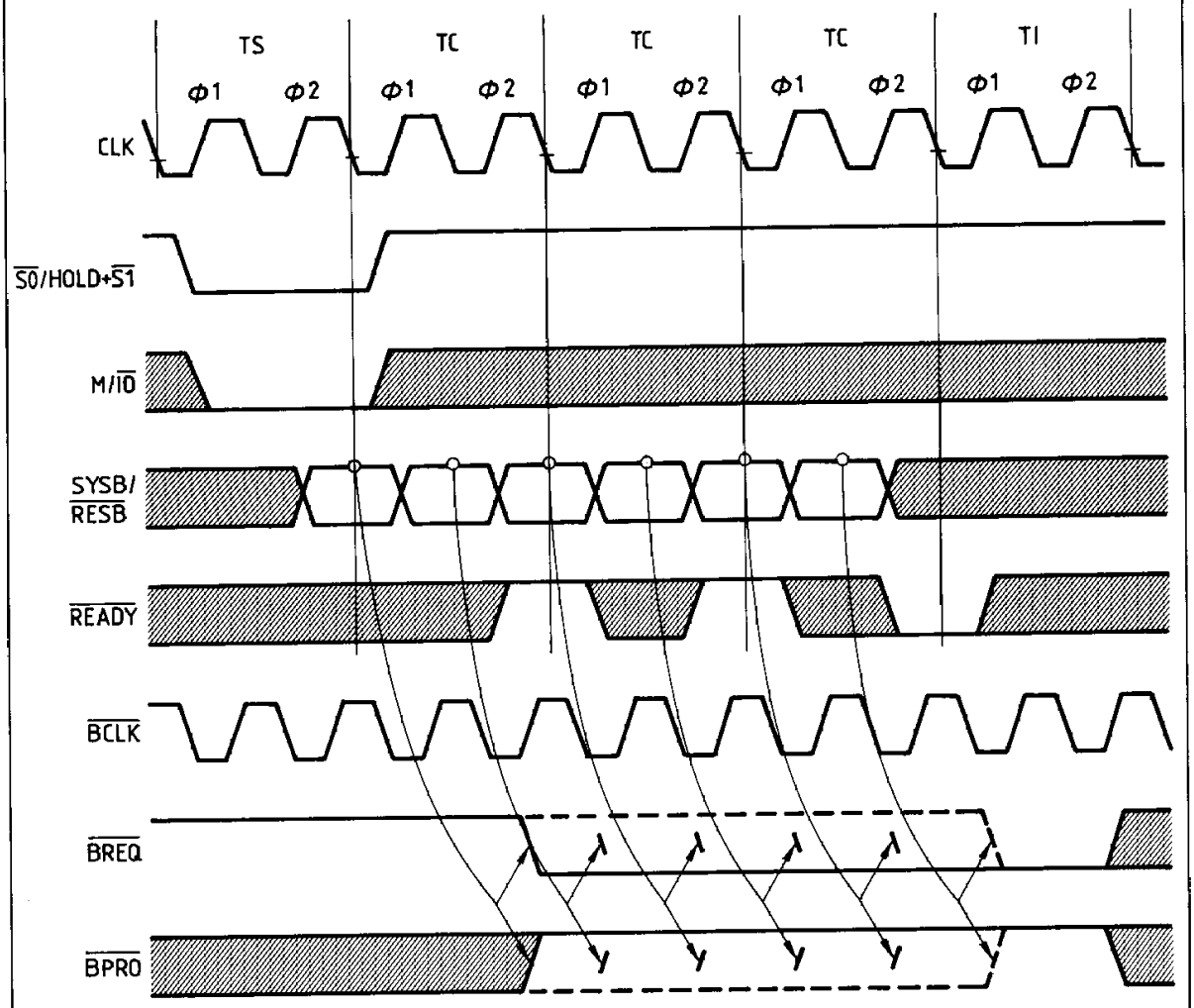


Figure 7
Parallel Priority Resolving Technique

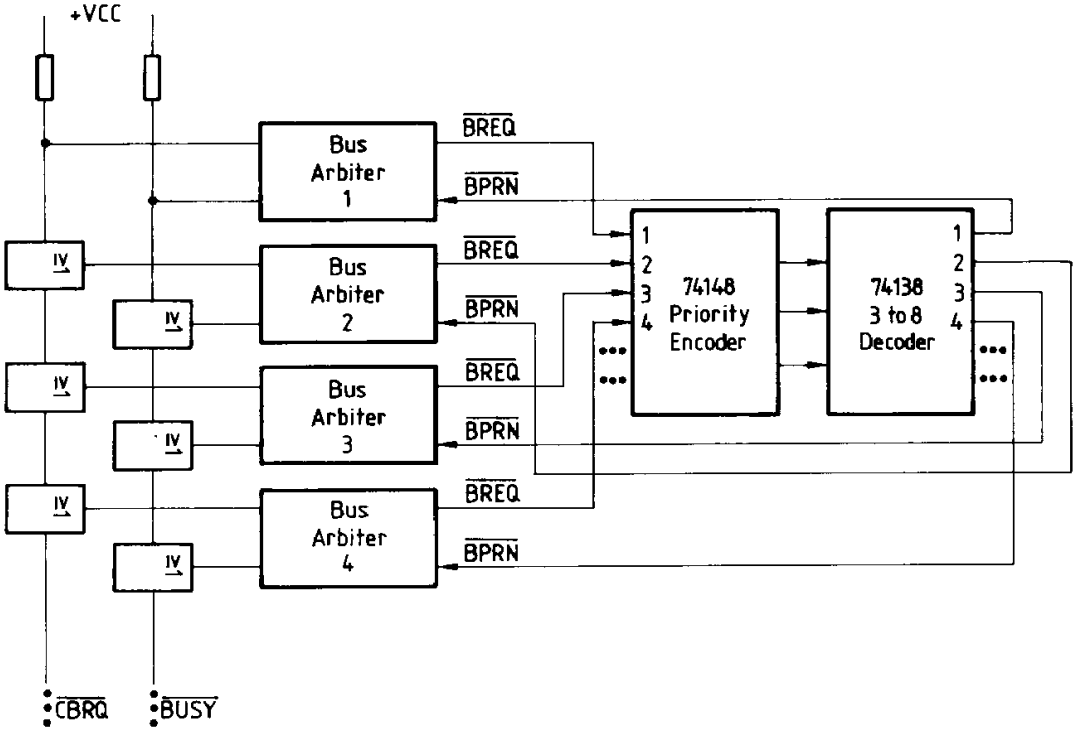
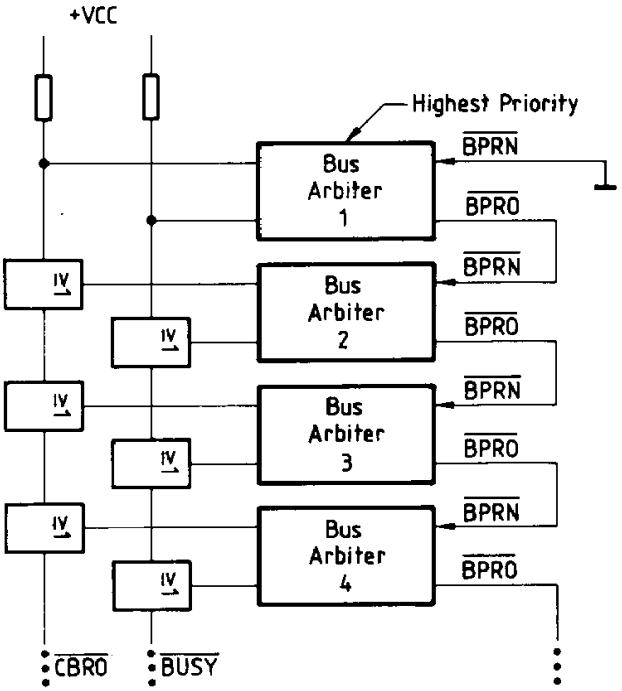


Figure 8
Connections for Serial Priority Resolving Technique



Parallel Priority Resolving Technique

The parallel priority resolving technique requires a separate bus request line ($\overline{BREQ}$) for each arbiter on the multimaster system bus (see figure 7). Each $\overline{BREQ}$ line enters a priority encoder which generates the binary address of the highest priority $\overline{BREQ}$ line currently active. The binary address is decoded to select the $\overline{BPRN}$ line corresponding to the highest priority arbiter requesting the bus. In a parallel scheme, the $\overline{BPRO}$ output is not used.

The arbiter receiving priority ($\overline{BPRN}$ low) then allows its associated bus master onto the multimaster system bus as soon as the bus becomes available (i.e. the bus is no longer busy). Any number of bus masters may be accommodated in this way, limited only by the complexity of the external priority resolving circuitry. Such circuitry must resolve the priority within one $\overline{BCLK}$ period.

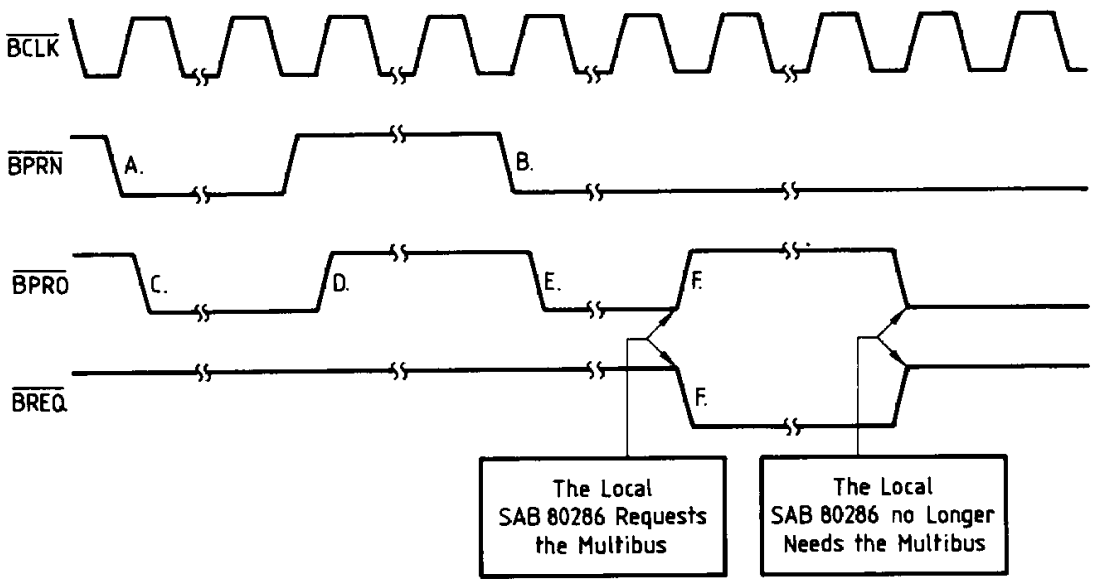
Serial Priority Resolving Technique

The serial priority resolving technique eliminates the need for the priority circuitry of the parallel technique by daisy-chaining the bus arbiters together, that is, connecting the higher priority arbiter's $\overline{BPRO}$ output to the $\overline{BPRN}$ of the next lower priority arbiter (see figure 8). The highest priority bus arbiter would have its $\overline{BPRN}$ tied low in this configuration, signifying to the arbiter that it always has the highest priority when requesting the system bus. In a serial scheme, the $\overline{BREQ}$ output is not used.

Since arbitration must be resolved within one $\overline{BCLK}$ period the number of arbiters connected together in the serial priority is limited by the arbiter's $\overline{BPRN}$ to $\overline{BPRO}$ propagation delay (18ns). For a 10 MHz Multibus $\overline{BCLK}$, five SAB 82289 bus arbiters may be connected in serial configuration.

Maximum number of chained-priority devices = $\frac{\overline{BCLK} \text{ period}}{\overline{BPRN} \text{ to } \overline{BPRO} \text{ delay}}$

Figure 9
Serial Priority Bus Behavior



Note: Events A through F described in the following

When using the serial priority resolving scheme, a higher priority arbiter (for example, arbiter 2, figure 8) passes priority to the next lower priority arbiter (arbiter 3) by asserting its $\overline{BPRO}$ signal (low). This asserts $\overline{BPRN}$ of next arbiter (arbiter 3) as shown in figure 9 event A and event B. An arbiter's $\overline{BPRO}$ is asserted if the arbiter has priority ($\overline{BPRN}$ is asserted) but is not accessing or requesting the system bus (as indicated by $\overline{BREQ}$ inactive as shown in figure 9 event C and event E for arbiter 3). Whenever a higher priority arbiter (arbiter 3) issues a bus request its $\overline{BPRO}$ goes inactive causing the next lower priority arbiter (arbiter 4) to lose its bus priority (figure 9 event F). Any arbiter (arbiter 3) will also bring its $\overline{BPRO}$ inactive if its $\overline{BPRN}$ goes inactive (from arbiter 2), thereby passing the loss of bus priority on to the lower priority arbiters (e.g. arbiter 4) as shown in figure 9 event D.

Rotating Priority Resolving Technique

The rotating priority resolving technique is similar to the parallel priority resolving technique except that priority is dynamically re-assigned. The priority encoder is replaced by a more complex circuitry which rotates priority between requesting arbiters, thus allowing each arbiter an equal chance to use the multimaster system bus over a given period of time.

Selecting the Appropriate Priority Resolving Technique

The choice of a priority resolving technique involves a trade-off between external logic complexity and ease of Multibus access for the different bus masters in the system. The rotating priority resolving technique requires a substantial amount of external logic, but guarantees all the bus masters an equal opportunity to access the system bus. The serial priority resolving technique uses no external logic but has fixed bus master priority levels and can accomodate only a limited number of bus arbiters.

The parallel priority resolving technique is in general a compromise between the other two techniques (for example parallel priority configuration in figure 7 allows up to eight arbiters to be present on the Multibus, with fixed priority levels, while not requiring a large amount of complex external logic to implement).

Releasing the Multibus

Following a data transfer cycle on the Multibus, the SAB 82289 bus arbiter can either retain control of the system bus or release the bus for use by some other bus master. The SAB 82289 can operate in one of three modes, defining different conditions under which the arbiter relinquishes control of the multimaster system bus. These release modes are described in the table below.

If the arbiter was programmed to operate in Always Release Mode (mode 1) during the previous reset, it will surrender the Multibus after each complete transfer cycle. If the arbiter is not in Always Release Mode, it will not surrender the bus until the local SAB 80286 processor enters a halt state, the arbiter is forced off the bus by the loss of $\overline{BPRN}$ (mode 2 or 3), or by a common bus request when the $\overline{CBRQ}$ input is enabled by the $\overline{CBQLCK}$ input (mode 2).

$\overline{CBRQ}$ can save the bus exchange overhead in many cases. If $\overline{CBRQ}$ is high, it indicates to the bus master that no other master is requesting the bus and therefore the present bus master can retain the bus. Without $\overline{CBRQ}$, only $\overline{BPRN}$ indicates whether or not another master is requesting the bus and that only if the other master is of higher priority. Between its bus transfer cycles the master must give up the bus in order to allow lower priority masters to take the bus if they need it. At the start of the master's next transfer cycle, the bus must be regained. If no other master has the bus, this can take approximately two $\overline{BCLK}$ periods. To avoid this overhead of unnecessarily giving up and regaining the bus when no other masters needs it, $\overline{CBRQ}$ is

SAB 82289 Release Modes

Release Mode	Conditions under which the bus arbiter releases the system bus (unless cycles are LOCKed)
Mode 1	The bus arbiter always releases the bus at the end of each transfer cycle
Mode 2	The bus arbiter ratains the bus until: • a higher-priority bus master requests the bus, driving $\overline{BPRN}$ high • a lower-priority bus master requests the bus by pulling $\overline{CBRQ}$ low
Mode 3	The bus arbiter retains the bus until: • a higher-priority bus master requests the bus, driving $\overline{BPRN}$ high ($\overline{CBRQ}$ low ignored)

extremely useful. Any master that wants but does not have the bus, must assert $\overline{CBRQ}$ (low). If $\overline{CBRQ}$ line is not asserted the bus does not have to be released, thereby eliminating the delay of regaining the bus at the start of the next cycle.

The $\overline{LOCK}$ input to the arbiter can be used to override any of the conditions shown in the table before. While $\overline{LOCK}$ is asserted, the arbiter will not surrender control of the Multibus to any other requesting arbiter. Note that the arbiter will surrender the Multibus (synchronous to $\overline{BCLK}$) either in response to RESET or $\overline{INIT}$ signals independent of the current release mode or the state of the arbiter inputs.

The three bus release modes have the same operation when supporting either the SAB 80286 processor or some other bus master.

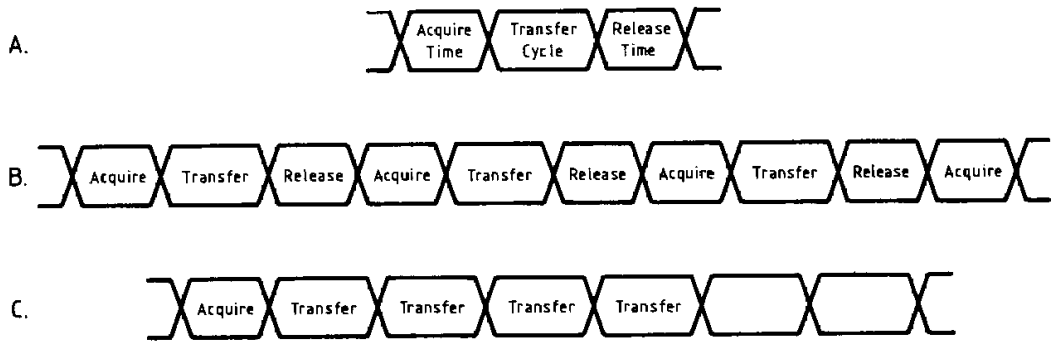
Selecting the Appropriate Release Mode

The choice of which release mode to use may affect the bus utilization of the individual subsystems, and the system as a whole. Mode-dependent performance variations are due to the bus acquisition/release overhead. The effect of these acquire and release times on system bus efficiency is illustrated in figure 10.

An isolated transfer on the multimaster system bus is depicted in figure 10-A. Figure 10-B shows utilization for the bus arbiter operation in mode 1. The arbiter must request and release the system bus for each transfer cycle. Lower priority arbiters have easy access to the system bus, but overall bus efficiency is low. Bus utilization for a bus arbiter operating in mode 2 or 3 is shown in the figure 10-C. In this situation the arbiter acquires the bus once for a sequence of transfers. The arbiter retains the bus until forced off by another bus master's request as defined in table before.

The three release modes of the SAB 82289 allow the designer to optimize the system use of the Multibus.

Figure 10
Effects of Bus Contention on Bus Efficiency



Configuring the SAB 82289 Release Mode

The SAB 82289 bus arbiter can be configured in any of its three bus release modes without additional hardware. It can also be configured to switch between mode 2 and mode 3 under software control of the SAB 80286 processor, requiring that a parallel port or addressable latch be used to drive the $\overline{\text{ALWAYS}}/\overline{\text{CBQLCK}}$ input pin of the SAB 82289 (see figure below).

Figure 11
SAB 82289 Release Mode Configurations

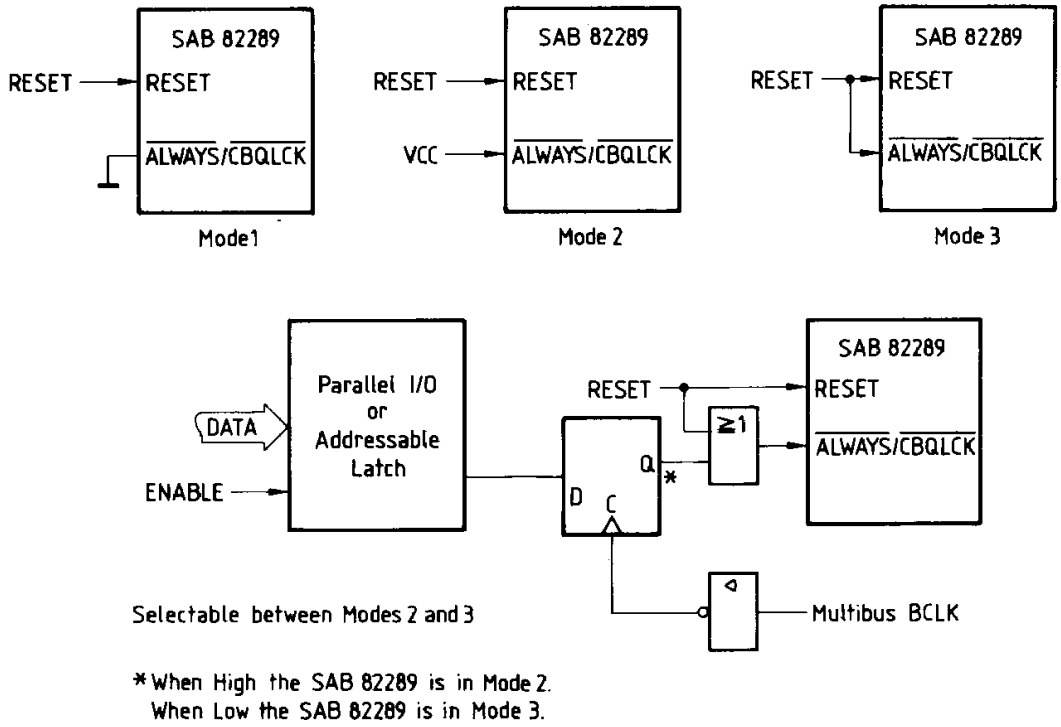
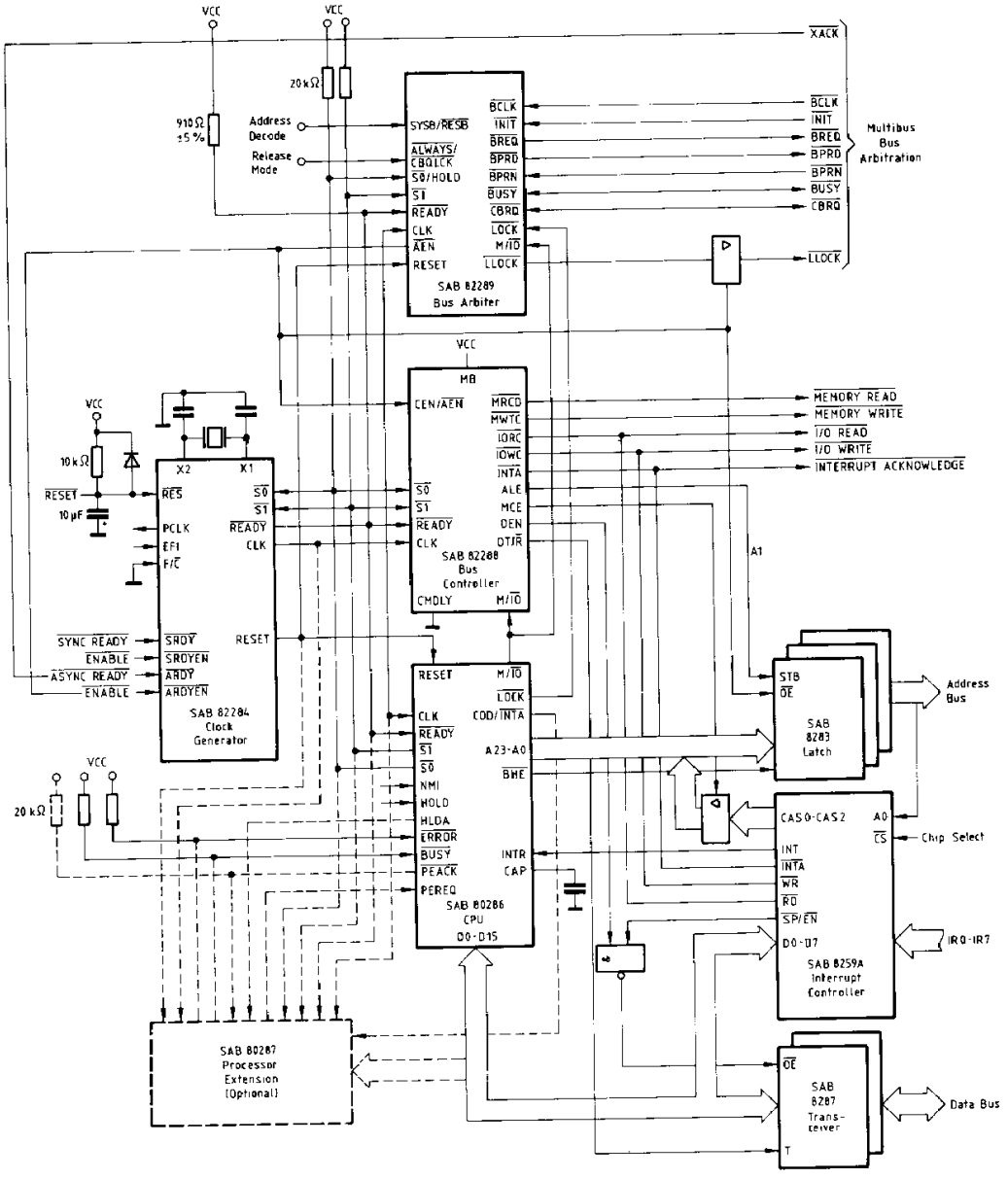


Figure 12
Typical SAB 80286 Subsystem Multibus Interface



Asserting the $\overline{\text{LOCK}}$ Signal

Independent of the particular release mode of the SAB 82289 bus arbiter, the SAB 80286 processor can assert a $\overline{\text{LOCK}}$ signal synchronously to CLK to prevent the arbiter from releasing the Multibus. This software-controlled $\overline{\text{LOCK}}$ signal prevents the SAB 82289 from surrendering the system bus to any other bus master, whether that bus master is of higher or lower priority. The $\overline{\text{LOCK}}$ signal is typically used for implementing software semaphores for shared resources or for critical processes that must run in real-time.

The SAB 82289 $\overline{\text{LLOCK}}$ output is the Multibus timing-compatible signal asserted during all bus cycles which are locked together. The $\overline{\text{LLOCK}}$ is set or reset depending on processor $\overline{\text{LOCK}}$ at the end of the TS cycle. $\overline{\text{LLOCK}}$ will delay going inactive until the termination of the current transfer cycle.

The SAB 82289 will continue to assert the $\overline{\text{LLOCK}}$ signal retaining control of the Multibus until the end of the first "unLOCKed" SAB 80286 bus cycle (SAB 80286 disables its $\overline{\text{LOCK}}$ output on the last bus cycle indicating that no future locked cycles are needed). While the $\overline{\text{LOCK}}$ signal will force the arbiter presently in control to hold the system bus, it cannot force another arbiter to surrender the bus any earlier than it normally would.

The $\overline{\text{LLOCK}}$ signal from the SAB 82289 must be connected to a tri-state buffer in order to drive the Multibus $\overline{\text{LOCK}}$ signal. This tri-state buffer should be enabled by the $\overline{\text{AEN}}$ signal from the arbiter going active.

SAB 82289 Reset and Initialization

The SAB 82289 bus arbiter provides the RESET and $\overline{\text{INIT}}$ pins for initialization. RESET is a CLK synchronous signal from the SAB 82284 clock generator and $\overline{\text{INIT}}$ is an asynchronous signal on the multimaster system bus. By having RESET pin high or $\overline{\text{INIT}}$ pin low the $\overline{\text{BREQ}}$, $\overline{\text{BUSY}}$ and $\overline{\text{AEN}}$ output pins will all become inactive. RESET will also deactivate the $\overline{\text{LLOCK}}$ signal. Unlike RESET, $\overline{\text{INIT}}$ will not clear any pending bus request, the bus request would be asserted after the $\overline{\text{INIT}}$ signal goes inactive.

Note that when the SAB 82289 is initialized by the RESET input it does not wait until the end of the current bus cycle to reset. Any bus cycle in process when RESET goes active will be aborted by the arbiter. Although the $\overline{\text{INIT}}$ signal will also interrupt an active bus cycle, the arbiter can request the Multibus and complete the bus cycle when $\overline{\text{INIT}}$ goes inactive.

As mentioned in the pin description and figure 11 the functions of the $\overline{\text{S0}}$/HOLD pin and the release mode ($\overline{\text{ALWAYS}}$/$\overline{\text{CBQLCK}}$ pin) are programmed at the falling edge of RESET.

Absolute Maximum Ratings [1]

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on Any Pin With Respect to GND	−0.5 to +7V
Power Dissipation	1 W

DC Characteristics

TA = 0 to 70°C, VCC = 5V ±5%

Symbol	Parameter	Limit values		Unit	Test condition
		min.	max.		
VIL	Input low Voltage	−0.5	0.8	V	–
VIH	Input High Voltage	2.0	VCC+0.5	V	–
VILC	CLK Input Low Voltage	−0.5	0.6	V	–
VIHC	CLK Input High Voltage	3.8	VCC+1.0	V	–
VOL	Output Low Voltage: $\overline{BUSY}$, $\overline{CBRQ}$ $\overline{BPRO}$, $\overline{BREQ}$, $\overline{AEN}$ $\overline{LLOCK}$	–	0.45	V	IOL = 32mA IOL = 16 mA IOL = 5mA
VOH	Output High Voltage	2.4	–	V	IOH = 400 µA
ILI	Input Leakage Current	–	±10 ±1	µA mA	0.45 V ≤VIN ≤VCC 0 V ≤VIN <0.45 V
ILO	Output Leakage Current	–	±10	µA	0.45 V ≤VOUT ≤VCC
ICC	Power Supply Current	–	120	mA	–
CCLK	CLK, $\overline{BCLK}$ Input Capacitance	–	12	pF	fC = 1 MHz
CIN	Input Capacitance	–	10	pF	fC = 1 MHz
CIO	Input/Output Capacitance	–	20	pF	fC = 1 MHz

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics SAB 82289

TA = 0 to 70°C, VCC = 5V ±5%
AC timings are referenced to 0.8 and 2.0 V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter	Limit values * 8 MHz		Unit	Test condition	Shown in Figure
		min.	max.			
1	CLK Cycle Period	62	t5+50	ns	–	13
2	CLK Low Time	15	230	ns	at 1.0 V	13
3	CLK High Time	20	235	ns	at 3.6V	13
4	CLK Rise/Fall Time	–	10	ns	1.0 to 3.6V	13
5	$\overline{\text{BCLK}}$ Cycle Time	100	∞	ns	–	13
6	$\overline{\text{BCLK}}$ High/Low Time	30	–	ns	–	13
7	$\overline{\text{S0}}$/HOLD, $\overline{\text{S1}}$, M/$\overline{\text{IO}}$ Setup	22	–	ns	–	13, 22
8	$\overline{\text{S0}}$/HOLD, $\overline{\text{S1}}$, M/$\overline{\text{IO}}$ Hold	1	–	ns	–	13, 22
9	$\overline{\text{READY}}$ Setup	38	–	ns	–	13
10	$\overline{\text{READY}}$ Hold Time	25	–	ns	–	13
11	$\overline{\text{LOCK}}$, SYSB/$\overline{\text{RESB}}$ Setup Time	20	–	ns	–	13, 18
12	$\overline{\text{LOCK}}$, SYSB/$\overline{\text{RESB}}$ Hold Time	1	–	ns	–	13, 18
13	RESET Setup Time	20	–	ns	–	19
14	RESET Hold Time	1	–	ns	–	19
15	RESET Active Pulse Width	16	–	CLKs	–	19
16	$\overline{\text{INIT}}$ Setup Time	45	–	ns	9)	20
17	$\overline{\text{INIT}}$ Hold Time	1	–	ns	9)	20
18	$\overline{\text{INIT}}$ Active Pulse Width	3 (t1) +3(t14)	–	ns	–	20
19	$\overline{\text{BUSY}}$, $\overline{\text{BPRN}}$, $\overline{\text{CBRQ}}$, $\overline{\text{CBQLCK}}$/$\overline{\text{ALWAYS}}$ Setup to $\overline{\text{BCLK}}$ (or to RESET)	20	–	ns	–	13, 15, 21, 22
20	$\overline{\text{BUSY}}$, $\overline{\text{BPRN}}$, $\overline{\text{CBRQ}}$, $\overline{\text{CBQLCK}}$/$\overline{\text{ALWAYS}}$ Hold to $\overline{\text{BCLK}}$ (or to RESET)	1	–	ns	–	13, 15, 21, 22
21	$\overline{\text{BCLK}}$ to $\overline{\text{BREQ}}$ Delay	–	30	ns	1)	13,14,22
22	$\overline{\text{BCLK}}$ to $\overline{\text{BPRO}}$ Delay	–	35	ns	2)	17
23	$\overline{\text{BPRN}}$ to $\overline{\text{BPRO}}$ Delay	–	25	ns	2)	17
24	$\overline{\text{BCLK}}$ to $\overline{\text{BUSY}}$ Active Delay	1	60	ns	3)	13, 22

For notes see next page.

AC Characteristics SAB 82289 (continued)

Symbol	Parameter	Limit values * 8 MHz		Unit	Test condition	Shown in Figure
		min.	max.			
25	$\overline{BCLK}$ to $\overline{BUSY}$ Float Delay	–	35	ns	4)	13, 14
26	$\overline{BCLK}$ to $\overline{CBRQ}$ Active Delay	–	55	ns	5)	13, 22
27	$\overline{BCLK}$ to $\overline{CBRQ}$ Float Delay	–	35	ns	4)	13,20,22
28	$\overline{BCLK}$ to $\overline{AEN}$ Active Delay	1	25	ns	6)	13
29	CLK to $\overline{AEN}$ Inactive Delay	3	25	ns	6)	13, 14
30	CLK to $\overline{LLOCK}$ Delay	–	20	ns	7)	18
31	RESET to $\overline{LLOCK}$ Delay	–	35	ns	7)	19
32	CLK to $\overline{BCLK}$ Setup Time	38	–	ns	8)	13,16,20
33	$\overline{BCLK}$ to $\overline{AEN}$ Output Delay	1	30	ns	6)	22

*) Preliminary

1) $\overline{BREQ}$ load CL = 60 pF

2) $\overline{BPRO}$ load CL = 60 pF

3) $\overline{BUSY}$ load CL = 300 pF

4) Float condition occurs when output current is less than ILO in magnitude

5) $\overline{CBRQ}$ load CL = 300 pF

6) $\overline{AEN}$ load CL = 150 pF

7) $\overline{LLOCK}$ load CL = 60 pF

8) In actual use, CLK and $\overline{BCLK}$ are usually asynchronous to each other. However, for component testing purposes this specification is required to assure signal recognition at specific CLK and $\overline{BCLK}$ edges.

9) $\overline{INIT}$ is asynchronous to CLK and to $\overline{BCLK}$. However, for component testing purposes, this specification is required to assure signal recognition at specific CLK and $\overline{BCLK}$ edges.

AC Characteristics SAB 82289-6

TA = 0 to 70°C, VCC = 5V ±5%
AC timings are referenced to 0.8 and 2.0 V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter	Limit values * 6 MHz		Unit	Test condition	Shown in Figure
		min.	max.			
1	CLK Cycle Period	83	t5+50	ns	–	13
2	CLK Low Time	20	225	ns	at 1.0 V	13
3	CLK High Time	25	230	ns	at 3.6 V	13
4	CLK Rise/Fall Time	–	10	ns	1.0 to 3.6 V	13
5	$\overline{\text{BCLK}}$ Cycle Time	100	∞	ns	–	13
6	$\overline{\text{BCLK}}$ High/Low Time	30	–	ns	–	13
7	$\overline{\text{S0}}$/HOLD, $\overline{\text{S1}}$, M/$\overline{\text{IO}}$ Setup	28	–	ns	–	13, 22
8	$\overline{\text{S0}}$/HOLD, $\overline{\text{S1}}$, M/$\overline{\text{IO}}$ Hold	1	–	ns	–	13, 22
9	$\overline{\text{READY}}$ Setup	50	–	ns	–	13
10	$\overline{\text{READY}}$ Hold Time	35	–	ns	–	13
11	$\overline{\text{LOCK}}$, SYSB/$\overline{\text{RESB}}$ Setup Time	28	–	ns	–	13, 18
12	$\overline{\text{LOCK}}$, SYSB/$\overline{\text{RESB}}$ Hold Time	1	–	ns	–	13, 18
13	RESET Setup Time	28	–	ns	–	19
14	RESET Hold Time	1	–	ns	–	19
15	RESET Active Pulse Width	16	–	CLKs	–	19
16	$\overline{\text{INIT}}$ Setup Time	45	–	ns	9)	20
17	$\overline{\text{INIT}}$ Hold Time	1	–	ns	9)	20
18	$\overline{\text{INIT}}$ Active Pulse Width	3 (t1) +3(t14)	–	ns	–	20
19	$\overline{\text{BUSY}}$, $\overline{\text{BPRN}}$, $\overline{\text{CBRQ}}$, $\overline{\text{CBQLCK}}$/$\overline{\text{ALWAYS}}$ Setup to $\overline{\text{BCLK}}$ (or to RESET)	20	–	ns	–	13, 15, 21, 22
20	$\overline{\text{BUSY}}$, $\overline{\text{BPRN}}$ $\overline{\text{CBRQ}}$, $\overline{\text{CBQLCK}}$/$\overline{\text{ALWAYS}}$ Hold to $\overline{\text{BCLK}}$ (or to RESET)	1	–	ns	–	13, 15, 21, 22
21	$\overline{\text{BCLK}}$ to $\overline{\text{BREQ}}$ Delay	–	30	ns	1)	13,14,22
22	$\overline{\text{BCLK}}$ to $\overline{\text{BPRO}}$ Delay	–	35	ns	2)	17
23	$\overline{\text{BPRN}}$ to $\overline{\text{BPRO}}$ Delay	–	25	ns	2)	17
24	$\overline{\text{BCLK}}$ to $\overline{\text{BUSY}}$ Active Delay	1	60	ns	3)	13, 22

For notes see next page.

AC Characteristics SAB 82289-6 (continued)

Symbol	Parameter	Limit values * 6 MHz		Unit	Test condition	Shown in Figure
		min.	max.			
25	$\overline{BCLK}$ to $\overline{BUSY}$ Float Delay	–	35	ns	4)	13, 14
26	$\overline{BCLK}$ to $\overline{CBRQ}$ Active Delay	–	55	ns	5)	13, 22
27	$\overline{BCLK}$ to $\overline{CBRQ}$ Float Delay	–	35	ns	4)	13,20,22
28	$\overline{BCLK}$ to $\overline{AEN}$ Active Delay	1	25	ns	6)	13
29	CLK to $\overline{AEN}$ Inactive Delay	3	25	ns	6)	13, 14
30	CLK to $\overline{LLOCK}$ Delay	–	20	ns	7)	18
31	RESET to $\overline{LLOCK}$ Delay	–	35	ns	7)	19
32	CLK to $\overline{BCLK}$ Setup Time	38	–	ns	8)	13,16, 20
33	$\overline{BCLK}$ to $\overline{AEN}$ Output Delay	1	30	ns	6)	22

*) Preliminary

1) $\overline{BREQ}$ load CL = 60 pF

2) $\overline{BPRO}$ load CL = 60 pF

3) $\overline{BUSY}$ load CL = 300 pF

4) Float condition occurs when output current is less than ILO in magnitude

5) $\overline{CBRQ}$ load CL = 300 pF

6) $\overline{AEN}$ load CL = 150 pF

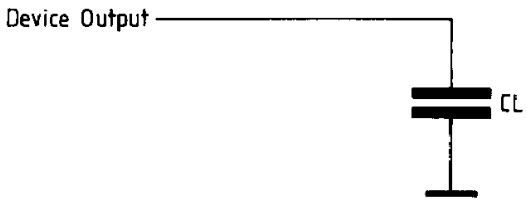
7) $\overline{LLOCK}$ load CL = 60 pF

8) In actual use, CLK and $\overline{BCLK}$ are usually asynchronous to each other. However, for component testing purposes this specification is required to assure signal recognition at specific CLK and $\overline{BCLK}$ edges.

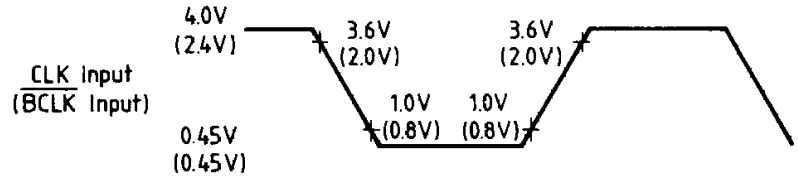
9) $\overline{INIT}$ is asynchronous to CLK and to $\overline{BCLK}$. However, for component testing purposes, this specification is required to assure signal recognition at specific CLK and $\overline{BCLK}$ edges.

AC Testing Waveforms

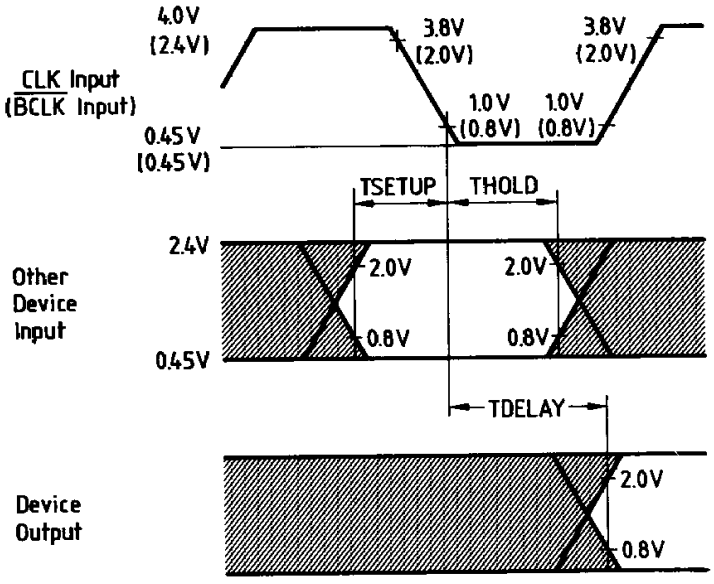
Test Loading on Outputs



Drive and Measurement Points – CLK Input ($\overline{BCLK}$ Input)



Setup, Hold and Delay Time Measurement – General



Waveforms

The waveforms (figures 13 to 21) show the timing relationships of the inputs and the outputs and do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown via the general cases. Special cases are shown when needed.

To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.

The SAB 82289 bus arbiter serves as an interface between the SAB 80286 subsystem which operates synchronously to the CLK signal and Multibus which operates synchronously to $\overline{\text{BCLK}}$ signal. CLK and $\overline{\text{BCLK}}$ generally operate asynchronously to each other and at different frequencies. Thus, the exact clock period in which an input synchronous to one clock will cause a response synchronous to the other clock depends on the relative phase and frequency of CLK and $\overline{\text{BCLK}}$ at the time the input is sensed.

One strict relation between CLK and $\overline{\text{BCLK}}$ must be maintained for proper Multibus arbitration. If the CLK period is too long relative to $\overline{\text{BCLK}}$ period (t1 greater than t5 +50 ns), another arbiter could gain control of the system bus before this arbiter has released $\overline{\text{AEN}}$ synchronously to its CLK. This situation arises since the release of $\overline{\text{AEN}}$ is synchronous to the next falling CLK edge after the processor cycle ends but the release of $\overline{\text{BREQ}}$ and $\overline{\text{BUSY}}$ is synchronous to the next falling $\overline{\text{BCLK}}$ edge after the processor cycle ends. In practice, any CLK frequency greater than 6.66 MHz (i.e. SAB 80286 processor speeds greater than 3.33 MHz) will avoid conflict with a 10 MHz $\overline{\text{BCLK}}$. Therefore all SAB 80286 speed selections are Multibus compatible.

Figure 13
Multibus Acquisition and Always-Release Operation

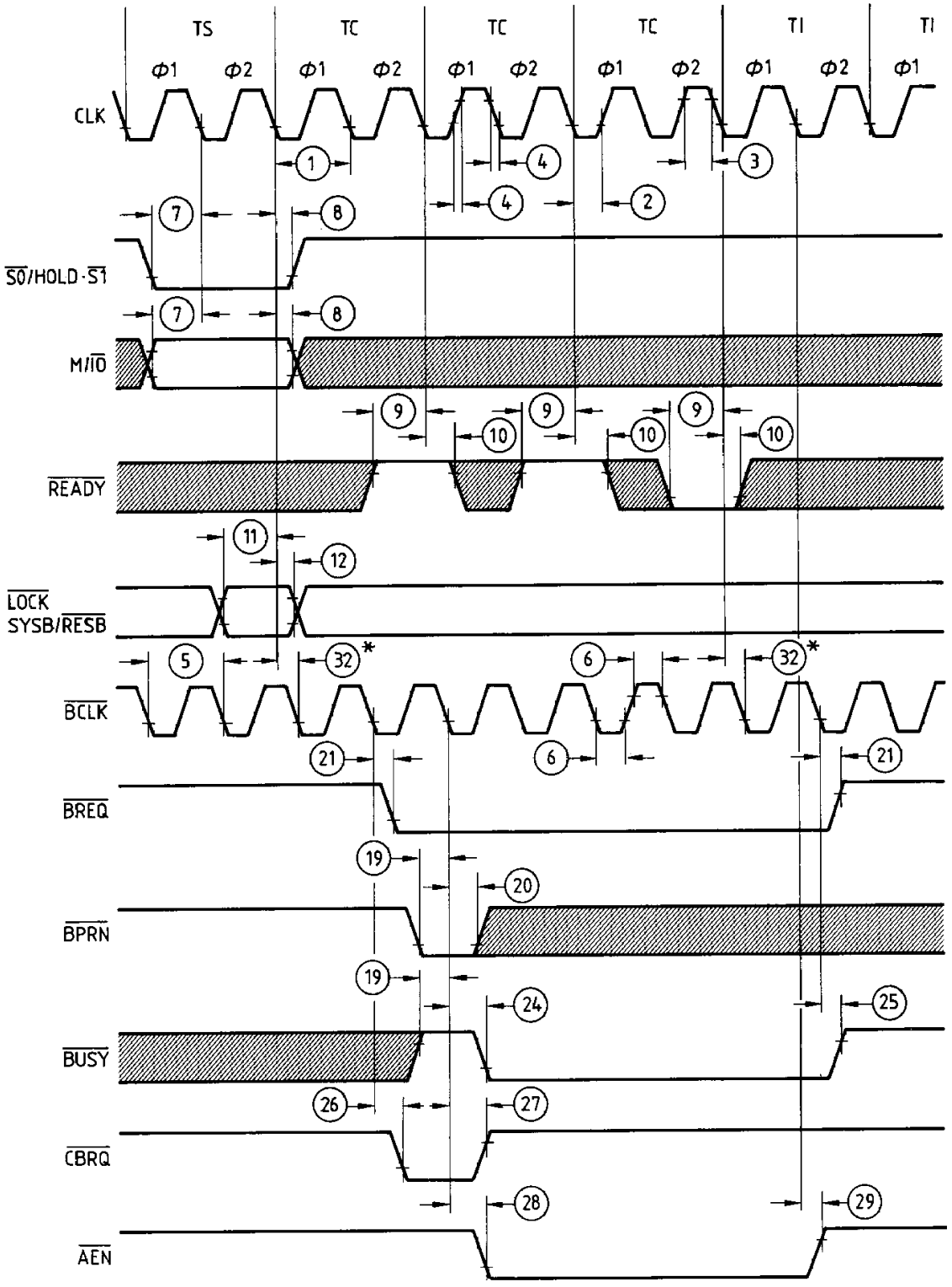
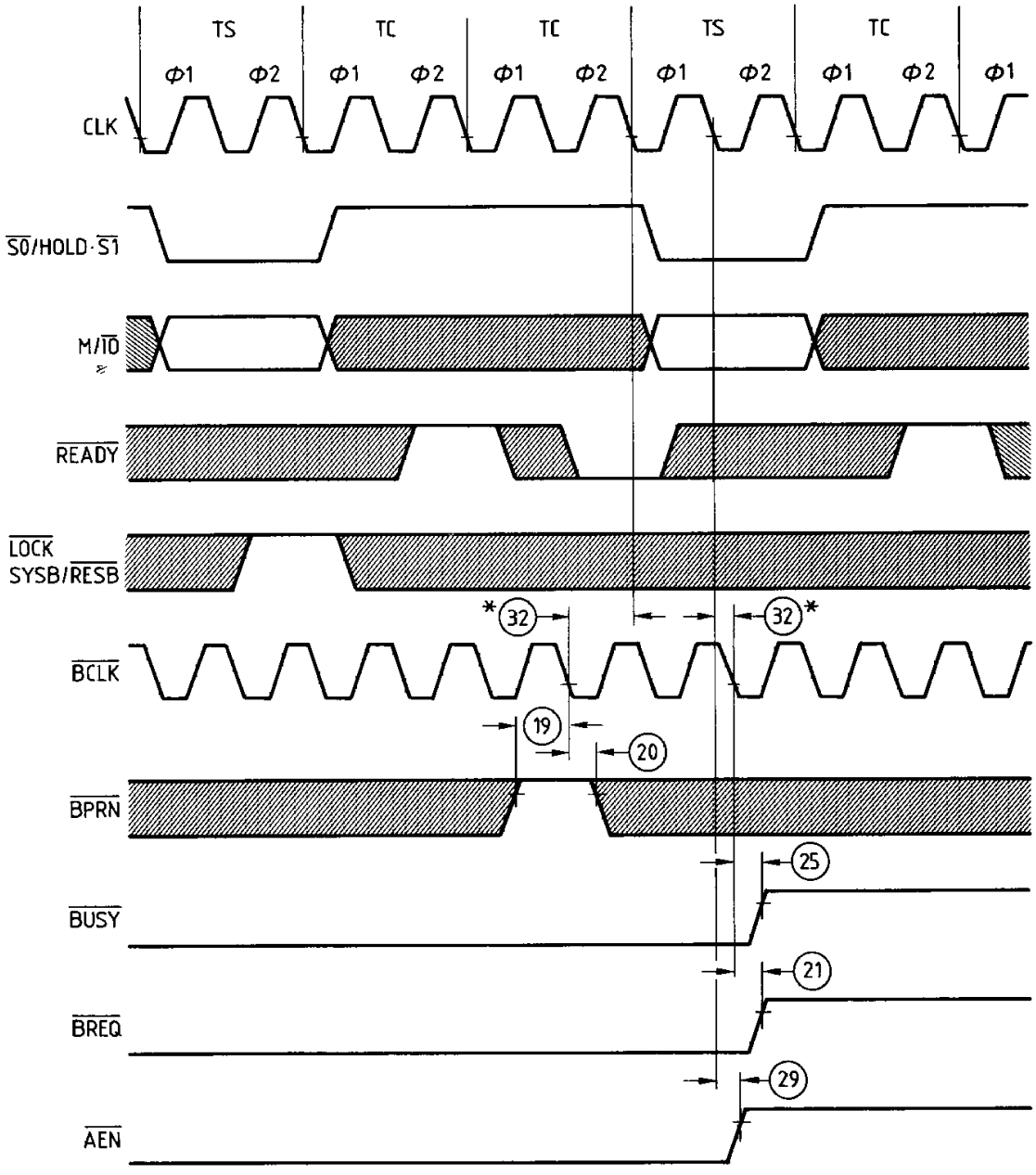
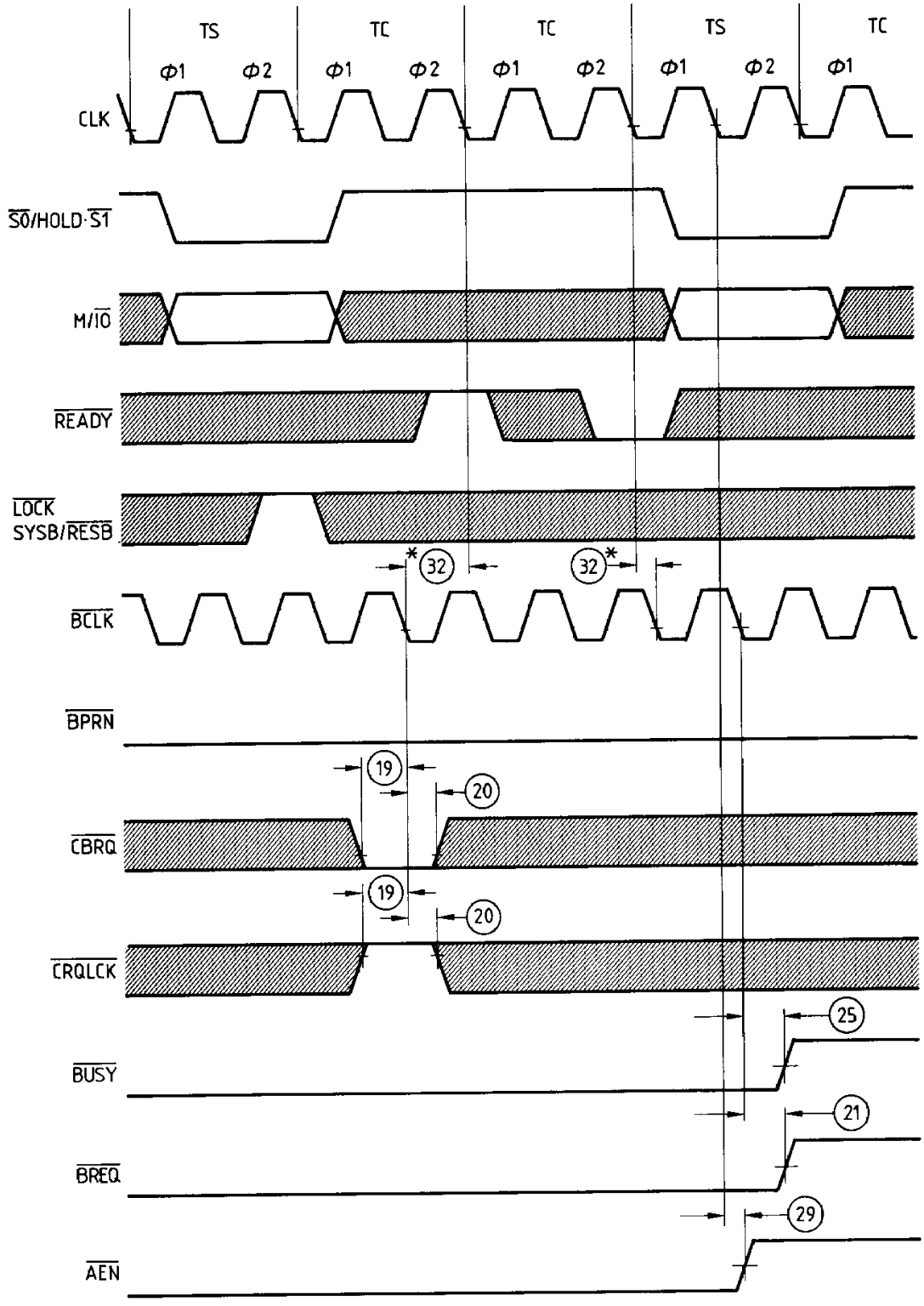


Figure 14
Multibus Release due to $\overline{\text{BPRN}}$ Inactive



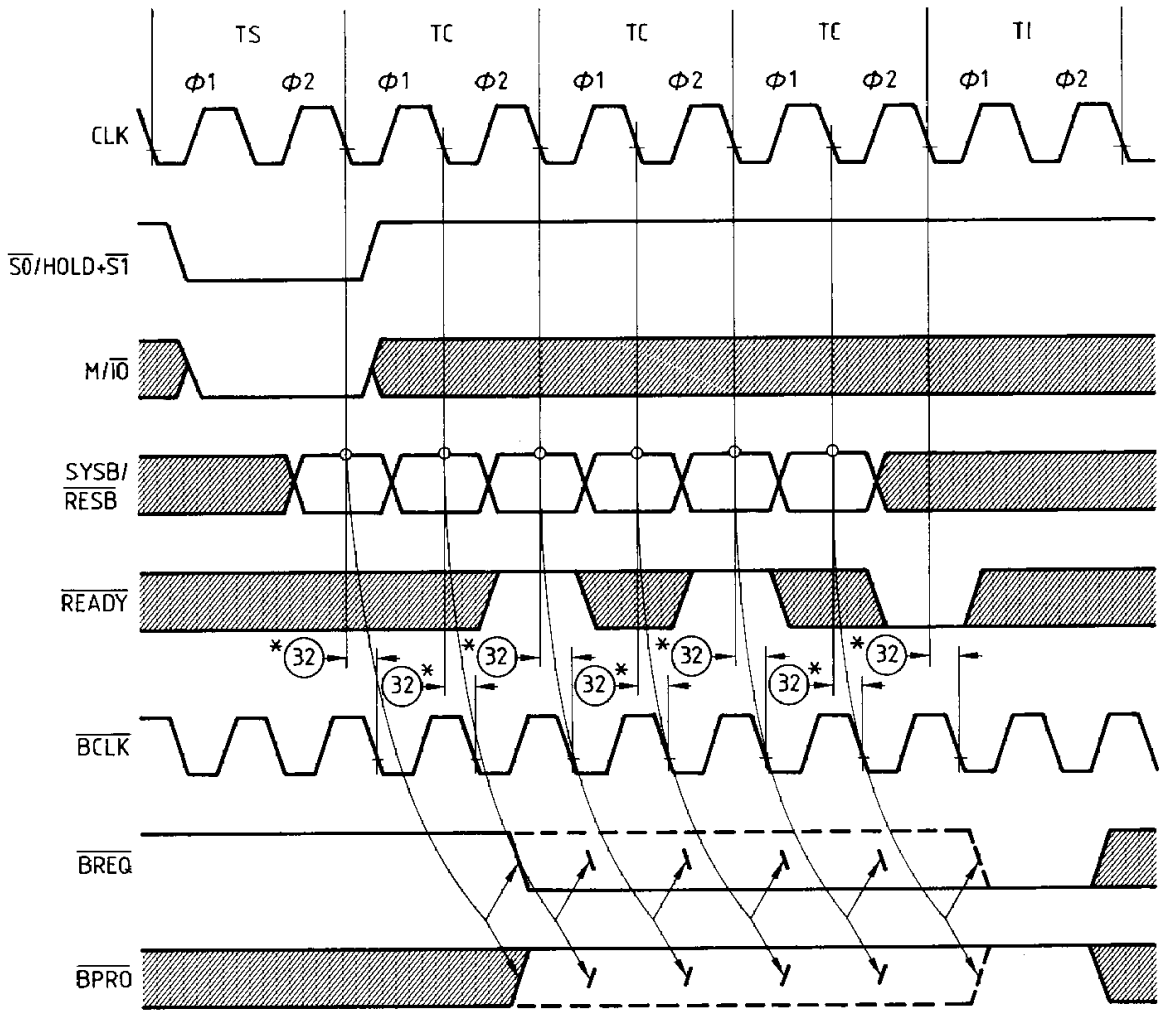
*Only for SAB 82289 Test Purposes

Figure 15
Multibus Release due to $\overline{CBRQ}$ Active



*Only for SAB 82289 Test Purposes

Figure 16
Multibus Acquisition during SAB 80286 INTA Cycles



*Only for SAB 82289 test purposes

Figure 17
$\overline{\text{BPRN}}$ to $\overline{\text{BPRO}}$ Timing Relationship

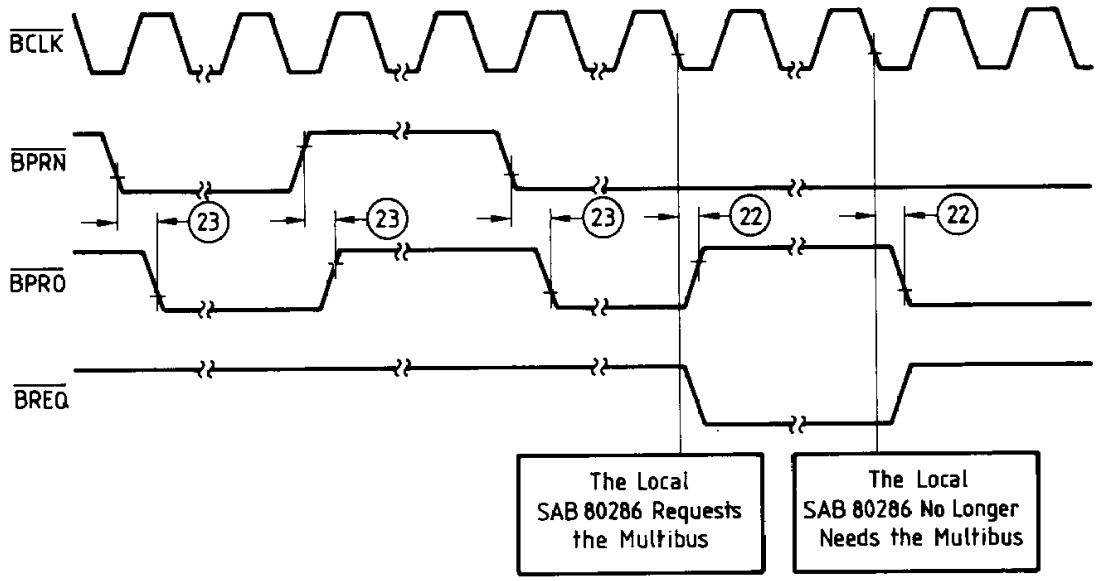


Figure 18
SAB 80286 $\overline{\text{LOCK}}$ and SAB 82289 $\overline{\text{LLOCK}}$ Relationship

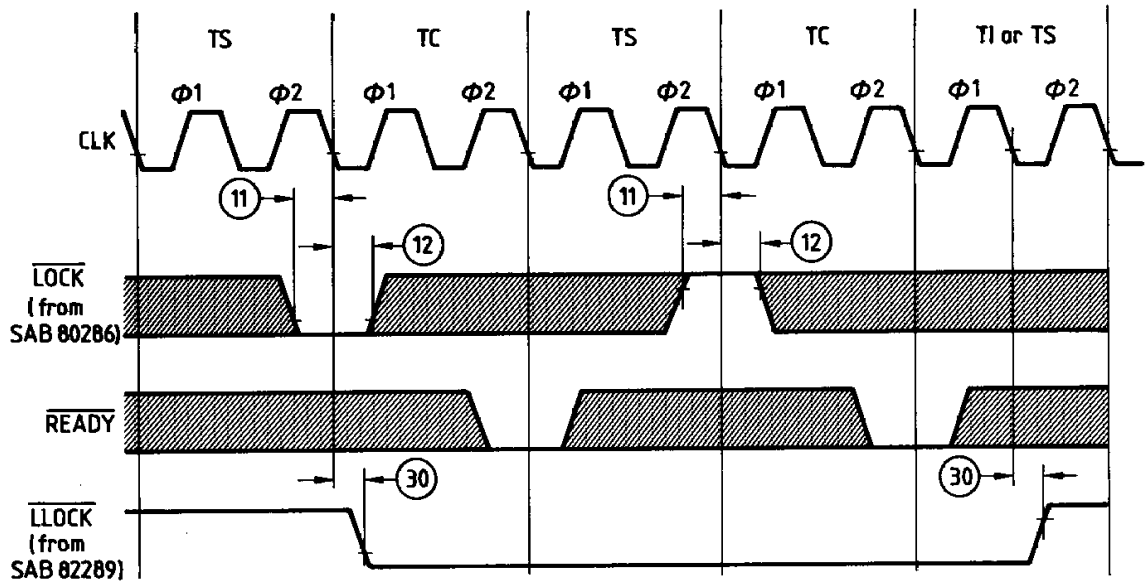
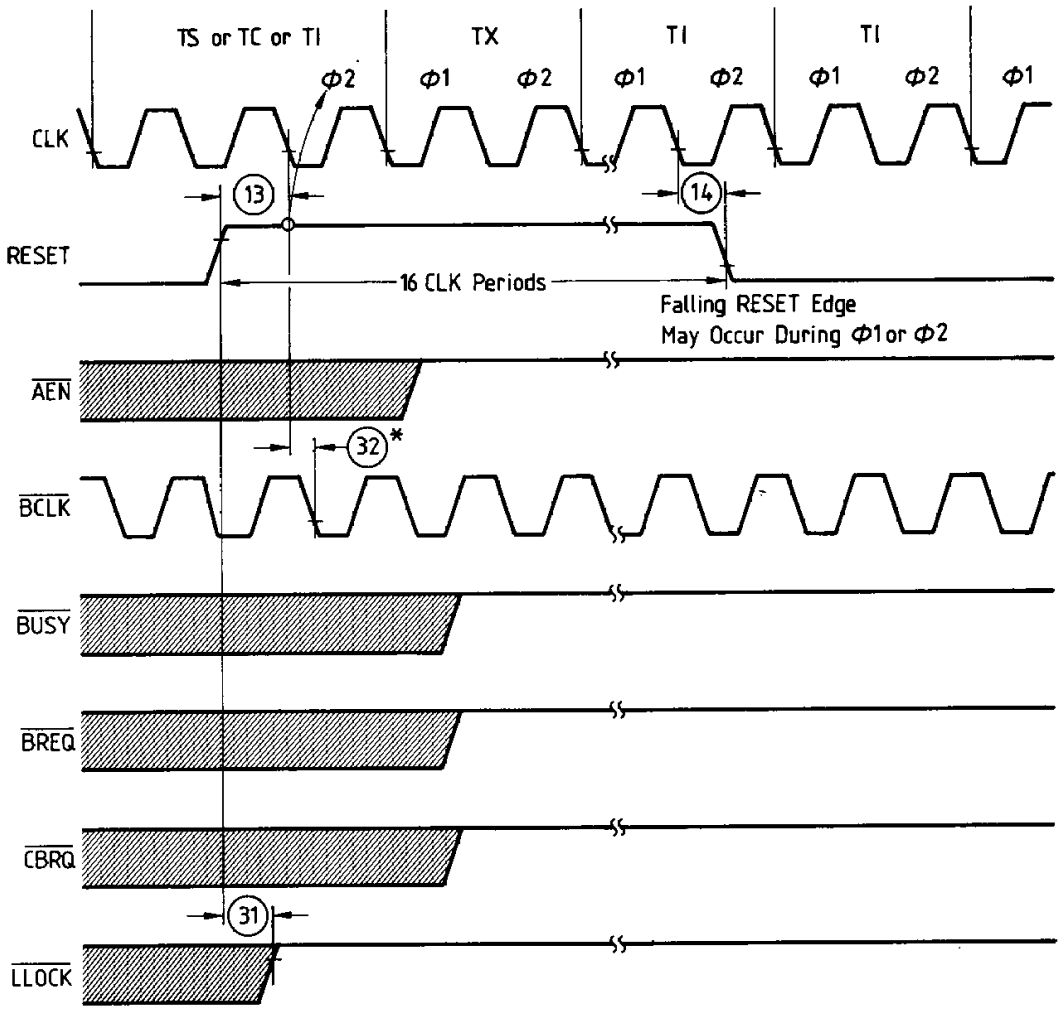
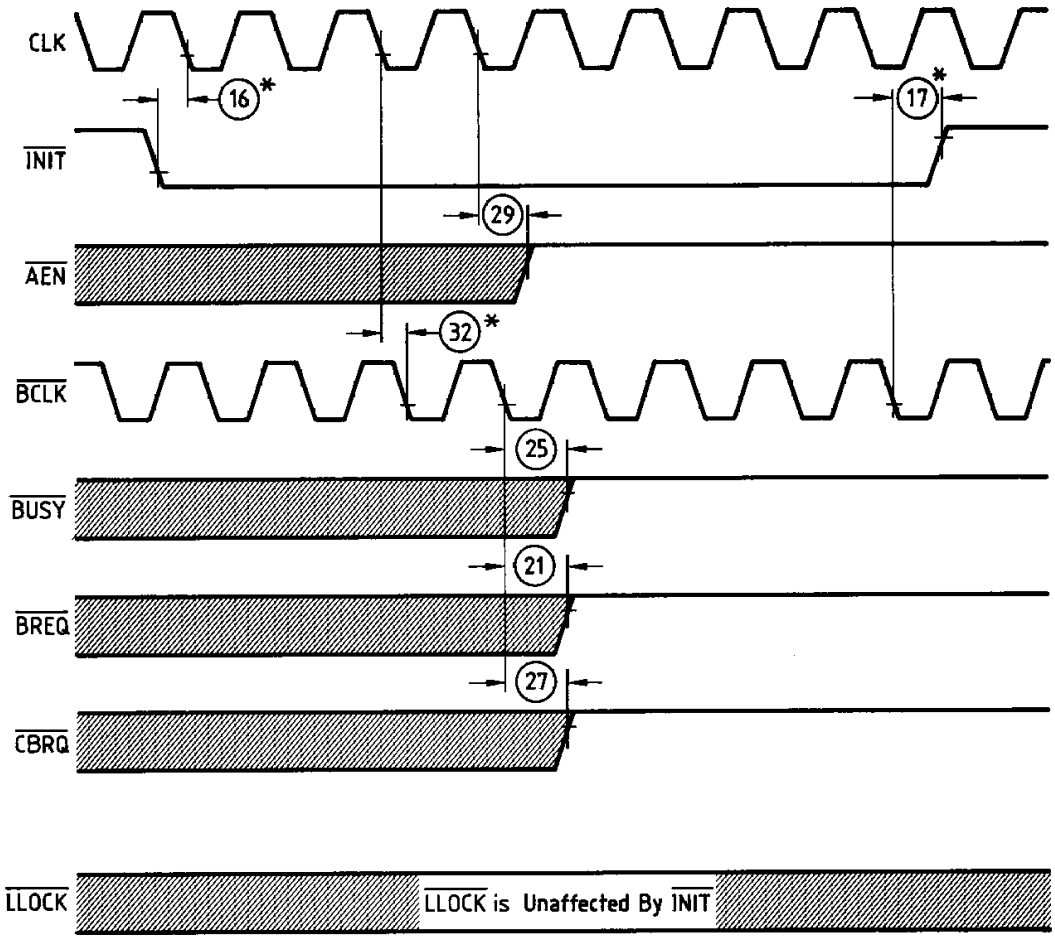


Figure 19
RESET Active Pulse



*For SAB 82289 Test Purposes Only.

Figure 20
$\overline{\text{INIT}}$ Active Pulse



*For SAB 82289 Test Purposes Only.

Figure 21
Programming the Always-Release/Common-Bus-Request-Release Option

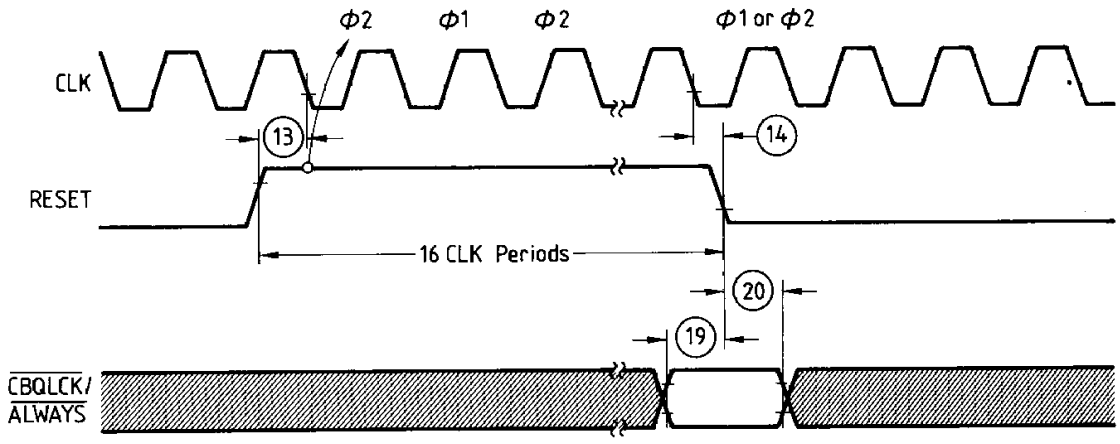
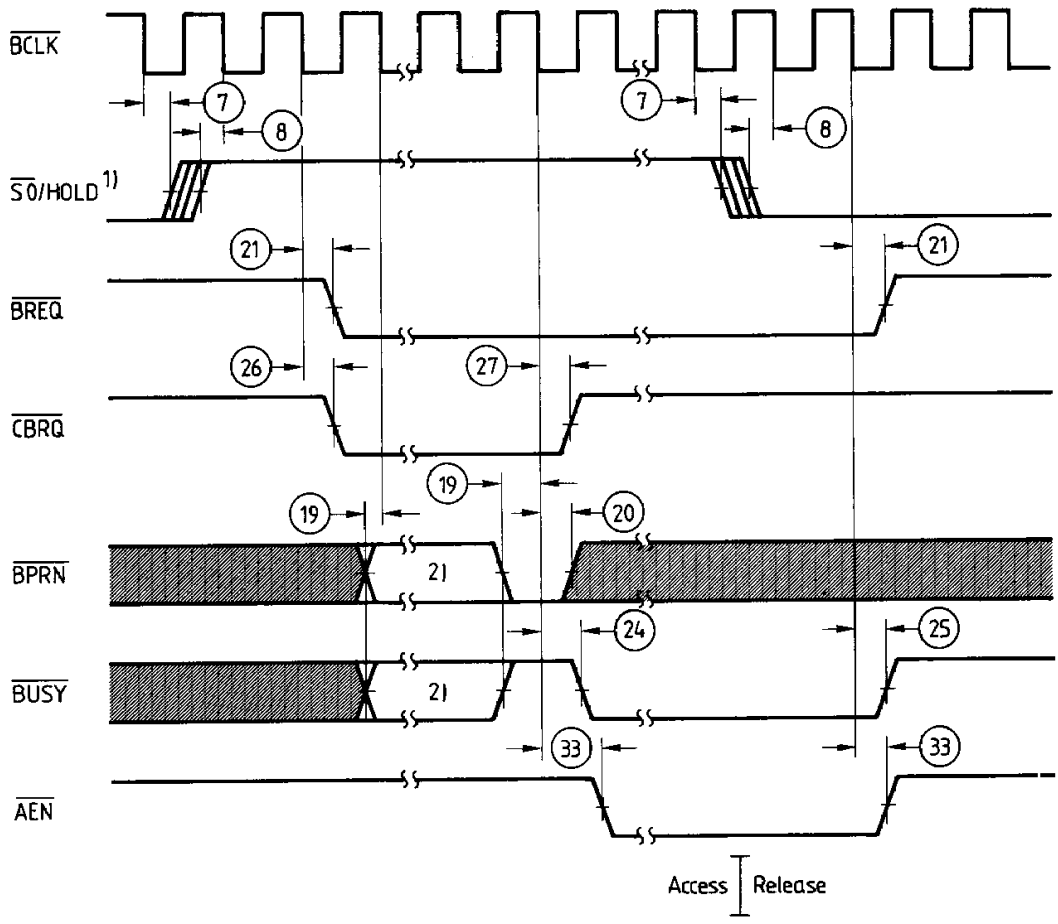


Figure 22
Multibus Arbitration Activated by HOLD Input



[1] Used as HOLD input

[2] Valid conditions are $\overline{\text{BPRN}}$ high or $\overline{\text{BUSY}}$ low. If one of the two conditions is fulfilled, the level of the other signal ($\overline{\text{BUSY}}$ or $\overline{\text{BPRN}}$) may be arbitrary

Ordering Information

Type	Ordering code	Description
SAB 82289-P	Q67020-Y77	Bus Arbiter 16 MHz (plastic)
SAB 82289-6-P	Q67120-Y111	Bus Arbiter 12 MHz (plastic)