32-Lane 24-Port PCIe® Gen2 System Interconnect Switch

89HPES32NT24AG2 Datasheet

Device Overview

The 89HPES32NT24AG2 is a member of the IDT family of PCI Express® switching solutions. The PES32NT24AG2 is a 32-lane, 24-port system interconnect switch optimized for PCI Express Gen2 packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include multi-host or intelligent I/O based systems where inter-domain communication is required, such as servers, storage, communications, and embedded systems.

Features

- High Performance Non-Blocking Switch Architecture
  - 32-lane, 24-port PCIe switch with flexible port configuration
  - Integrated SerDes supports 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
  - Delivers up to 32 GBps (256 Gbps) of switching capacity
  - Supports 128 Bytes to 2 KB maximum payload size
  - Low latency cut-through architecture
  - Supports one virtual channel and eight traffic classes
- Port Configurability
  - Four x8 stacks
    - Two x8 stacks, each configurable as:
      - One x8 port
      - Two x4 ports
      - Four x2 ports
      - Eight x1 ports
      - Several combinations of the above lane widths
    - Two x8 stacks, each configurable as:
      - One x8 port
      - Two x4 ports
      - Four x2 ports
      - Several combinations of the above lane widths
  - Automatic per port link width negotiation (x8 → x4 → x2 → x1)
  - Crosslink support
  - Automatic lane reversal
  - Per lane SerDes configuration
    - De-emphasis
    - Receive equalization
    - Drive strength
- Innovative Switch Partitioning Feature
  - Supports up to 8 fully independent switch partitions
  - Logically independent switches in the same device
  - Configurable downstream port device numbering
  - Supports dynamic reconfiguration of switch partitions
    - Dynamic port reconfiguration — downstream, upstream, non-transparent bridge
    - Dynamic migration of ports between partitions
    - Movable upstream port within and between switch partitions
- Non-Transparent Bridging (NTB) Support
  - Supports up to 8 NT endpoints per switch, each endpoint can communicate with other switch partitions or external PCIe domains or CPUs
  - 6 BARs per NT Endpoint
    - Bar address translation
    - All BARs support 32/64-bit base and limit address translation
    - Two BARs (BAR2 and BAR4) support look-up table based address translation
  - 32 inbound and outbound doorbell registers
  - 4 inbound and outbound message registers
  - Supports up to 64 masters
  - Unlimited number of outstanding transactions
- Multicast
  - Compliant with the PCI-SIG multicast
  - Supports 64 multicast groups
  - Supports multicast across non-transparent port
  - Multicast overlay mechanism support
  - ECRC regeneration support
- Integrated Direct Memory Access (DMA) Controllers
  - Supports up to 2 DMA upstream ports, each with 2 DMA channels
  - Supports 32-bit and 64-bit memory-to-memory transfers
    - Fly-by translation provides reduced latency and increased performance over buffered approach
    - Supports arbitrary source and destination address alignment
    - Supports intra- as well as inter-partition data transfers using the non-transparent endpoint
  - Supports DMA transfers to multicast groups
  - Linked list descriptor-based operation
  - Flexible addressing modes
    - Linear addressing
    - Constant addressing
- Quality of Service (QoS)
  - Port arbitration
    - Round robin
  - Request metering
    - IDT proprietary feature that balances bandwidth among switch ports for maximum system throughput

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- High performance switch core architecture
  - Combined Input Output Queued (CIOQ) switch architecture with large buffers
- Clocking
  - Supports 100 MHz and 125 MHz reference clock frequencies
  - Flexible port clocking modes
    - Common clock
    - Non-common clock
    - Local port clock with SSC (spread spectrum setting) and port reference clock input
- Hot-Plug and Hot Swap
  - Hot-plug controller on all ports
    - Hot-plug supported on all downstream switch ports
  - All ports support hot-plug using low-cost external I^2C I/O expanders
  - Configurable presence-detect supports card and cable applications
  - GPE output pin for hot-plug event notification
    - Enables SCI/SMI generation for legacy operating system support
  - Hot-swap capable I/O
- Power Management
  - Supports D0, D3hot and D3 power management states
  - Active State Power Management (ASPM)
    - Supports L0, L0s, L1, L2/L3 Ready, and L3 link states
    - Configurable L0s and L1 entry timers allow performance/power-savings tuning
  - SerDes power savings
    - Supports low swing / half-swing SerDes operation
    - SerDes associated with unused ports are turned off
    - SerDes associated with unused lanes are placed in a low power state
- Reliability, Availability, and Serviceability (RAS)
  - ECRC support
  - AER on all ports
  - SECDED ECC protection on all internal RAMs
  - End-to-end data path parity protection
  - Checksum Serial EEPROM content protected
  - Ability to generate an interrupt (INTx or MSI) on link up/down transitions
- Initialization / Configuration
  - Supports Root (BIOS, OS, or driver), Serial EEPROM, or SMBus switch initialization
  - Common switch configurations are supported with pin strapping (no external components)
  - Supports in-system Serial EEPROM initialization/programming
- On-Die Temperature Sensor
  - Range of 0 to 127.5 degrees Celsius
  - Three programmable temperature thresholds with over and under temperature threshold alarms
  - Automatic recording of maximum high or minimum low temperature
- 9 General Purpose I/O
- Test and Debug
  - Ability to inject AER errors simplifies in system error handling software validation
  - On-chip link activity and status outputs available for several ports
  - Per port link activity and status outputs available using external I^2C I/O expander for all remaining ports
  - Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG
- Standards and Compatibility
  - PCI Express Base Specification 2.1 compliant
  - Implements the following optional PCI Express features
    - Advanced Error Reporting (AER) on all ports
    - End-to-End CRC (ECRC)
    - Access Control Services (ACS)
    - Device Serial Number Enhanced Capability
    - Sub-System ID and Sub-System Vendor ID Capability
    - Internal Error Reporting
    - Multicast
    - VGA and ISA enable
    - L0s and L1 ASPM
    - ARI
- Power Supplies
  - Requires three power supply voltages (1.0V, 2.5V, and 3.3V)
- Packaged in a 23mm x 23mm 484-ball Flip Chip BGA with 1mm ball spacing

Product Description

With Non-Transparent Bridging functionality and innovative Switch Partitioning feature, the PES32NT24AG2 allows true multi-host or multi-processor communications in a single device. Integrated DMA controllers enable high-performance system design by off-loading data transfer operations across memories from the processors. Each lane is capable of 5 GT/s link speed in both directions and is fully compliant with PCI Express Base Specification 2.1.

A non-transparent bridge (NTB) is required when two PCI Express domains need to communicate to each other. The main function of the NTB block is to initialize and translate addresses and device IDs to allow data exchange across PCI Express domains. The major functionalities of the NTB block are summarized in Table 1.

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Block Diagram

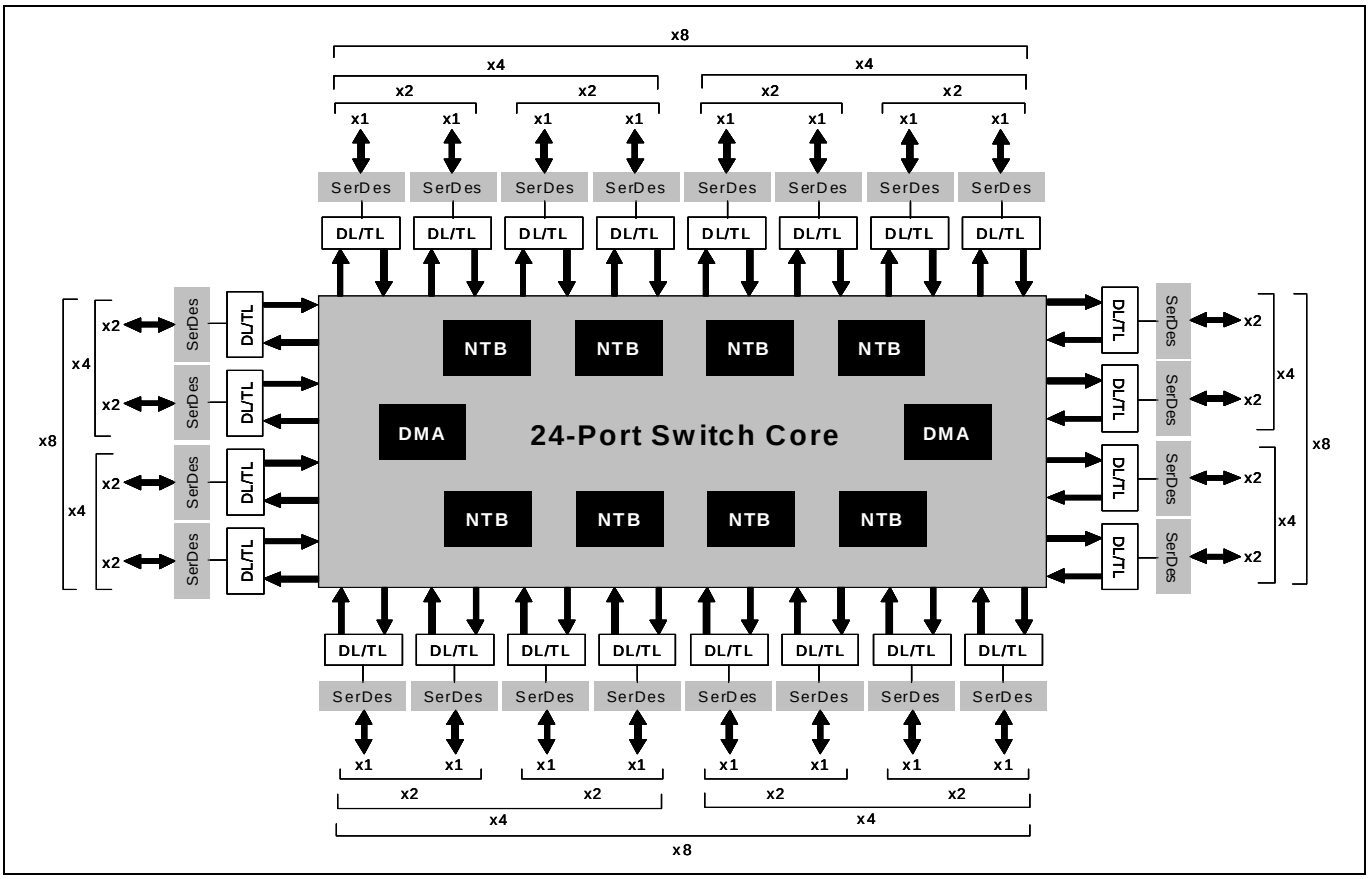

Figure 1 PES32NT24AG2 Block Diagram

Function	Number	Description
NTB ports	Up to 8	Each device can be configured to have up to 8 NTB functions and can support up to 8 CPUs/roots.
Mapping table entries	Up to 64 for entire device	Each device can have up to 64 masters ID for address and ID translations.
Mapping windows	Six 32-bits or three 64-bits	Each NT port has six BARs, where each BAR opening an NT window to another domain.
Address translation	Direct-address and lookup table trans-lations	Lookup-table translation divides the BAR aperture into up to 24 segments, where each segment has independent translation programming and is associated with an entry in a look-up table.
Doorbell registers	32 bits	Doorbell register is used for event signaling between domains, where an outbound doorbell bit sets a corresponding bit at the inbound doorbell in the other domain.
Message registers	4 inbound and out-bound registers of 32-bits	Message registers allow mailbox message passing between domains -- message placed in the inbound register will be seen at the outbound register at the other domain.

Table 1 Non-Transparent Bridge Function Summary

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SMBus Interface

The PES32NT24AG2 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES32NT24AG2, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES32NT24AG2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Each of the two SMBus interfaces contain an SMBus clock pin and an SMBus data pin. In addition, the slave SMBus has SSMBADDR1 and SSMBADDR2 pins. As shown in Figure 2, the master and slave SMBuses may only be used in a split configuration. In the split configuration, the master and slave SMBuses operate as two independent buses; thus, multi-master arbitration is not required. The SMBus master interface does not support SMBus arbitration. As a result, the switch's SMBus master must be the only master in the SMBus lines that connect to the serial EEPROM and I/O expander slaves.

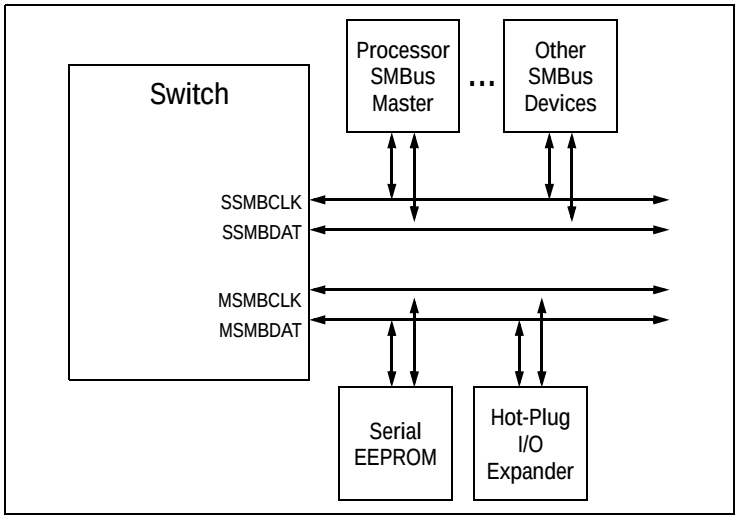

Figure 2 Split SMBus Interface Configuration

Hot-Plug Interface

The PES32NT24AG2 supports PCI Express Hot-Plug on each downstream port (ports 1 through 23). To reduce the number of pins required on the device, the PES32NT24AG2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES32NT24AG2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEXPINTN input pin (alternate function of GPIO) of the PES32NT24AG2. In response to an I/O expander interrupt, the PES32NT24AG2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES32NT24AG2 provides 9 General Purpose I/O (GPIO) pins that may be individually configured as general purpose inputs, general purpose outputs, or alternate functions. All GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES32NT24AG2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level. Differential signals end with a suffix "N" or "P." The differential signal ending in "P" is the positive portion of the differential pair and the differential signal ending in "N" is the negative portion of the differential pair.

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Signal	Type	Name/Description
PE00RN[1:0] PE00RP[1:0]	I	**PCI Express Port 0 Serial Data Receive.** Differential PCI Express receive pairs for port 0.
PE00TN[1:0] PE00TP[1:0]	O	**PCI Express Port 0 Serial Data Transmit.** Differential PCI Express transmit pairs for port 0.
PE01RN[1:0] PE01RP[1:0]	I	**PCI Express Port 1 Serial Data Receive.** Differential PCI Express receive pairs for port 1.
PE01TN[1:0] PE01TP[1:0]	O	**PCI Express Port 1 Serial Data Transmit.** Differential PCI Express transmit pairs for port 1.
PE02RN[1:0] PE02RP[1:0]	I	**PCI Express Port 2 Serial Data Receive.** Differential PCI Express receive pairs for port 2.
PE02TN[1:0] PE02TP[1:0]	O	**PCI Express Port 2 Serial Data Transmit.** Differential PCI Express transmit pairs for port 2.
PE03RN[1:0] PE03RP[1:0]	I	**PCI Express Port 3 Serial Data Receive.** Differential PCI Express receive pairs for port 3.
PE03TN[1:0] PE03TP[1:0]	O	**PCI Express Port 3 Serial Data Transmit.** Differential PCI Express transmit pairs for port 3.
PE04RN[1:0] PE04RP[1:0]	I	**PCI Express Port 4 Serial Data Receive.** Differential PCI Express receive pairs for port 4.
PE04TN[1:0] PE04TP[1:0]	O	**PCI Express Port 4 Serial Data Transmit.** Differential PCI Express transmit pairs for port 4.
PE05RN[1:0] PE05RP[1:0]	I	**PCI Express Port 5 Serial Data Receive.** Differential PCI Express receive pairs for port 5.
PE05TN[1:0] PE05TP[1:0]	O	**PCI Express Port 5 Serial Data Transmit.** Differential PCI Express transmit pairs for port 5.
PE06RN[1:0] PE06RP[1:0]	I	**PCI Express Port 6 Serial Data Receive.** Differential PCI Express receive pairs for port 6.
PE06TN[1:0] PE06TP[1:0]	O	**PCI Express Port 6 Serial Data Transmit.** Differential PCI Express transmit pairs for port 6.
PE07RN[1:0] PE07RP[1:0]	I	**PCI Express Port 7 Serial Data Receive.** Differential PCI Express receive pairs for port 7.
PE07TN[1:0] PE07TP[1:0]	O	**PCI Express Port 7 Serial Data Transmit.** Differential PCI Express transmit pairs for port 7.
PE08RN[0] PE08RP[0]	I	**PCI Express Port 8 Serial Data Receive.** Differential PCI Express receive pair for port 8.
PE08TN[0] PE08TP[0]	O	**PCI Express Port 8 Serial Data Transmit.** Differential PCI Express transmit pair for port 8.
PE09RN[0] PE09RP[0]	I	**PCI Express Port 9 Serial Data Receive.** Differential PCI Express receive pair for port 9.
PE09TN[[0] PE09TP[0]	O	**PCI Express Port 9 Serial Data Transmit.** Differential PCI Express transmit pair for port 9.
PE10RN[0] PE10RP[0]	I	**PCI Express Port 10 Serial Data Receive.** Differential PCI Express receive pair for port 10.

Table 2 PCI Express Interface Pins (Part 1 of 3)

Signal	Type	Name/Description
PE10TN[0] PE10TP[0]	O	PCI Express Port 10 Serial Data Transmit. Differential PCI Express transmit pair for port 10.
PE11RN[0] PE11RP[0]	I	PCI Express Port 11 Serial Data Receive. Differential PCI Express receive pair for port 11.
PE11TN[0] PE11TP[0]	O	PCI Express Port 11 Serial Data Transmit. Differential PCI Express transmit pair for port 11.
PE12RN[0] PE12RP[0]	I	PCI Express Port 12 Serial Data Receive. Differential PCI Express receive pair for port 12.
PE12TN[0] PE12TP[0]	O	PCI Express Port 12 Serial Data Transmit. Differential PCI Express transmit pair for port 12.
PE13RN[0] PE13RP[0]	I	PCI Express Port 13 Serial Data Receive. Differential PCI Express receive pair for port 13.
PE13TN[0] PE13TP[0]	O	PCI Express Port 13 Serial Data Transmit. Differential PCI Express transmit pair for port 13. W
PE14RN[0] PE14RP[0]	I	PCI Express Port 14 Serial Data Receive. Differential PCI Express receive pair for port 14.
PE14TN[0] PE14TP[0]	O	PCI Express Port 14 Serial Data Transmit. Differential PCI Express transmit pair for port 14.
PE15RN[0] PE15RP[0]	I	PCI Express Port 15 Serial Data Receive. Differential PCI Express receive pair for port 15.
PE15TN[0] PE15TP[0]	O	PCI Express Port 15 Serial Data Transmit. Differential PCI Express transmit pair for port 15.
PE16RN[0] PE16RP[0]	I	PCI Express Port 16 Serial Data Receive. Differential PCI Express receive pair for port 16.
PE16TN[0] PE16TP[0]	O	PCI Express Port 16 Serial Data Transmit. Differential PCI Express transmit pair for port 16.
PE17RN[0] PE17RP[0]	I	PCI Express Port 17 Serial Data Receive. Differential PCI Express receive pair for port 17.
PE17TN[0] PE17TP[0]	O	PCI Express Port 17 Serial Data Transmit. Differential PCI Express transmit pair for port 17.
PE18RN[0] PE18RP[0]	I	PCI Express Port 18 Serial Data Receive. Differential PCI Express receive pair for port 18.
PE18TN[0] PE18TP[0]	O	PCI Express Port 18 Serial Data Transmit. Differential PCI Express transmit pair for port 18.
PE19RN[0] PE19RP[0]	I	PCI Express Port 19 Serial Data Receive. Differential PCI Express receive pair for port 19.
PE19TN[0] PE19TP[0]	O	PCI Express Port 19 Serial Data Transmit. Differential PCI Express transmit pair for port 19.
PE20RN[0] PE20RP[0]	I	PCI Express Port 20 Serial Data Receive. Differential PCI Express receive pair for port 20.
PE20TN[0] PE20TP[0]	O	PCI Express Port 20 Serial Data Transmit. Differential PCI Express transmit pair for port 20.
PE21RN[0] PE21RP[0]	I	PCI Express Port 21 Serial Data Receive. Differential PCI Express receive pair for port 21.

Table 2 PCI Express Interface Pins (Part 2 of 3)

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Signal	Type	Name/Description
PE21TN[0] PE21TP[0]	O	**PCI Express Port 21 Serial Data Transmit.** Differential PCI Express transmit pair for port 21.
PE22RN[0] PE22RP[0]	I	**PCI Express Port 22 Serial Data Receive.** Differential PCI Express receive pair for port 22.
PE22TN[0] PE22TP[0]	O	**PCI Express Port 22 Serial Data Transmit.** Differential PCI Express transmit pair for port 22.
PE23RN[0] PE23RP[0]	I	**PCI Express Port 23 Serial Data Receive.** Differential PCI Express receive pair for port 23.
PE23TN[0] PE23TP[0]	O	**PCI Express Port 23 Serial Data Transmit.** Differential PCI Express transmit pair for port 23.

Table 2 PCI Express Interface Pins (Part 3 of 3)

Signal	Type	Name/Description
GCLKN[1:0] GCLKP[1:0]	I	**Global Reference Clock.** Differential reference clock input pairs. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic. The frequency of the differential reference clock is determined by the GCLKFSEL signal. Note: Both pairs of the Global Reference Clocks must be connected to and derived from the same clock source. Refer to the Overview section of Chapter 2 in the PES32NT24xG2 User Manual for additional details.
P00CLKN P00CLKP	I	**Port Reference Clock**. Differential reference clock pair associated with port 0.
P02CLKN P02CLKP	I	**Port Reference Clock**. Differential reference clock pair associated with port 2.
P04CLKN P04CLKP	I	**Port Reference Clock**. Differential reference clock pair associated with port 4.
P06CLKN P06CLKP	I	**Port Reference Clock**. Differential reference clock pair associated with port 6.
P08CLKN P08CLKP	I	**Port Reference Clock**. Differential reference clock pair associated with port 8.
P12CLKN P12CLKP	I	**Port Reference Clock**. Differential reference clock pair associated with port 12.
P16CLKN P16CLKP	I	**Port Reference Clock**. Differential reference clock pair associated with port 16.
P20CLKN P20CLKP	I	**Port Reference Clock**. Differential reference clock pair associated with port 20.

Table 3 Reference Clock Pins

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Signal	Type	Name/Description
MSMBCLK	I/O	**Master SMBus Clock.** This bidirectional signal is used to synchronize transfers on the master SMBus. It is active and generating the clock only when the EEPROM or I/O Expanders are being accessed.
MSMBDAT	I/O	**Master SMBus Data.** This bidirectional signal is used for data on the master SMBus.
SSMBADDR[2,1]	I	**Slave SMBus Address.** These pins determine the SMBus address to which the slave SMBus interface responds.
SSMBCLK	I/O	**Slave SMBus Clock.** This bidirectional signal is used to synchronize transfers on the slave SMBus.
SSMBDAT	I/O	**Slave SMBus Data.** This bidirectional signal is used for data on the slave SMBus.

Table 4 SMBus Interface Pins

Signal	Type	Name/Description
GPIO[0]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: PART0PERSTN 1st Alternate function pin type: Input/Output 1st Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition. 2nd Alternate function pin name: P16LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 16 Link Up Status output.
GPIO[1]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: PART1PERSTN 1st Alternate function pin type: Input/Output 1st Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition. 2nd Alternate function pin name: P16ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 16 Link Active Status Output.
GPIO[2]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: PART2PERSTN 1st Alternate function pin type: Input/Output 1st Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition. 2nd Alternate function pin name: P4LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 4 Link Up Status output.
GPIO[3]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: PART3PERSTN 1st Alternate function pin type: Input/Output 1st Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition. 2nd Alternate function pin name: P4ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 4 Link Active Status Output.

Table 5 General Purpose I/O Pins (Part 1 of 2)

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Signal	Type	Name/Description
GPIO[4]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: FAILOVER0 1st Alternate function pin type: Input 1st Alternate function: When this signal changes state and the corresponding failover capability is enabled, a failover event is signaled. 2nd Alternate function pin name: P0LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Up Status output.
GPIO[5]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: GPEN 1st Alternate function pin type: Output 1st Alternate function: Hot-plug general purpose even output. 2nd Alternate function pin name: P0ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Active Status Output.
GPIO[6]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: FAILOVER1 1st Alternate function pin type: Input 1st Alternate function: When this signal changes state and the corresponding failover capability is enabled, a failover event is signaled. 2nd Alternate function pin name: FAILOVER3 2nd Alternate function pin type: Input 2nd Alternate function: When this signal changes state and the corresponding failover capability is enabled, a failover event is signaled.
GPIO[7]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: FAILOVER2 1st Alternate function pin type: Input 1st Alternate function: When this signal changes state and the corresponding failover capability is enabled, a failover event is signaled. 2nd Alternate function pin name: P8LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 8 Link Up Status output.
GPIO[8]	I/O	General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: IOEXPINTN 1st Alternate function pin type: Input 1st Alternate function: IO expander interrupt. 2nd Alternate function pin name: P8ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 8 Link Active Status Output.

Table 5 General Purpose I/O Pins (Part 2 of 2)

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Signal	Type	Name/Description
STK0CFG[1:0]	I	**Stack 0 Configuration.** These pins select the configuration of stack 0.
STK1CFG[1:0]	I	**Stack 1 Configuration.** These pins select the configuration of stack 1.
STK2CFG[4:0]	I	**Stack 2 Configuration.** These pins select the configuration of stack 2.
STK3CFG[4:0]	I	**Stack 3 Configuration.** These pins select the configuration of stack 3.

Table 6 Stack Configuration Pins

Signal	Type	Name/Description
CLKMODE[1:0]	I	**Clock Mode.** These signals determine the port clocking mode used by ports of the device.
GCLKFSEL	I	**Global Clock Frequency Select.** These signals select the frequency of the GCLKP and GCLKN signals. 0x0 100 MHz 0x1 125 MHz
PERSTN	I	**Fundamental Reset.** Assertion of this signal resets all logic inside the device.
RSTHALT	I	**Reset Halt.** When this signal is asserted during a switch fundamental reset sequence, the switch remains in a quasi-reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the quasi-reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master.
SWMODE[3:0]	I	**Switch Mode.** These configuration pins determine the switch operating mode. These pins should be static and not change following the negation of PERSTN. 0x0 - Single partition 0x1 - Single partition with Serial EEPROM initialization 0x2 - Single partition with Serial EEPROM Jump 0 initialization 0x3 - Single partition with Serial EEPROM Jump 1 initialization 0x4 through 0x7 - Reserved 0x8 - Single partition with reduced latency 0x9 - Single partition with Serial EEPROM initialization and reduced latency 0xA - Multi-partition with Unattached ports 0xB - Multi-partition with Unattached ports and I^2C Reset 0xC - Multi-partition with Unattached ports and Serial EEPROM initialization 0xD - Multi-partition with Unattached ports with I^2C Reset and Serial EEPROM initialization 0xE - Multi-partition with Disabled ports 0xF - Multi-partition with Disabled ports and Serial EEPROM initialization

Table 7 System Pins

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Signal	Type	Name/Description
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic or JTAG Controller.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board

Table 8 Test Pins

Signal	Type	Name/Description
REFRES[7:0]	—	**External Reference Resistor**. Reference for the corresponding SerDes bias currents and PLL calibration circuitry. A 3K Ohm +/- 1% resistor should be connected from this pin to ground and isolated from any source of noise injection. Each bit of this signal corresponds to a SerDes quad, e.g., REFRES[5] is the reference resistor for SerDes quad 5.
REFRESPLL	—	**PLL External Reference Resistor**. Provides a reference for the PLL bias currents and PLL calibration circuitry. A 3K Ohm +/- 1% resistor should be connected from this pin to ground and isolated from any source of noise injection.
V_{DD}CORE	—	**Core $V_{DD.}$** Power supply for core logic (1.0V).
V_{DD}I/O	—	**I/O $V_{DD.}$** LVTTL I/O buffer power supply (3.3V).
V_{DD}PEA	—	**PCI Express Analog Power**. Serdes analog power supply (1.0V).
V_{DD}PEHA	—	**PCI Express Analog High Power**. Serdes analog power supply (2.5V).
V_{DD}PETA	—	**PCI Express Transmitter Analog Voltage**. Serdes transmitter analog power supply (1.0V).
V_{SS}	—	**Ground**.

Table 9 Power, Ground, and SerDes Resistor Pins

Pin Characteristics

Note: Some input pads of the switch do not contain internal pull-ups or pull-downs. Unused SMBus and System inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, floating pins can cause a slight increase in power consumption. Unused Serdes (Rx and Tx) pins should be left floating. Finally, No Connection pins should not be connected.

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface	PE00RN[1:0]	I	PCIe differential[2]	Serial Link		Note: Unused SerDes pins can be left floating
	PE00RP[1:0]	I				
	PE00TN[1:0]	O				
	PE00TP[1:0]	O				
	PE01RN[1:0]	I				
	PE01RP[1:0]	I				
	PE01TN[1:0]	O				
	PE01TP[1:0]	O				
	PE02RN[1:0]	I				
	PE02RP[1:0]	I				
	PE02TN[1:0]	O				
	PE02TP[1:0]	O				
	PE03RN[1:0]	I				
	PE03RP[1:0]	I				
	PE03TN[1:0]	O				
	PE03TP[1:0]	O				
	PE04RN[1:0]	I				
	PE04RP[1:0]	I				
	PE04TN[1:0]	O				
	PE04TP[1:0]	O				
	PE05RN[1:0]	I				
	PE05RP[1:0]	I				
	PE05TN[1:0]	O				
	PE05TP[1:0]	O				
	PE06RN[1:0]	I				
	PE06RP[1:0]	I				
	PE06TN[1:0]	O				
	PE06TP[1:0]	O				
	PE07RN[1:0]	I				
	PE07RP[1:0]	I				
	PE07TN[1:0]	O				
	PE07TP[1:0]	O				
	PE08RN[0]	I				
	PE08RP[0]	I				
	PE08TN[0]	O				

Table 10 Pin Characteristics (Part 1 of 5)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface (cont.)	PE08TP[0]	O	PCIe differential	Serial Link		
	PE09RN[0]	I				
	PE09RP[0]	I				
	PE09TN[0]	O				
	PE09TP[0]	O				
	PE10RN[0]	I				
	PE10RP[0]	I				
	PE10TN[0]	O				
	PE10TP[0]	O				
	PE11RN[0]	I				
	PE11RP[0]	I				
	PE11TN[0]	O				
	PE11TP[0]	O				
	PE12RN[0]	I				
	PE12RP[0]	I				
	PE12TN[0]	O				
	PE12TP[0]	O				
	PE13RN[0]	I				
	PE13RP[0]	I				
	PE13TN[0]	O				
	PE13TP[0]	O				
	PE14RN[0]	I				
	PE14RP[0]	I				
	PE14TN[0]	O				
	PE14TP[0]	O				
	PE15RN[0]	I				
	PE15RP[0]	I				
	PE15TN[0]	O				
	PE15TP[0]	O				
	PE16RN[0]	I				
	PE16RP[0]	I				
	PE16TN[0]	O				
	PE16TP[0]	O				
	PE17RN[0]	I				
	PE17RP[0]	I				
	PE17TN[0]	O				
	PE17TP[0]	O				

Table 10 Pin Characteristics (Part 2 of 5)

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
PCI Express Interface (cont.)	PE18RN[0]	I	PCIe differential	Serial Link		
	PE18RP[0]	I				
	PE18TN[0]	O				
	PE18TP[0]	O				
	PE19RN[0]	I				
	PE19RP[0]	I				
	PE19TN[0]	O				
	PE19TP[0]	O				
	PE20RN[0]	I				
	PE20RP[0]	I				
	PE20TN[0]	O				
	PE20TP[0]	O				
	PE21RN[0]	I				
	PE21RP[0]	I				
	PE21TN[0]	O				
	PE21TP[0]	O				
	PE22RN[0]	I				
	PE22RP[0]	I				
	PE22TN[0]	O				
	PE22TP[0]	O				
	PE23RN[0]	I				
	PE23RP[0]	I				
	PE23TN[0]	O				
	PE23TP[0]	O				

Table 10 Pin Characteristics (Part 3 of 5)

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Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
Reference Clocks	GCLKN[1:0]	I	HCSL	Diff. Clock Input		Refer to Table 11 Note: Unused port clock pins should be connected to Vss on the board.
	GCLKP[1:0]	I				
	P00CLKN	I				
	P00CLKP	I				
	P02CLKN	I				
	P02CLKP	I				
	P04CLKN	I				
	P04CLKP	I				
	P06CLKN	I				
	P06CLKP	I				
	P08CLKN	I				
	P08CLKP	I				
	P12CLKN	I				
	P12CLKP	I				
	P16CLKN	I				
	P16CLKP	I				
	P20CLKN	I				
	P20CLKP	I				
SMBus	MSMBCLK	I/O	LVTTL	STI[3]	Note: When unused, these signals must be pulled up on the board using an external resistor or current source in accordance with the SMBus specification.	
	MSMBDAT	I/O		STI		
	SSMBADDR[2,1]	I			pull-up	
	SSMBCLK	I/O		STI	Note: When unused, these signals must be pulled up on the board using an external resistor or current source in accordance with the SMBus specification.	
	SSMBDAT	I/O		STI		
General Purpose I/O	GPIO[8:0]	I/O	LVTTL	STI, High Drive	pull-up	Unused pins can be left floating.
Stack Configuration	STK0CFG[1:0]	I	LVTTL	Input	pull-down	Unused pins can be left floating.
	STK1CFG[1:0]	I			pull-down	
	STK2CFG[4:0]	I			pull-down	
	STK3CFG[4:0]	I			pull-down	

Table 10 Pin Characteristics (Part 4 of 5)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor[1]	Notes
System Pins	CLKMODE[1:0]	I	LVTTL	Input	pull-up	Unused pins can be left floating.
	GCLKFSEL	I			pull-down	
	PERSTN	I				Schmitt trigger
	RSTHALT	I			pull-down	Unused pins can be left floating.
	SWMODE[3:0]	I			pull-down	
EJTAG / JTAG	JTAG_TCK	I	LVTTL	STI	pull-up	Unused pins can be left floating.
	JTAG_TDI	I		STI	pull-up	
	JTAG_TDO	O				
	JTAG_TMS	I		STI	pull-up	
	JTAG_TRST_N	I		STI	pull-up	
SerDes Reference Resistors	REFRES[7:0]	—	Analog			Unused pins should be connected to Vss on the board.
	REFRESPLL	—				

Table 10 Pin Characteristics (Part 5 of 5)

1. Internal resistor values under typical operating conditions are 92K Ω for pull-up and 91K Ω for pull-down.

2. All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.

3. Schmitt Trigger Input (STI).

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Logic Diagram — PES32NT24AG2

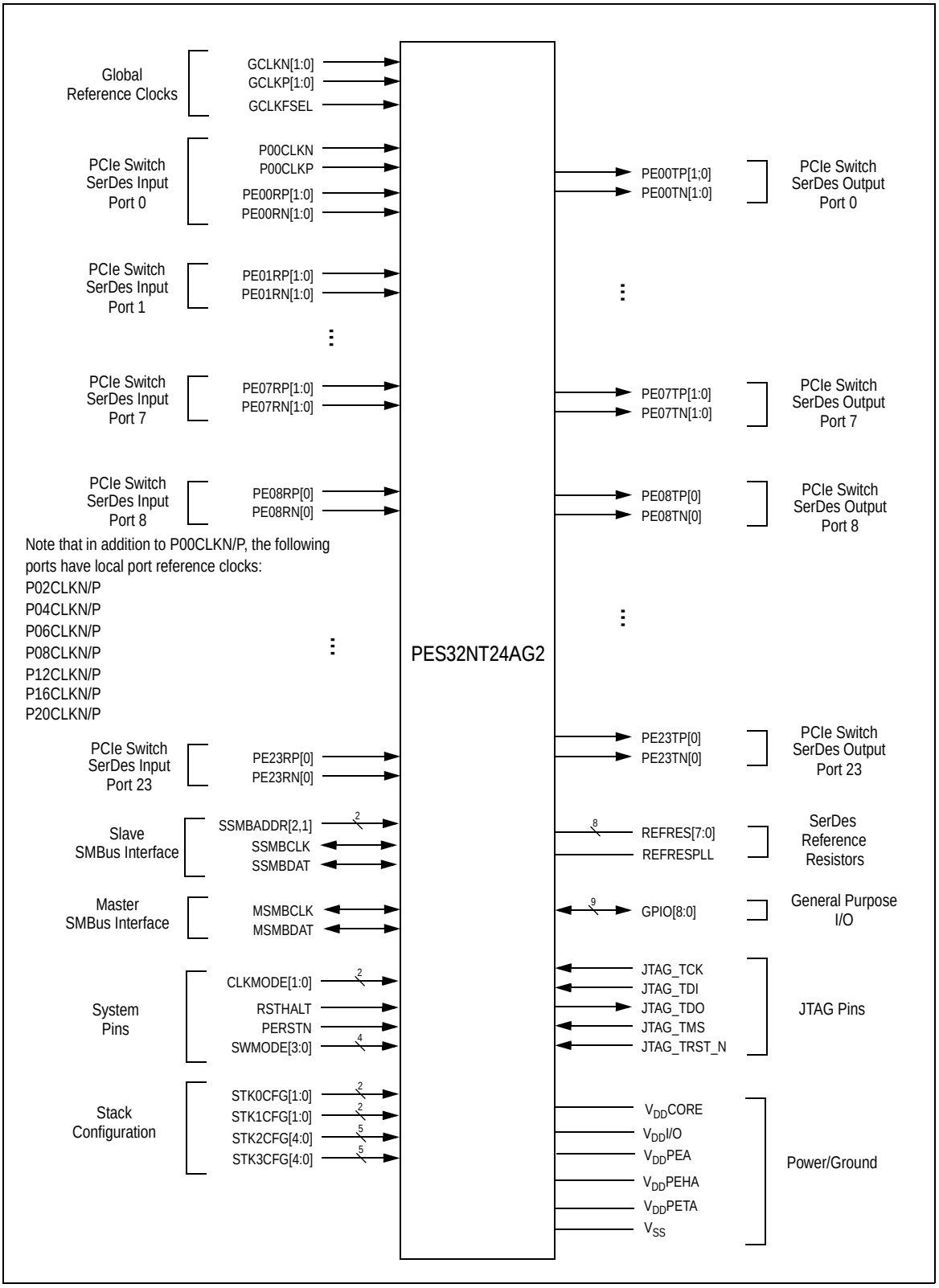

Figure 3 PES32NT24AG2 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 16 and 15.

Parameter	Description	Condition	Min	Typical	Max	Unit
$Refclk_{FREQ}$	Input reference clock frequency range		100		125[1]	MHz
T_{C-RISE}	Rising edge rate	Differential	0.6		4	V/ns
T_{C-FALL}	Falling edge rate	Differential	0.6		4	V/ns
V_{IH}	Differential input high voltage	Differential	+150			mV
V_{IL}	Differential input low voltage	Differential			-150	mV
V_{CROSS}	Absolute single-ended crossing point voltage	Single-ended	+250		+550	mV
$V_{CROSS-DELTA}$	Variation of V_{CROSS} over all rising clock edges	Single-ended			+140	mV
V_{RB}	Ring back voltage margin	Differential	-100		+100	mV
T_{STABLE}	Time before V_{RB} is allowed	Differential	500			ps
$T_{PERIOD-AVG}$	Average clock period accuracy		-300		2800	ppm
$T_{PERIOD-ABS}$	Absolute period, including spread-spectrum and jitter		9.847		10.203	ns
$T_{CC-JITTER}$	Cycle to cycle jitter				150	ps
V_{MAX}	Absolute maximum input voltage				+1.15	V
V_{MIN}	Absolute minimum input voltage		-0.3			V
Duty Cycle	Duty cycle		40		60	%
Rise/Fall Matching	Single ended rising Refclk edge rate versus falling Refclk edge rate			20		%
Z_{C-DC}	Clock source output DC impedance		40		60	Ω

Table 11 Input Clock Requirements

1. The input clock frequency will be either 100 or 125 MHz depending on signal GCLKFSEL.

Note: Refclk jitter compliant to PCIe Gen2 Common Clock architecture is adequate for the GCLKN/P[x] and PE[x]CLKN/P pins of this IDT PCIe switch. This same jitter specification is applicable when interfacing the switch to another IDT switch in a Separate (Non-Common) Clock architecture.

AC Timing Characteristics

Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
PCIe Transmit								
UI	Unit Interval	399.88	400	400.12	199.94	200	200.06	ps
T_{TX-EYE}	Minimum Tx Eye Width	0.75			0.75			UI

Table 12 PCIe AC Timing Characteristics (Part 1 of 2)

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Parameter	Description	Gen 1			Gen 2			Units
		Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]	
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median			0.125				UI
$T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$	TX Rise/Fall Time: 20% - 80%	0.125			0.15			UI
$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum time in idle	20			20			UI
$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	Maximum time to transition to a valid Idle after sending an Idle ordered set			8			8	ns
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Maximum time to transition from valid idle to diff data			8			8	ns
$T_{TX\text{-}SKEW}$	Transmitter data skew between any 2 lanes			1.3			1.3	ns
$T_{MIN\text{-}PULSED}$	Minimum Instantaneous Lone Pulse Width	NA			0.9			UI
$T_{TX\text{-}HF\text{-}DJ\text{-}DD}$	Transmitter Deterministic Jitter > 1.5MHz Bandwidth	NA					0.15	UI
$T_{RF\text{-}MISMATCH}$	Rise/Fall Time Differential Mismatch	NA					0.1	UI
PCIe Receive								
UI	Unit Interval	399.88	400	400.12	199.94		200.06	ps
$T_{RX\text{-}EYE\ (with\ jitter)}$	Minimum Receiver Eye Width (jitter tolerance)	0.4			0.4			UI
$T_{RX\text{-}EYE\text{-}MEDIUM\ TO\ MAX\ JITTER}$	Max time between jitter median & max deviation			0.3				UI
$T_{RX\text{-}SKEW}$	Lane to lane input skew			20			8	ns
$T_{RX\text{-}HF\text{-}RMS}$	1.5 — 100 MHz RMS jitter (common clock)	NA					3.4	ps
$T_{RX\text{-}HF\text{-}DJ\text{-}DD}$	Maximum tolerable DJ by the receiver (common clock)	NA					88	ps
$T_{RX\text{-}LF\text{-}RMS}$	10 KHz to 1.5 MHz RMS jitter (common clock)	NA					4.2	ps
$T_{RX\text{-}MIN\text{-}PULSE}$	Minimum receiver instantaneous eye width	NA			0.6			UI

Table 12 PCIe AC Timing Characteristics (Part 2 of 2)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Express Base Specification 2.1.

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
GPIO						
GPIO[8:0][1]	Tpw_13b[2]	None	50	—	ns	See Figure 4.

Table 13 GPIO AC Timing Characteristics

1. GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

2. The values for this symbol were determined by calculation, not by testing.

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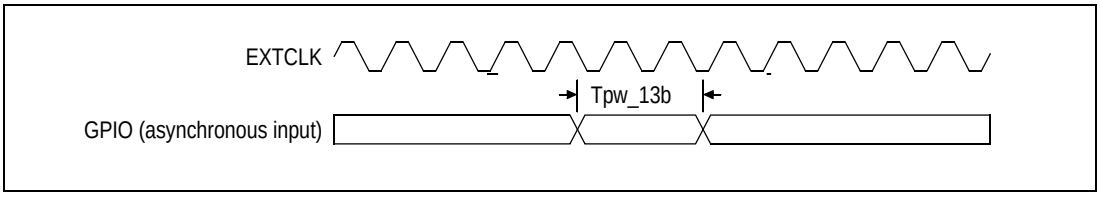

Figure 4 GPIO AC Timing Waveform

Signal	Symbol	Reference Edge	Min	Max	Unit	Timing Diagram Reference
JTAG						
JTAG_TCK	Tper_16a	none	50.0	—	ns	See Figure 5.
	Thigh_16a, Tlow_16a		10.0	25.0	ns	
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	ns	
	Thld_16b		1.0	—	ns	
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	20	ns	
	Tdz_16c[2]		—	20	ns	
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	ns	

Table 14 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

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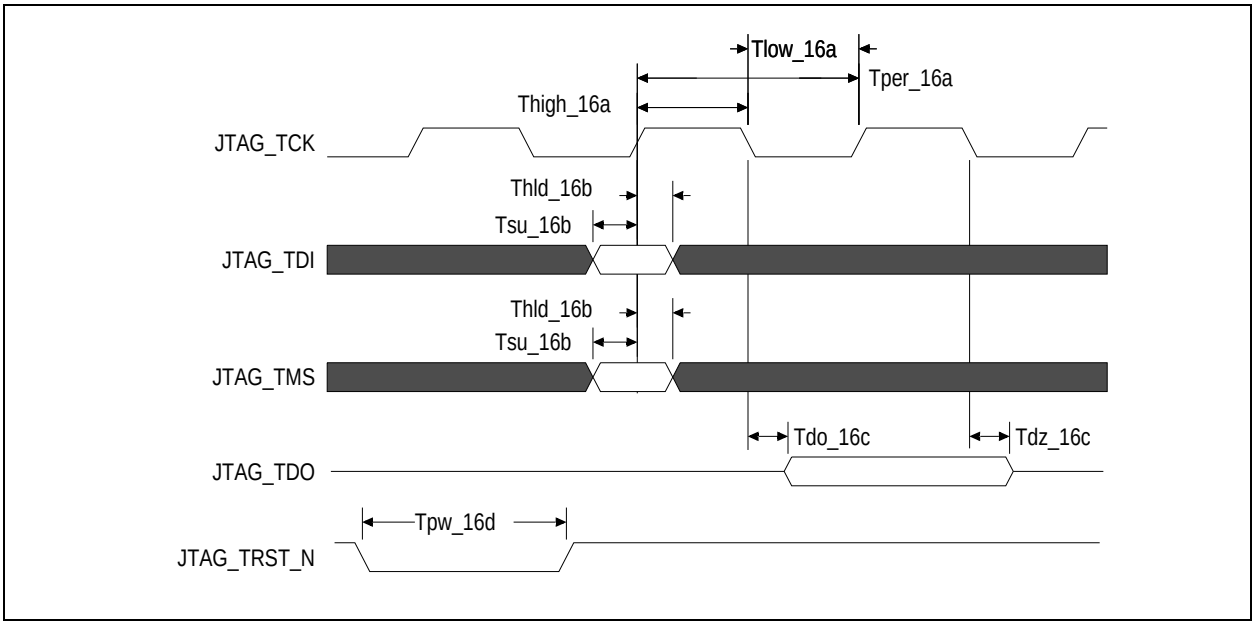

Figure 5 JTAG AC Timing Waveform

Recommended Operating Temperature

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 15 PES32NT24AG2 Operating Temperatures

Recommended Operating Supply Voltages — Commercial Temperature

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes	3.125	3.3	3.465	V
V_{DD}PEA[1]	PCI Express Analog Power	0.95	1.0	1.1	V
V_{DD}PEHA[2]	PCI Express Analog High Power	2.25	2.5	2.75	V
V_{DD}PETA[1]	PCI Express Transmitter Analog Voltage	0.95	1.0	1.1	V
V_{SS}	Common ground	0	0	0	V

Table 16 PES32NT24AG2 Operating Voltages — Commercial Temperature

1. V_{DD}PEA and V_{DD}PETA should have no more than 25m$V_{peak\text{-}peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.

2. V_{DD}PEHA should have no more than 50m$V_{peak\text{-}peak}$ AC power supply noise superimposed on the 2.5V nominal DC value.

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Recommended Operating Supply Voltages — Industrial Temperature

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}CORE	Internal logic supply	0.9	1.0	1.1	V
V_{DD}I/O	I/O supply except for SerDes	3.125	3.3	3.465	V
V_{DD}PEA[1]	PCI Express Analog Power	0.95	1.0	1.05	V
V_{DD}PEHA[2]	PCI Express Analog High Power	2.25	2.5	2.75	V
V_{DD}PETA[1]	PCI Express Transmitter Analog Voltage	0.95	1.0	1.1	V
V_{SS}	Common ground	0	0	0	V

Table 17 PES32NT24AG2 Operating Voltages — Industrial Temperature

1. V_{DD}PEA and V_{DD}PETA should have no more than 25m$V_{peak-peak}$ AC power supply noise superimposed on the 1.0V nominal DC value.

2. V_{DD}PEHA should have no more than 50m$V_{peak-peak}$ AC power supply noise superimposed on the 2.5V nominal DC value.

Power-Up/Power-Down Sequence

During power supply ramp-up, V_{DD}CORE must remain at least 1.0V below V_{DD}I/O at all times. There are no other power-up sequence requirements for the various operating supply voltages. The power-down sequence can occur in any order.

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 16 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 16 (and also listed below).

Number of Active Lanes per Port		Core Supply		PCIe Analog Supply		PCIe Analog High Supply		PCIe Transmitter Supply		I/O Supply		Total	
		Typ 1.0V	Max 1.1V	Typ 1.0V	Max 1.1V	Typ 2.5V	Max 2.75V	Typ 1.0V	Max 1.1V	Typ 3.3V	Max 3.465	Typ Power	Max Power
x8/x8/x8/x4/x4 (Full Swing)	mA	2535	3400	1627	1855	233	233	687	740	3	5		
	Watts	2.54	3.74	1.63	2.04	0.58	0.64	0.69	0.81	0.01	0.02	5.45	7.25
x8/x8/x8/x4/x4 (Half Swing)	mA	2535	3400	1399	1595	233	233	357	385	3	5		
	Watts	2.54	3.74	1.40	1.76	0.58	0.64	0.36	0.42	0.01	.02	4.89	6.58

Table 18 PES32NT24AG2 Power Consumption

Note 1: The above power consumption assumes that all ports are functioning at Gen2 (5.0 GT/S) speeds. Power consumption can be reduced by turning off unused ports through software or through boot EEPROM. Power savings will occur in V_{DD}PEA, V_{DD}PEHA, and V_{DD}PETA. Power savings can be estimated as directly proportional to the number of unused ports, since the power consumption of a turned-off port is close to zero. For example, if 3 ports out of 16 are turned off, then the power savings for each of the above three power rails can be calculated quite simply as 3/16 multiplied by the power consumption indicated in the above table.

Note 2: Using a port in Gen1 mode (2.5GT/S) results in approximately 18% power savings for each power rail: V_{DD}PEA, V_{DD}PEHA, and V_{DD}PETA.

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Thermal Considerations

This section describes thermal considerations for the PES32NT24AG2 (23mm^2 FCBGA484 package). The data in Table 19 below contains information that is relevant to the thermal performance of the PES32NT24AG2 switch.

Symbol	Parameter	Value	Units	Conditions
$T_{J(max)}$	Junction Temperature	125	^{0}C	Maximum
$T_{A(max)}$	Ambient Temperature	70	^{0}C	Maximum for commercial-rated products
		85	^{0}C	Maximum for industrial-rated products
$\theta_{JA(effective)}$	Effective Thermal Resistance, Junction-to-Ambient	15.2	^{0}C/W	Zero air flow
		8.5	^{0}C/W	1 m/S air flow
		7.1	^{0}C/W	2 m/S air flow
θ_{JB}	Thermal Resistance, Junction-to-Board	3.1	^{0}C/W	
θ_{JC}	Thermal Resistance, Junction-to-Case	0.15	^{0}C/W	
P	Power Dissipation of the Device	7.25	Watts	Maximum

Table 19 Thermal Specifications for PES32NT24AG2, 23x23 mm FCBGA484 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 19. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 19), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

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DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 16.

Note: See Table 10, Pin Characteristics, for a complete I/O listing.

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Condi-tions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link	PCIe Transmit									
	$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	800		1200	800		1200	mV	
	$V_{TX-DIFFp-p-LOW}$	Low-Drive Differential Peak to Peak Output Voltage	400		1200	400		1200	mV	
	$V_{TX-DE-RATIO-3.5dB}$	De-emphasized differential output voltage	-3		-4	-3.0	-3.5	-4.0	dB	
	$V_{TX-DE-RATIO-6.0dB}$	De-emphasized differential output voltage	NA			-5.5	-6.0	-6.5	dB	
	$V_{TX-DC-CM}$	DC Common mode voltage	0		3.6	0		3.6	V	
	$V_{TX-CM-ACP}$	RMS AC peak common mode output voltage			20				mV	
	$V_{TX-CM-DC-active-idle-delta}$	Abs delta of DC common mode voltage between L0 and idle			100			100	mV	
	$V_{TX-CM-DC-line-delta}$	Abs delta of DC common mode voltage between D+ and D-			25			25	mV	
	$V_{TX-Idle-DiffP}$	Electrical idle diff peak output			20			20	mV	
	$RL_{TX-DIFF}$	Transmitter Differential Return loss	10					10	dB	0.05 - 1.25GHz
								8	dB	1.25 - 2.5GHz
	RL_{TX-CM}	Transmitter Common Mode Return loss	6					6	dB	
	$Z_{TX-DIFF-DC}$	DC Differential TX impedance	80	100	120			120	Ω	
	VTX-CM-ACpp	Peak-Peak AC Common	NA					100	mV	
	$V_{TX-DC-CM}$	Transmit Driver DC Common Mode Voltage	0		3.6	0		3.6	V	
	$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detec-tion			600			600	mV	
	$I_{TX-SHORT}$	Transmitter Short Circuit Current Limit	0		90				90	mA

Table 20 DC Electrical Characteristics (Part 1 of 3)

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Condi-tions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Serial Link (cont.)	PCIe Receive									
	$V_{RX-DIFFp-p}$	Differential input voltage (peak-to-peak)	175		1200	120		1200	mV	
	$RL_{RX-DIFF}$	Receiver Differential Return Loss	10					10	dB	0.05 - 1.25GHz
								8		1.25 - 2.5GHz
	RL_{RX-CM}	Receiver Common Mode Return Loss	6					6	dB	
	$Z_{RX-DIFF-DC}$	Differential input impedance (DC)	80	100	120	Refer to return loss spec			Ω	
	Z_{RX--DC}	DC common mode impedance	40	50	60	40		60	Ω	
	$Z_{RX-COMM-DC}$	Powered down input common mode impedance (DC)	200k	350k				50k	Ω	
	$Z_{RX-HIGH-IMP-DC-POS}$	DC input CM input impedance for V>0 during reset or power down			50k			50k	Ω	
	$Z_{RX-HIGH-IMP-DC-NEG}$	DC input CM input impedance for V<0 during reset or power down			1.0k			1.0k	Ω	
	$V_{RX-IDLE-DET-DIFFp-p}$	Electrical idle detect threshold	65		175	65		175	mV	
	$V_{RX-CM-ACp}$	Receiver AC common-mode peak voltage			150			150	mV	$V_{RX-CM-ACp}$
PCIe REFCLK										
	C_{IN}	Input Capacitance	1.5	—		1.5	—		pF	
Other I/Os										
LOW Drive Output	I_{OL}		—	2.5	—	—	2.5	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-5.5	—	—	-5.5	—	mA	V_{OH} = 1.5V
High Drive Output	I_{OL}		—	12.0	—	—	12.0	—	mA	V_{OL} = 0.4v
	I_{OH}		—	-20.0	—	—	-20.0	—	mA	V_{OH} = 1.5V
Schmitt Trig-ger Input (STI)	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—
Input	V_{IL}		-0.3	—	0.8	-0.3	—	0.8	V	—
	V_{IH}		2.0	—	V_{DD}I/O + 0.5	2.0	—	V_{DD}I/O + 0.5	V	—
3.3V Output Low Voltage	V_{OL}		—	—	0.4		—	0.4	V	I_{OL} = 8mA for JTAG_TDO and GPIO pins
3.3V Output High Voltage	V_{OH}		2.4	—	—	2.4	—	—	V	I_{OH} = 8mA for JTAG_TDO and GPIO pins
Capacitance	C_{IN}		—	—	8.5	—	—	8.5	pF	—

Table 20 DC Electrical Characteristics (Part 2 of 3)

I/O Type	Parameter	Description	Gen1			Gen2			Unit	Condi-tions
			Min[1]	Typ[1]	Max[1]	Min[1]	Typ[1]	Max[1]		
Leakage	Inputs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/downs		—	—	± 10	—	—	± 10	µA	V_{DD}I/O (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/downs		—	—	± 80	—	—	± 80	µA	V_{DD}I/O (max)

Table 20 DC Electrical Characteristics (Part 3 of 3)

1. Minimum, Typical, and Maximum values meet the requirements under PCI Express Base Specification 2.1.

Absolute Maximum Voltage Rating

Core Supply	PCIe Analog Supply	PCIe Analog High Supply	PCIe Transmitter Supply	I/O Supply
1.5V	1.5V	4.6V	1.5V	4.6V

Table 21 PES32NT24AG2 Absolute Maximum Voltage Rating

Warning: For proper and reliable operation in adherence with this data sheet, the device should not exceed the recommended operating voltages in Table 16. The absolute maximum operating voltages in Table 21 are offered to provide guidelines for voltage excursions outside the recommended voltage ranges. Device functionality is not guaranteed at these conditions and sustained operation at these values or any exposure to voltages outside the maximum range may adversely affect device functionality and reliability.

SMBus Characterization

Symbol	Parameter	SMBus 2.0 Char. Data[1]			Unit
		3V	3.3V	3.6V	
DC Parameter for SDA Pin					
V_{IL}	Input Low	1.16	1.26	1.35	V
V_{IH}	Input High	1.56	1.67	1.78	V
$V_{OL@350uA}$	Output Low	15	15	15	mV
$I_{OL@0.4V}$		23	24	25	mA
I_{Pullup}	Current Source	—	—	—	µA
I_{IL_Leak}	Input Low Leakage	0	0	0	µA
I_{IH_Leak}	Input High Leakage	0	0	0	µA

Table 22 SMBus DC Characterization Data (Part 1 of 2)

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Symbol	Parameter	SMBus 2.0 Char. Data[1]			Unit
		3V	3.3V	3.6V	
DC Parameter for SCL Pin					
$V_{IL\ (V)}$	Input Low	1.11	1.2	1.31	V
$V_{IH\ (V)}$	Input High	1.54	1.65	1.76	V
I_{IL_Leak}	Input Low Leakage	0	0	0	µA
I_{IH_Leak}	Input High Leakage	0	0	0	µA

Table 22 SMBus DC Characterization Data (Part 2 of 2)

1. Data at room and hot temperature.

Symbol	Parameter	SMBus @3.3V ±10%[1]		Unit
		Min	Max	
F_{SCL}	Clock frequency	5	600	KHz
T_{BUF}	Bus free time between Stop and Start	3.5	—	µs
$T_{HD:STA}$	Start condition hold time	1	—	µs
$T_{SU:STA}$	Start condition setup time	1	—	µs
$T_{SU:STO}$	Stop condition setup time	1	—	µs
$T_{HD:DAT}$	Data hold time	1	—	ns
$T_{SU:DAT}$	Data setup time	1	—	ns
$T_{TIMEOUT}$	Detect clock low time out	—	74.7	ms
T_{LOW}[2]	Clock low period	3.7	—	µs
T_{HIGH}[2]	Clock high period	3.7	—	µs
T_F	Clock/Data fall time	—	72.2	ns
T_R	Clock/Data rise time	—	68.3	ns
$T_{POR@10kHz}$	Time which a device must be operational after power-on reset	20	—	ms

Table 23 SMBus AC Timing Data

1. Data at room and hot temperature.

2. T_{LOW} and T_{HIGH} are measured at F_{SCL} = 135 kHz.

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Package Pinout — 484-BGA Signal Pinout for the PES32NT24AG2

The following table lists the pin numbers and signal names for the PES32NT24AG2 device. Note: Pins labeled NC are No Connection.

Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
A1	STK2CFG1		B5	PE07TN1		C9	REFRES03	
A2	STK2CFG2		B6	PE07TN0		C10	V_{SS}	
A3	STK2CFG3		B7	V_{SS}		C11	V_{SS}	
A4	V_{SS}		B8	PE06TN1		C12	V_{SS}	
A5	PE07TP1		B9	PE06TN0		C13	V_{SS}	
A6	PE07TP0		B10	V_{SS}		C14	V_{SS}	
A7	V_{SS}		B11	P06CLKN		C15	V_{SS}	
A8	PE06TP1		B12	GCLKN0		C16	NC	
A9	PE06TP0		B13	P04CLKN		C17	V_{SS}	
A10	V_{SS}		B14	V_{SS}		C18	V_{SS}	
A11	P06CLKP		B15	PE05TN1		C19	V_{SS}	
A12	GCLKP0		B16	PE05TN0		C20	MSMBDAT	
A13	P04CLKP		B17	V_{SS}		C21	SSMBDAT	
A14	V_{SS}		B18	PE04TN1		C22	JTAG_TCK	
A15	PE05TP1		B19	PE04TN0		D1	V_{SS}	
A16	PE05TP0		B20	PERSTN		D2	V_{DD}I/O	
A17	V_{SS}		B21	JTAG_TMS		D3	V_{SS}	
A18	PE04TP1		B22	CLKMODE1		D4	V_{SS}	
A19	PE04TP0		C1	STK3CFG3		D5	V_{SS}	
A20	MSMBCLK		C2	V_{SS}		D6	V_{SS}	
A21	JTAG_TDO		C3	STK3CFG4		D7	PE07RN1	
A22	JTAG_TRST_N		C4	V_{SS}		D8	PE07RN0	
B1	STK2CFG4		C5	V_{SS}		D9	V_{SS}	
B2	STK3CFG1		C6	V_{SS}		D10	PE06RN1	
B3	STK3CFG2		C7	V_{SS}		D11	PE06RN0	
B4	V_{SS}		C8	V_{SS}		D12	REFRESPLL	

Table 24 PES32NT24AG2 Signal Pin-Out (Part 1 of 7)

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Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
D13	REFRES02		E17	PE04RP1		F21	V_{SS}	
D14	PE05RN1		E18	PE04RP0		F22	V_{SS}	
D15	PE05RN0		E19	V_{DD}I/O		G1	PE08TP0	
D16	V_{SS}		E20	P02CLKP		G2	PE08TN0	
D17	PE04RN1		E21	V_{DD}I/O		G3	V_{SS}	
D18	PE04RN0		E22	V_{DD}I/O		G4	PE08RN0	
D19	V_{SS}		F1	V_{SS}		G5	PE08RP0	
D20	JTAG_TDI		F2	V_{SS}		G6	V_{DD}PETA	
D21	SSMBCLK		F3	P08CLKN		G7	V_{DD}PEHA	
D22	SSMBADDR2		F4	V_{SS}		G8	V_{SS}	
E1	V_{DD}I/O		F5	V_{SS}		G9	V_{DD}PEA	
E2	V_{DD}I/O		F6	V_{SS}		G10	V_{DD}PEA	
E3	P08CLKP		F7	V_{DD}PEHA		G11	V_{DD}PEA	
E4	V_{DD}I/O		F8	V_{DD}PEHA		G12	V_{DD}PEA	
E5	V_{SS}		F9	V_{DD}PETA		G13	V_{DD}PEA	
E6	V_{SS}		F10	V_{DD}PETA		G14	V_{DD}PEA	
E7	PE07RP1		F11	V_{DD}PETA		G15	V_{SS}	
E8	PE07RP0		F12	V_{DD}PETA		G16	V_{DD}PEHA	
E9	V_{SS}		F13	V_{DD}PETA		G17	V_{DD}PETA	
E10	PE06RP1		F14	V_{DD}PETA		G18	PE03RP1	
E11	PE06RP0		F15	V_{DD}PEHA		G19	PE03RN1	
E12	V_{SS}		F16	V_{DD}PEHA		G20	V_{SS}	
E13	V_{SS}		F17	V_{SS}		G21	PE03TN1	
E14	PE05RP1		F18	V_{SS}		G22	PE03TP1	
E15	PE05RP0		F19	V_{SS}		H1	PE09TP0	
E16	V_{SS}		F20	P02CLKN		H2	PE09TN0	

Table 24 PES32NT24AG2 Signal Pin-Out (Part 2 of 7)

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Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
H3	V_{SS}		J7	V_{DD}PEA		K11	V_{SS}	
H4	PE09RN0		J8	V_{SS}		K12	V_{SS}	
H5	PE09RP0		J9	V_{DD}CORE		K13	V_{DD}CORE	
H6	V_{DD}PETA		J10	V_{DD}CORE		K14	V_{DD}CORE	
H7	V_{DD}PEHA		J11	V_{SS}		K15	V_{SS}	
H8	V_{SS}		J12	V_{SS}		K16	V_{DD}PEA	
H9	V_{DD}CORE		J13	V_{DD}CORE		K17	REFRES01	
H10	V_{DD}CORE		J14	V_{DD}CORE		K18	PE02RP1	
H11	V_{SS}		J15	V_{SS}		K19	PE02RN1	
H12	V_{SS}		J16	V_{DD}PEA		K20	V_{SS}	
H13	V_{DD}CORE		J17	V_{DD}PETA		K21	PE02TN1	
H14	V_{DD}CORE		J18	V_{SS}		K22	PE02TP1	
H15	V_{SS}		J19	V_{SS}		L1	PE11TP0	
H16	V_{DD}PEHA		J20	V_{SS}		L2	PE11TN0	
H17	V_{DD}PETA		J21	V_{SS}		L3	V_{SS}	
H18	PE03RP0		J22	V_{SS}		L4	PE11RN0	
H19	PE03RN0		K1	PE10TP0		L5	PE11RP0	
H20	V_{SS}		K2	PE10TN0		L6	V_{DD}PEA	
H21	PE03TN0		K3	V_{SS}		L7	V_{DD}PEA	
H22	PE03TP0		K4	PE10RN0		L8	V_{SS}	
J1	V_{SS}		K5	PE10RP0		L9	V_{DD}CORE	
J2	V_{SS}		K6	REFRES04		L10	V_{DD}CORE	
J3	V_{SS}		K7	V_{DD}PEA		L11	V_{DD}CORE	
J4	V_{SS}		K8	V_{SS}		L12	V_{DD}CORE	
J5	V_{SS}		K9	V_{DD}CORE		L13	V_{DD}CORE	
J6	V_{DD}PETA		K10	V_{DD}CORE		L14	V_{DD}CORE	

Table 24 PES32NT24AG2 Signal Pin-Out (Part 3 of 7)

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Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
L15	V_{SS}		M19	V_{SS}		P1	PE13TP0	
L16	V_{DD}PEA		M20	V_{SS}		P2	PE13TN0	
L17	V_{DD}PEA		M21	V_{SS}		P3	V_{SS}	
L18	PE02RP0		M22	V_{SS}		P4	PE13RN0	
L19	PE02RN0		N1	PE12TP0		P5	PE13RP0	
L20	V_{SS}		N2	PE12TN0		P6	V_{DD}PETA	
L21	PE02TN0		N3	V_{SS}		P7	V_{DD}PEA	
L22	PE02TP0		N4	PE12RN0		P8	V_{SS}	
M1	V_{SS}		N5	PE12RP0		P9	V_{DD}CORE	
M2	V_{SS}		N6	REFRES05		P10	V_{DD}CORE	
M3	V_{SS}		N7	V_{DD}PEA		P11	V_{SS}	
M4	V_{SS}		N8	V_{SS}		P12	V_{SS}	
M5	V_{SS}		N9	V_{DD}CORE		P13	V_{DD}CORE	
M6	V_{DD}PEA		N10	V_{DD}CORE		P14	V_{DD}CORE	
M7	V_{DD}PEA		N11	V_{SS}		P15	V_{SS}	
M8	V_{SS}		N12	V_{SS}		P16	V_{DD}PEA	
M9	V_{DD}CORE		N13	V_{DD}CORE		P17	V_{DD}PETA	
M10	V_{DD}CORE		N14	V_{DD}CORE		P18	PE01RP0	
M11	V_{DD}CORE		N15	V_{SS}		P19	PE01RN0	
M12	V_{DD}CORE		N16	V_{DD}PEA		P20	V_{SS}	
M13	V_{DD}CORE		N17	REFRES00		P21	PE01TN0	
M14	V_{DD}CORE		N18	PE01RP1		P22	PE01TP0	
M15	V_{SS}		N19	PE01RN1		R1	V_{SS}	
M16	V_{DD}PEA		N20	V_{SS}		R2	V_{SS}	
M17	V_{DD}PEA		N21	PE01TN1		R3	V_{SS}	
M18	V_{SS}		N22	PE01TP1		R4	V_{SS}	

Table 24 PES32NT24AG2 Signal Pin-Out (Part 4 of 7)

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Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
R5	V_{SS}		T9	V_{DD}PEA		U13	V_{DD}PETA	
R6	V_{DD}PETA		T10	V_{DD}PEA		U14	V_{DD}PETA	
R7	V_{DD}PEHA		T11	V_{DD}PEA		U15	V_{DD}PEHA	
R8	V_{SS}		T12	V_{DD}PEA		U16	V_{DD}PEHA	
R9	V_{DD}CORE		T13	V_{DD}PEA		U17	V_{SS}	
R10	V_{DD}CORE		T14	V_{DD}PEA		U18	PE00RP0	
R11	V_{SS}		T15	V_{SS}		U19	PE00RN0	
R12	V_{SS}		T16	V_{DD}PEHA		U20	V_{SS}	
R13	V_{DD}CORE		T17	V_{DD}PETA		U21	PE00TN0	
R14	V_{DD}CORE		T18	PE00RP1		U22	PE00TP0	
R15	V_{SS}		T19	PE00RN1		V1	V_{SS}	
R16	V_{DD}PEHA		T20	V_{SS}		V2	V_{SS}	
R17	V_{DD}PETA		T21	PE00TN1		V3	P12CLKP	
R18	V_{SS}		T22	PE00TP1		V4	V_{SS}	
R19	V_{SS}		U1	PE15TP0		V5	V_{SS}	
R20	V_{SS}		U2	PE15TN0		V6	PE16RP0	
R21	V_{SS}		U3	V_{SS}		V7	PE17RP0	
R22	V_{SS}		U4	PE15RN0		V8	V_{SS}	
T1	PE14TP0		U5	PE15RP0		V9	PE18RP0	
T2	PE14TN0		U6	V_{SS}		V10	PE19RP0	
T3	V_{SS}		U7	V_{DD}PEHA		V11	V_{SS}	
T4	PE14RN0		U8	V_{DD}PEHA		V12	V_{SS}	
T5	PE14RP0		U9	V_{DD}PETA		V13	PE20RP0	
T6	V_{DD}PETA		U10	V_{DD}PETA		V14	PE21RP0	
T7	V_{DD}PEHA		U11	V_{DD}PETA		V15	V_{SS}	
T8	V_{SS}		U12	V_{DD}PETA		V16	PE22RP0	

Table 24 PES32NT24AG2 Signal Pin-Out (Part 5 of 7)

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Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
V17	PE23RP0		W21	V_{DD}I/O		AA3	SWMODE1	
V18	V_{SS}		W22	V_{DD}I/O		AA4	RSTHALT	
V19	V_{SS}		Y1	STK0CFG0		AA5	PE16TN0	
V20	P00CLKN		Y2	STK3CFG0		AA6	PE17TN0	
V21	V_{SS}		Y3	SWMODE0		AA7	V_{SS}	
V22	V_{SS}		Y4	SWMODE2		AA8	PE18TN0	
W1	V_{DD}I/O		Y5	SWMODE3		AA9	PE19TN0	
W2	V_{DD}I/O		Y6	V_{SS}		AA10	V_{SS}	
W3	P12CLKN		Y7	V_{SS}		AA11	P16CLKN	
W4	V_{DD}I/O		Y8	NC		AA12	P20CLKN	
W5	V_{SS}		Y9	REFRES06		AA13	V_{SS}	
W6	PE16RN0		Y10	V_{SS}		AA14	PE20TN0	
W7	PE17RN0		Y11	GCLKP1		AA15	PE21TN0	
W8	V_{SS}		Y12	GCLKN1		AA16	V_{SS}	
W9	PE18RN0		Y13	V_{SS}		AA17	PE22TN0	
W10	PE19RN0		Y14	REFRES07		AA18	PE23TN0	
W11	V_{SS}		Y15	V_{SS}		AA19	GPIO__00	
W12	V_{SS}		Y16	V_{SS}		AA20	GPIO__02	
W13	PE20RN0		Y17	V_{SS}		AA21	GPIO__06	
W14	PE21RN0		Y18	GPIO__01		AA22	GPIO__07	
W15	V_{SS}		Y19	GPIO__03		AB1	STK1CFG0	
W16	PE22RN0		Y20	GPIO__04		AB2	GCLKFSEL	
W17	PE23RN0		Y21	GPIO__08		AB3	V_{SS}	
W18	V_{SS}		Y22	SSMBADDR1		AB4	V_{SS}	
W19	V_{DD}I/O		AA1	CLKMODE0		AB5	PE16TP0	
W20	P00CLKP		AA2	STK2CFG0		AB6	PE17TP0	

Table 24 PES32NT24AG2 Signal Pin-Out (Part 6 of 7)

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Pin	Function	Alt.	Pin	Function	Alt.	Pin	Function	Alt.
AB7	V_{SS}		AB13	V_{SS}		AB19	V_{SS}	
AB8	PE18TP0		AB14	PE20TP0		AB20	STK1CFG1	
AB9	PE19TP0		AB15	PE21TP0		AB21	STK0CFG1	
AB10	V_{SS}		AB16	V_{SS}		AB22	GPIO__05	
AB11	P16CLKP		AB17	PE22TP0				
AB12	P20CLKP		AB18	PE23TP0				

Table 24 PES32NT24AG2 Signal Pin-Out (Part 7 of 7)

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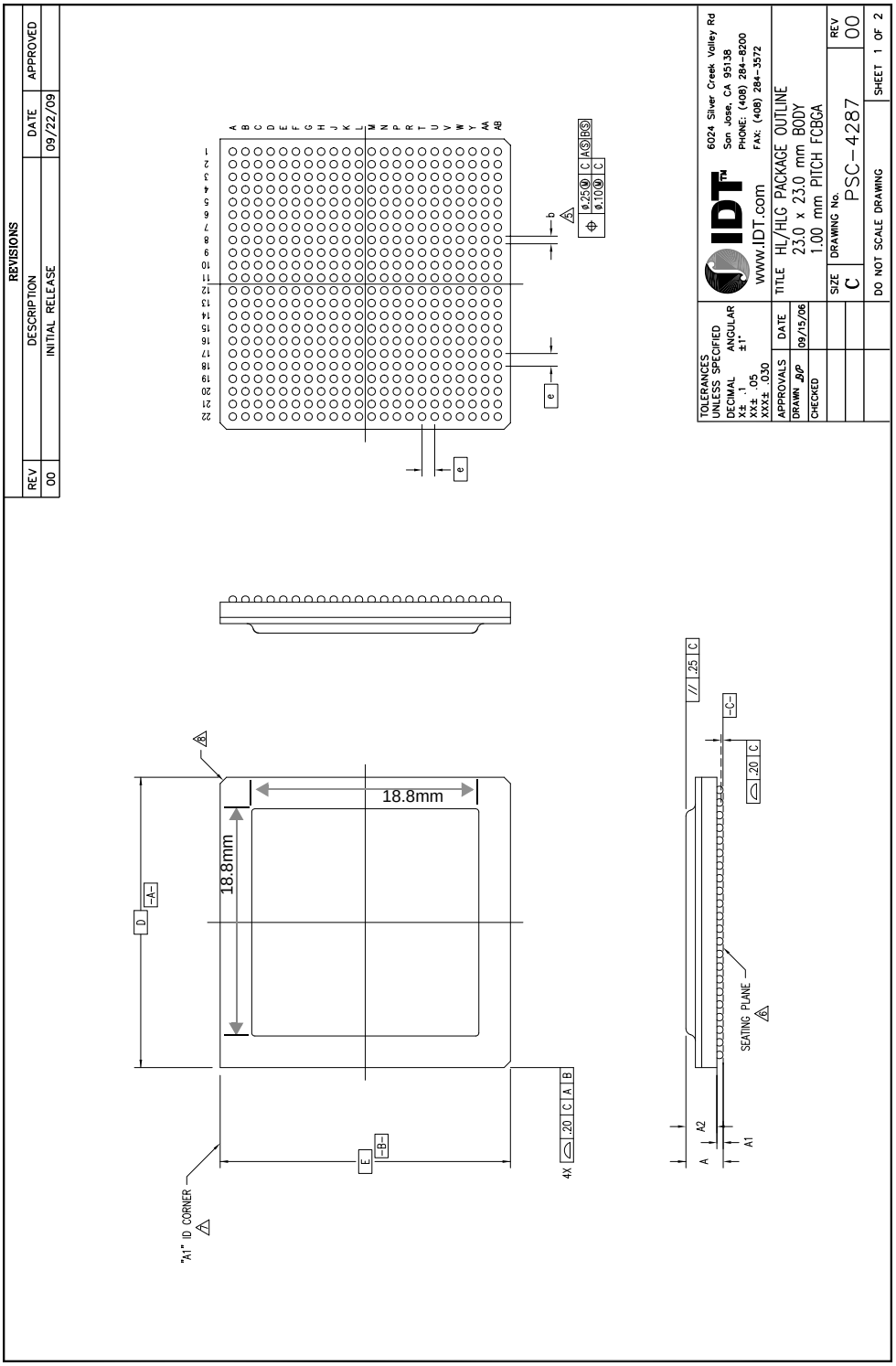
PES32NT24AG2 Package Drawing — 484-Pin HL/HLG484

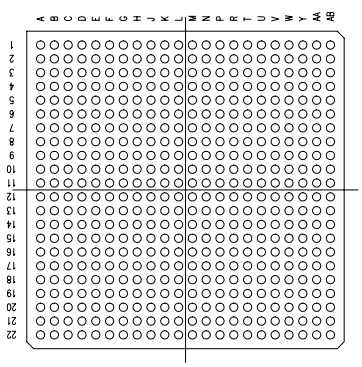


PES32NT24AG2 Package Drawing — Page Two

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	09/22/09	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE
4. "N" REPRESENTS THE BALLCOUNT NUMBER
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-
6. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
7. "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. ALL DIMENSIONS ARE IN MILLIMETERS



484 BALLS

SYMBOL	JEDEC VARIATION NONE MIN	NOM	MAX	NOTE
A	–	–	2.92	
A1	–	.50	–	
A2	1.96	–	2.32	
D	23.00 BSC			
E	23.00 BSC			
M	22			3
N	484			4
e	1.00 BSC			
b	.50	.64	.70	5
CENTER BALL MATRIX	N/A			

Note:
Nominal package height: 2.63mm
Minimum package height: 2.53mm.

TOLERANCES UNLESS SPECIFIED		
DECIMAL	ANGULAR	
X± .1	±1°	
XX± .05		
XXX± .030		

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APPROVALS	DATE
DRAWN JGP	09/22/09
CHECKED	

TITLE HL/HLG PACKAGE OUTLINE 23.0 x 23.0 mm BODY 1.00 mm PITCH FCBGA

SIZE C | DRAWING No. PSC-4287 | REV 00

DO NOT SCALE DRAWING | SHEET 2 OF 2

Revision History

October 27, 2010: Initial publication of final data sheet.

November 11, 2010: Added ZB silicon on Ordering page.

January 26, 2011: In Table 18, Power Consumption, revised IO (and Total) power numbers in Full Swing section and added Half Swing section. Adjusted P value in Table 19.

March 9, 2011: In Table 10, deleted “External pull-down” from the Notes column for JTAG_TRST_N.

March 28, 2011: In Tables 16 and 17, added V_{DD}PETA to footnote #1.

April 7, 2011: Added dimensions of raised portion of heat spreader in package drawing.

May 20, 2011: Removed ZA silicon and added ZC to Order page and codes.

November 7, 2011: Revised values in Table 18, Power Consumption, and updated power dissipation value in Table 19.

November 29, 2011: Added new Tables 22 and 23, SMBus Characterization and Timing.

March 14, 2012: In Table 3, revised description for GCLKN/P signals.

April 16, 2013: In Table 20, added 3.3V output voltage parameters under Other I/Os category.

May 16, 2013: Added Note after Table 11. In Table 20, added information in the Conditions column for the 3.3V parameters.

December 17, 2013: Added footnote 2 to Table 23.

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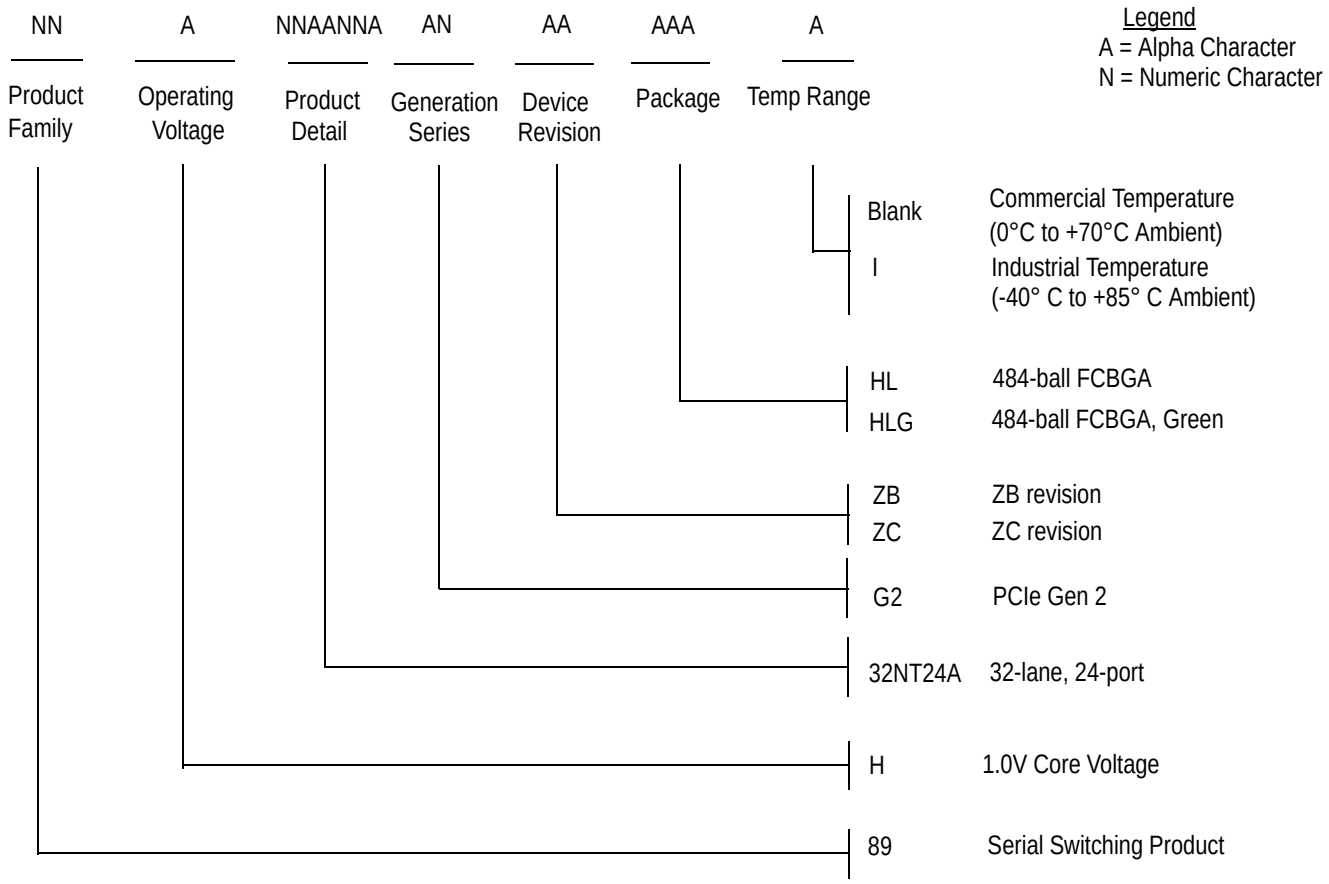
Ordering Information



Valid Combinations

89H32NT24AG2ZBHL	484-ball FCBGA package, Commercial Temp.	89H32NT24AG2ZCHL	484-ball FCBGA package, Commercial Temp.
89H32NT24AG2ZBHLG	484-ball Green FCBGA package, Commercial Temp.	89H32NT24AG2ZCHLG	484-ball Green FCBGA package, Commercial Temp.
89H32NT24AG2ZBHLI	484-ball FCBGA package, Industrial Temp.	89H32NT24AG2ZCHLI	484-ball FCBGA package, Industrial Temp.
89H32NT24AG2ZBHLGI	484-ball Green FCBGA package, Industrial Temp.	89H32NT24AG2ZCHLGI	484-ball Green FCBGA package, Industrial Temp.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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