



#### Description

The Atmel SAM4E series of Flash microcontrollers is based on the high-performance 32-bit ARM® Cortex®-M4 RISC processor and includes a floating point unit (FPU). It operates at a maximum speed of 120 MHz and features up to 1024 Kbytes of Flash, 2 Kbytes of cache memory and up to 128 Kbytes of SRAM.

The SAM4E offers a rich set of advanced connectivity peripherals including 10/100 Mbps Ethernet MAC supporting IEEE 1588 and dual CAN. With a single-precision FPU, advanced analog features, as well as a full set of timing and control functions, the SAM4E is the ideal solution for industrial automation, home and building control, machine-to-machine communications, automotive aftermarket and energy management applications.

The peripheral set includes a full-speed USB device port with embedded transceiver, a 10/100 Mbps Ethernet MAC supporting IEEE 1588, a high-speed MCI for SDIO/SD/MMC, an external bus interface featuring a static memory controller providing connection to SRAM, PSRAM, NOR Flash, LCD Module and NAND Flash, a parallel I/O capture mode for camera interface, hardware acceleration for AES256, two USARTs, two UARTs, two TWIs, three SPIs, as well as a 4-channel PWM, nine general-purpose 16-bit Timers (with stepper motor and quadrature decoder logic support), one RTC, two Analog Front End interfaces (16-bit ADC, DAC, MUX and PGA), one 12-bit DAC (2-ch) and an analog comparator.

## Features

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- Core
  - ARM® Cortex®-M4 with 2 Kbytes Cache running at up to 120 MHz<sup>(1)</sup>
  - Memory Protection Unit (MPU)
  - DSP Instruction
  - Floating Point Unit (FPU)
  - Thumb®-2 Instruction Set
- Memories
  - Up to 1024 Kbytes Embedded Flash
  - 128 Kbytes Embedded SRAM
  - 16 Kbytes ROM with Embedded Boot Loader Routines (UART) and IAP Routines
  - Static Memory Controller (SMC): SRAM, NOR, NAND Support.
  - NAND Flash Controller.
- System
  - Embedded Voltage Regulator for Single Supply Operation
  - Power-on-Reset (POR), Brown-out Detector (BOD) and Dual Watchdog for Safe Operation
  - Quartz or Ceramic Resonator Oscillators: 3 to 20 MHz Main Power with Failure Detection and Optional Low-power 32.768 kHz for RTC or Device Clock
  - RTC with Gregorian and Persian Calendar Mode, Waveform Generation in Low-power Modes
  - RTC Clock Calibration Circuitry for 32.768 kHz Crystal Frequency Compensation
  - High Precision 4/8/12 MHz Factory Trimmed Internal RC Oscillator with 4 MHz Default Frequency for Device Startup. In-application Trimming Access for Frequency Adjustment
  - Slow Clock Internal RC Oscillator as Permanent Low-power Mode Device Clock
  - One PLL up to 240 MHz for Device Clock and for USB
  - Temperature Sensor
  - Up to 2 Peripheral DMA Controller with up to 33 Channels (PDC)
  - One 4-channel DMA Controller
- Low-power Modes
  - Sleep and Backup Modes
  - Ultra Low-power RTC
- Peripherals
  - Two USARTs with USART1 (ISO7816, IrDA®, RS-485, SPI, Manchester and Modem Modes)
  - USB 2.0 Device: Full Speed (12 Mbits), 2668 byte FIFO, up to 8 Endpoints. On-chip Transceiver
  - Two 2-wire UARTs
  - Two Two-wire Interfaces (TWI)
  - High-speed Multimedia Card Interface (SDIO/SD Card/MMC)
  - One Master/Slave Serial Peripheral Interface (SPI) with Chip Select Signals
  - Three 3-Channel 32-bit Timer/Counter with Capture, Waveform, Compare and PWM Mode. Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor
  - 32-bit Real-time Timer and RTC with Calendar and Alarm Features
  - One Ethernet MAC (EMAC) 10/100 Mbps in MII mode only with dedicated DMA and Support for IEEE1588, Wake-on-LAN
  - Two CAN Controllers with eight Mailboxes
  - 4-channel 16-bit PWM with Complementary Output, Fault Input, 12-bit Dead Time Generator Counter for Motor Control

- Real-time Event Management
- Cryptography
  - AES 256-bit Key Algorithm compliant with FIPS Publication 197
- Analog
  - AFE (Analog Front End): 2x16-bit ADC, up to 24-channels, Differential Input Mode, Programmable Gain Stage, Auto Calibration and Automatic Offset Correction
  - One 2-channel 12-bit 1 Msps DAC
  - One Analog Comparator with Flexible Input Selection, Selectable Input Hysteresis
- I/O
  - Up to 117 I/O Lines with External Interrupt Capability (Edge or Level Sensitivity), Debouncing, Glitch Filtering and On-die Series Resistor Termination
  - Bidirectional Pad, Analog I/O, Programmable Pull-up/Pull-down
  - Five 32-bit Parallel Input/Output Controllers, Peripheral DMA Assisted Parallel Capture Mode
- Packages
  - 144-ball LFBGA, 10x10 mm, pitch 0.8 mm
  - 100-ball TFBGA, 9x9 mm, pitch 0.8 mm
  - 144-lead LQFP, 20x20 mm, pitch 0.5 mm
  - 100-lead LQFP, 14x14 mm, pitch 0.5 mm

Note: 1. 120 MHz: -40/+105°C, VDDCORE = 1.2V or using internal voltage regulator

# 1. Configuration Summary

The SAM4E series devices differ in memory size, package and features. [Table 1-1](#) summarizes the configurations of the device family.

**Table 1-1.** Configuration Summary

| Feature                        | SAM4E16E                                                    | SAM4E8E    | SAM4E16C                                                  | SAM4E8C    |
|--------------------------------|-------------------------------------------------------------|------------|-----------------------------------------------------------|------------|
| Flash                          | 1024 Kbytes                                                 | 512 Kbytes | 1024 Kbytes                                               | 512 Kbytes |
| SRAM                           | 128 Kbytes                                                  |            | 128 Kbytes                                                |            |
| CMCC                           | 2 Kbytes                                                    |            | 2 Kbytes                                                  |            |
| Package                        | LFBGA 144<br>LQFP 144                                       |            | TFBGA 100<br>LQFP 100                                     |            |
| Number of PIOs                 | 117                                                         |            | 79                                                        |            |
| External Bus Interface         | 8-bit Data, 4 Chip Selects, 24-bit Address                  |            | -                                                         |            |
| Analog Front End (AFE0 \ AFE1) | Up to 16 bits <sup>(1)</sup><br>16 ch.\ 8 ch <sup>(2)</sup> |            | Up to 16 bits <sup>(1)</sup><br>6 ch.\ 4ch <sup>(3)</sup> |            |
| EMAC                           | YES                                                         |            | YES                                                       |            |
| CAN                            | 2                                                           |            | 1                                                         |            |
| 12-bit DAC                     | 2 ch.                                                       |            | 2 ch.                                                     |            |
| Timer                          | 9 <sup>(4)</sup>                                            |            | 3 <sup>(5)</sup>                                          |            |
| PDC Channels                   | 24 +9                                                       |            | 21 +9                                                     |            |
| USART/ UART                    | 2/2 <sup>(6)</sup>                                          |            | 2/2 <sup>(6)</sup>                                        |            |
| USB                            | Full Speed                                                  |            | Full Speed                                                |            |
| HSMCI                          | 1 port<br>4 bits                                            |            | 1 port<br>4 bits                                          |            |
| TWI                            | 2                                                           |            | 2                                                         |            |

- Notes:
1. ADC is 12-bit, up to 16 bits with averaging.  
For details, please refer to the "Electrical Characteristics" section of this datasheet.
  2. AFE0 is 16 channels and AFE1 is 8 channels. The total number of AFE channels is 24.  
One channel is reserved for the internal temperature sensor.
  3. AFE0 is 6 channels and AFE1 is 4 channels. The total number of AFE channels is 10.  
One channel is reserved for the internal temperature sensor.
  4. 9 TC channels are accessible through PIO.
  5. 3 TC channels are accessible through PIO.
  6. Full Modem support on USART1.

## 2. Block Diagram

Figure 2-1. SAM4E 100-pin Block Diagram

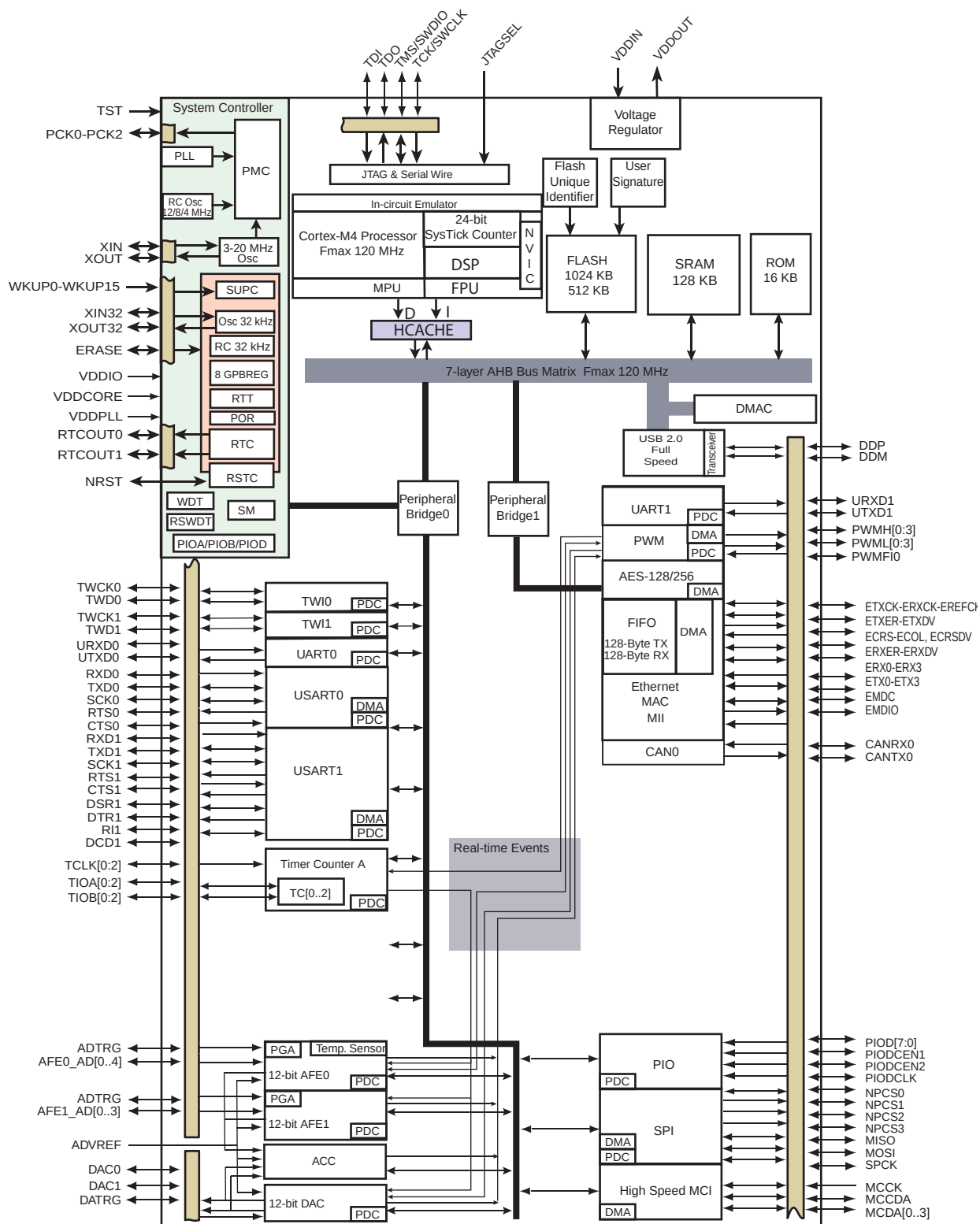
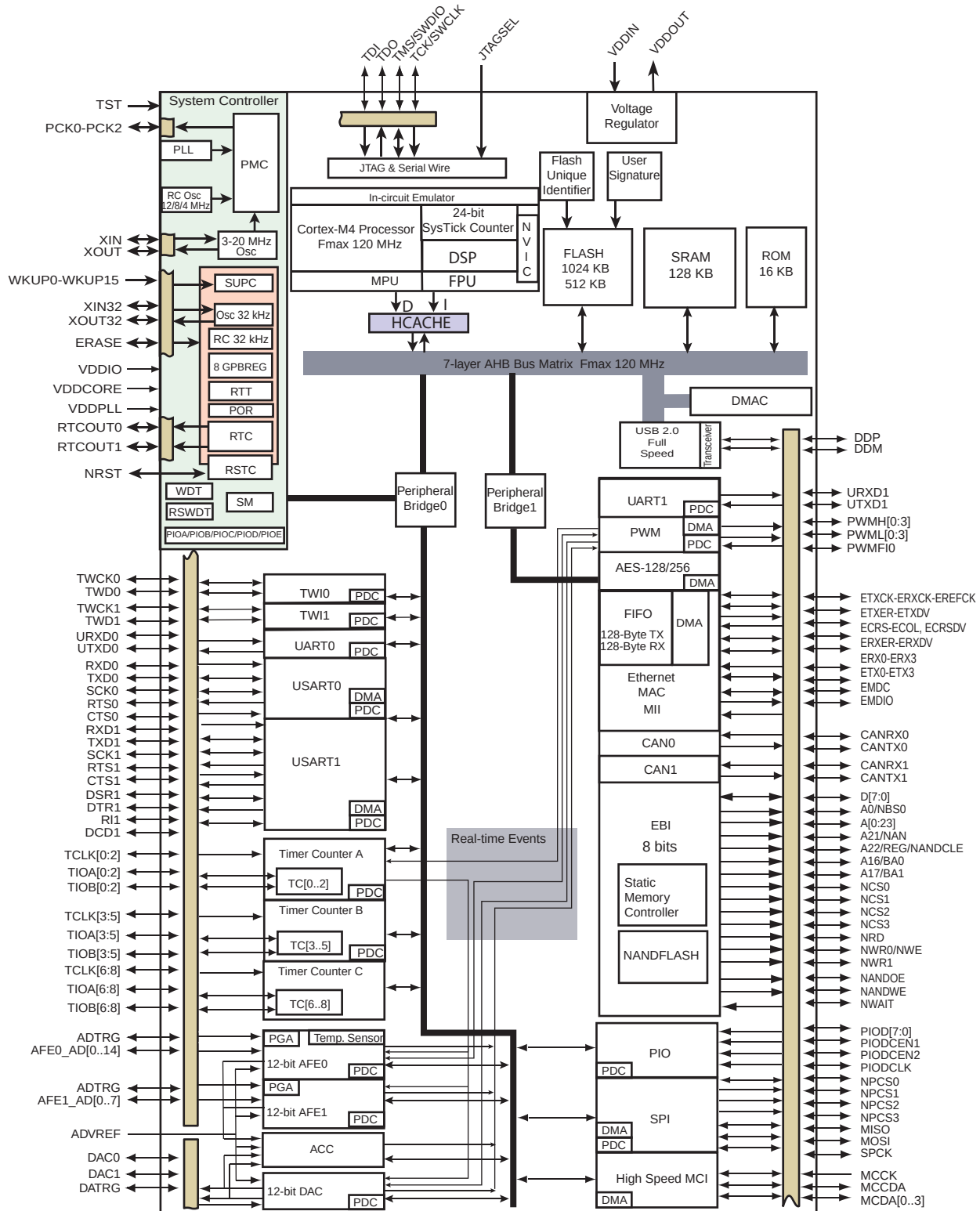


Figure 2-2. SAM4E 144-pin Block Diagram



### 3. Signal Description

Table 3-1 gives details on signal names classified by peripheral.

Table 3-1. Signal Description List

| Signal Name                          | Function                                                        | Type        | Active Level | Voltage Reference | Comments                                   |
|--------------------------------------|-----------------------------------------------------------------|-------------|--------------|-------------------|--------------------------------------------|
| Power Supplies                       |                                                                 |             |              |                   |                                            |
| VDDIO                                | Peripherals I/O Lines Power Supply                              | Power       |              |                   | 1.62V to 3.6V                              |
| VDDIN                                | Voltage Regulator Input, DAC and Analog Comparator Power Supply | Power       |              |                   | 1.62V to 3.6V <sup>(1)</sup>               |
| VDDOUT                               | Voltage Regulator Output                                        | Power       |              |                   | 1.2V Output                                |
| VDDPLL                               | Oscillator and PLL Power Supply                                 | Power       |              |                   | 1.08 V to 1.32V                            |
| VDDCORE                              | Power the core, the embedded memories and the peripherals       | Power       |              |                   | 1.08V to 1.32V                             |
| GND                                  | Ground                                                          | Ground      |              |                   |                                            |
| Clocks, Oscillators and PLLs         |                                                                 |             |              |                   |                                            |
| XIN                                  | Main Oscillator Input                                           | Input       |              | VDDIO             | Reset State:                               |
| XOUT                                 | Main Oscillator Output                                          | Output      |              |                   | - PIO Input                                |
| XIN32                                | Slow Clock Oscillator Input                                     | Input       |              |                   | - Internal Pull-up disabled                |
| XOUT32                               | Slow Clock Oscillator Output                                    | Output      |              |                   | - Schmitt Trigger enabled <sup>(2)</sup>   |
| PCK0 - PCK2                          | Programmable Clock Output                                       | Output      |              |                   | Reset State:                               |
|                                      |                                                                 |             |              |                   | - PIO Input                                |
|                                      |                                                                 |             |              |                   | - Internal Pull-up enabled                 |
|                                      |                                                                 |             |              |                   | - Schmitt Trigger enabled <sup>(2)</sup>   |
| Real-time Clock                      |                                                                 |             |              |                   |                                            |
| RTCOUT0                              | Programmable RTC waveform output                                | Output      |              | VDDIO             | Reset State:                               |
| RTCOUT1                              | Programmable RTC waveform output                                | Output      |              |                   | - PIO Input                                |
|                                      |                                                                 |             |              |                   | - Internal Pull-up enabled                 |
|                                      |                                                                 |             |              |                   | - Schmitt Trigger enabled <sup>(2)</sup>   |
| Serial Wire/JTAG Debug Port - SWJ-DP |                                                                 |             |              |                   |                                            |
| TCK/SWCLK                            | Test Clock/Serial Wire Clock                                    | Input       |              | VDDIO             | Reset State:                               |
| TDI                                  | Test Data In                                                    | Input       |              |                   | - SWJ-DP Mode                              |
| TDO/TRACESWO                         | Test Data Out / Trace Asynchronous Data Out                     | Output      |              |                   | - Internal Pull-up disabled <sup>(3)</sup> |
| TMS/SWDIO                            | Test Mode Select /Serial Wire Input/Output                      | Input / I/O |              |                   | - Schmitt Trigger enabled <sup>(2)</sup>   |
| JTAGSEL                              | JTAG Selection                                                  | Input       | High         |                   | Permanent Internal Pull-down               |
| Flash Memory                         |                                                                 |             |              |                   |                                            |
| ERASE                                | Flash and NVM Configuration Bits Erase Command                  | Input       | High         | VDDIO             | Reset State:                               |
|                                      |                                                                 |             |              |                   | - Erase Input                              |
|                                      |                                                                 |             |              |                   | - Internal Pull-down enabled               |
|                                      |                                                                 |             |              |                   | - Schmitt Trigger enabled <sup>(2)</sup>   |

Table 3-1. Signal Description List

| Signal Name                                                    | Function                          | Type   | Active Level | Voltage Reference | Comments                                 |
|----------------------------------------------------------------|-----------------------------------|--------|--------------|-------------------|------------------------------------------|
| Reset/Test                                                     |                                   |        |              |                   |                                          |
| NRST                                                           | Synchronous Microcontroller Reset | I/O    | Low          | VDDIO             | Permanent Internal Pull-up               |
| TST                                                            | Test Select                       | Input  |              |                   | Permanent Internal Pull-down             |
| Universal Asynchronous Receiver Transceiver - UARTx            |                                   |        |              |                   |                                          |
| URXDx                                                          | UART Receive Data                 | Input  |              |                   |                                          |
| UTXDx                                                          | UART Transmit Data                | Output |              |                   |                                          |
| PIO Controller - PIOA - PIOB - PIOC- PIOD - PIOE               |                                   |        |              |                   |                                          |
| PA0 - PA31                                                     | Parallel IO Controller A          | I/O    |              | VDDIO             | Reset State:                             |
| PB0 - PB14                                                     | Parallel IO Controller B          | I/O    |              |                   | - PIO or System IOs <sup>(4)</sup>       |
| PC0 - PC31                                                     | Parallel IO Controller C          | I/O    |              |                   | - Internal Pull-up enabled               |
| PD0 - PD31                                                     | Parallel IO Controller D          | I/O    |              |                   | - Schmitt Trigger enabled <sup>(2)</sup> |
| PE0 - PE5                                                      | Parallel IO Controller E          | I/O    |              |                   | Reset State:                             |
|                                                                |                                   |        |              |                   | - PIO or System IOs <sup>(4)</sup>       |
|                                                                |                                   |        |              |                   | - Internal Pull-up enabled               |
|                                                                |                                   |        |              |                   | - Schmitt Trigger enabled <sup>(2)</sup> |
| PIO Controller - Parallel Capture Mode                         |                                   |        |              |                   |                                          |
| PIODC0-PIODC7                                                  | Parallel Capture Mode Data        | Input  |              | VDDIO             |                                          |
| PIODCCLK                                                       | Parallel Capture Mode Clock       | Input  |              |                   |                                          |
| PIODCEN1-2                                                     | Parallel Capture Mode Enable      | Input  |              |                   |                                          |
| High Speed Multimedia Card Interface - HSMCI                   |                                   |        |              |                   |                                          |
| MCCK                                                           | Multimedia Card Clock             | I/O    |              |                   |                                          |
| MCCDA                                                          | Multimedia Card Slot A Command    | I/O    |              |                   |                                          |
| MCDA0 - MCDA3                                                  | Multimedia Card Slot A Data       | I/O    |              |                   |                                          |
| Universal Synchronous Asynchronous Receiver Transmitter USARTx |                                   |        |              |                   |                                          |
| SCKx                                                           | USARTx Serial Clock               | I/O    |              |                   |                                          |
| TXDx                                                           | USARTx Transmit Data              | I/O    |              |                   |                                          |
| RXDx                                                           | USARTx Receive Data               | Input  |              |                   |                                          |
| RTSx                                                           | USARTx Request To Send            | Output |              |                   |                                          |
| CTSx                                                           | USARTx Clear To Send              | Input  |              |                   |                                          |
| DTR1                                                           | USART1 Data Terminal Ready        | I/O    |              |                   |                                          |
| DSR1                                                           | USART1 Data Set Ready             | Input  |              |                   |                                          |
| DCD1                                                           | USART1 Data Carrier Detect        | Output |              |                   |                                          |
| RI1                                                            | USART1 Ring Indicator             | Input  |              |                   |                                          |
| Timer/Counter - TC                                             |                                   |        |              |                   |                                          |
| TCLKx                                                          | TC Channel x External Clock Input | Input  |              |                   |                                          |
| TIOAx                                                          | TC Channel x I/O Line A           | I/O    |              |                   |                                          |
| TIOBx                                                          | TC Channel x I/O Line B           | I/O    |              |                   |                                          |



Table 3-1. Signal Description List

| Signal Name                              | Function                                 | Type            | Active Level | Voltage Reference | Comments |
|------------------------------------------|------------------------------------------|-----------------|--------------|-------------------|----------|
| Serial Peripheral Interface - SPI        |                                          |                 |              |                   |          |
| MISO                                     | Master In Slave Out                      | I/O             |              |                   |          |
| MOSI                                     | Master Out Slave In                      | I/O             |              |                   |          |
| SPCK                                     | SPI Serial Clock                         | I/O             |              |                   |          |
| SPI_NPCS0                                | SPI Peripheral Chip Select 0             | I/O             | Low          |                   |          |
| SPI_NPCS1 - SPI_NPCS3                    | SPI Peripheral Chip Select               | Output          | Low          |                   |          |
| Two-Wire Interface - TWIx                |                                          |                 |              |                   |          |
| TWDx                                     | TWlx Two-wire Serial Data                | I/O             |              |                   |          |
| TWCKx                                    | TWlx Two-wire Serial Clock               | I/O             |              |                   |          |
| Analog                                   |                                          |                 |              |                   |          |
| ADVREF                                   | ADC, DAC and Analog Comparator Reference | Analog          |              |                   |          |
| 12-bit Analog-Front-End - AFEx           |                                          |                 |              |                   |          |
| AFE0_AD0-AFE0_AD14                       | Analog Inputs                            | Analog, Digital |              |                   |          |
| AFE1_AD0-AFE1_AD7                        | Analog Inputs                            | Analog, Digital |              |                   |          |
| ADTRG                                    | Trigger                                  | Input           |              | VDDIO             |          |
| 12-bit Digital-to-Analog Converter - DAC |                                          |                 |              |                   |          |
| DAC0 - DAC1                              | Analog output                            | Analog, Digital |              |                   |          |
| DACTRG                                   | DAC Trigger                              | Input           |              | VDDIO             |          |
| Fast Flash Programming Interface - FFPI  |                                          |                 |              |                   |          |
| PGMEN0-PGMEN2                            | Programming Enabling                     | Input           |              | VDDIO             |          |
| PGMM0-PGMM3                              | Programming Mode                         | Input           |              | VDDIO             |          |
| PGMD0-PGMD15                             | Programming Data                         | I/O             |              |                   |          |
| PGMRDY                                   | Programming Ready                        | Output          | High         |                   |          |
| PGMNVALID                                | Data Direction                           | Output          | Low          |                   |          |
| PGMNOE                                   | Programming Read                         | Input           | Low          |                   |          |
| PGMCK                                    | Programming Clock                        | Input           |              |                   |          |
| PGMNCMD                                  | Programming Command                      | Input           | Low          |                   |          |
| External Bus Interface                   |                                          |                 |              |                   |          |
| D0 - D7                                  | Data Bus                                 | I/O             |              |                   |          |
| A0 - A23                                 | Address Bus                              | Output          |              |                   |          |
| NWAIT                                    | External Wait Signal                     | Input           | Low          |                   |          |
| Static Memory Controller - SMC           |                                          |                 |              |                   |          |
| NCS0 - NCS3                              | Chip Select Lines                        | Output          | Low          |                   |          |
| NRD                                      | Read Signal                              | Output          | Low          |                   |          |

**Table 3-1. Signal Description List**

| Signal Name                                    | Function                               | Type               | Active Level | Voltage Reference | Comments                                                               |
|------------------------------------------------|----------------------------------------|--------------------|--------------|-------------------|------------------------------------------------------------------------|
| NWE                                            | Write Enable                           | Output             | Low          |                   |                                                                        |
| <b>NAND Flash Logic</b>                        |                                        |                    |              |                   |                                                                        |
| NANDOE                                         | NAND Flash Output Enable               | Output             | Low          |                   |                                                                        |
| NANDWE                                         | NAND Flash Write Enable                | Output             | Low          |                   |                                                                        |
| <b>Pulse Width Modulation Controller- PPMC</b> |                                        |                    |              |                   |                                                                        |
| PWMH                                           | PWM Waveform Output High for channel x | Output             |              |                   |                                                                        |
| PWML                                           | PWM Waveform Output Low for channel x  | Output             |              |                   | Only output in complementary mode when dead time insertion is enabled. |
| PWMFIO                                         | PWM Fault Input                        | Input              |              |                   |                                                                        |
| <b>Ethernet MAC 10/100 -EMAC</b>               |                                        |                    |              |                   |                                                                        |
| GREFCK                                         | Reference Clock                        | Input              |              |                   |                                                                        |
| GTXCK                                          | Transmit Clock                         | Input              |              |                   |                                                                        |
| GRXCK                                          | Receive Clock                          | Input              |              |                   |                                                                        |
| GTXEN                                          | Transmit Enable                        | Output             |              |                   |                                                                        |
| GTX0 - GTX3                                    | Transmit Data                          | Output             |              |                   |                                                                        |
| GTXER                                          | Transmit Coding Error                  | Output             |              |                   |                                                                        |
| GRXDV                                          | Receive Data Valid                     | Input              |              |                   |                                                                        |
| GRX0 - GRX3                                    | Receive Data                           | Input              |              |                   |                                                                        |
| GRXER                                          | Receive Error                          | Input              |              |                   |                                                                        |
| GCRS                                           | Carrier Sense                          | Input              |              |                   |                                                                        |
| GCOL                                           | Collision Detected                     | Input              |              |                   |                                                                        |
| GMDC                                           | Management Data Clock                  | Output             |              |                   |                                                                        |
| GMDIO                                          | Management Data Input/Output           | I/O                |              |                   |                                                                        |
| <b>Controller Area Network-CAN (x=[0:1])</b>   |                                        |                    |              |                   |                                                                        |
| CANRXx                                         | CAN Receive                            | Input              |              |                   |                                                                        |
| CANTXx                                         | CAN Transmit                           | Output             |              |                   |                                                                        |
| <b>USB Full Speed Device</b>                   |                                        |                    |              |                   |                                                                        |
| DDM                                            | DDM USB Full Speed Data -              | Analog,<br>Digital |              |                   | Reset State:<br>- USB Mode<br>- Internal Pull-down <sup>(1)</sup>      |
| DDP                                            | DDP USB Full Speed Data +              |                    |              |                   | Reset State:<br>- USB Mode<br>- Internal Pull-down <sup>(1)</sup>      |

- Notes:
1. See "Typical Powering Schematics" section of this datasheet for restrictions on voltage range of Analog Cells.
  2. Schmitt Triggers can be disabled through PIO registers.
  3. TDO pin is set in input mode when the Cortex-M4 Core is not in debug mode. Thus the internal pull-up corresponding to this PIO line must be enabled to avoid current consumption due to floating input.
  4. Some PIO lines are shared with System I/Os.

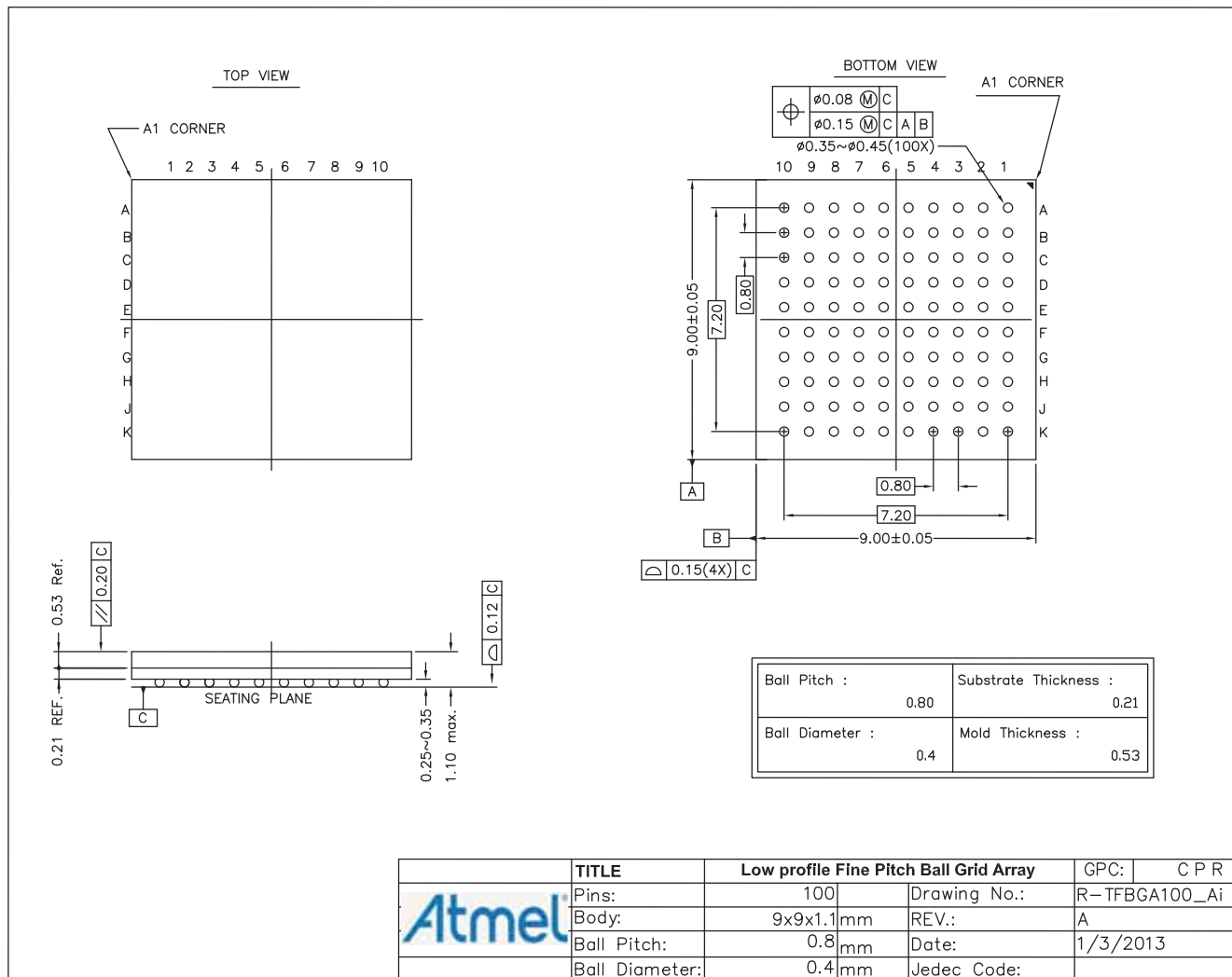
## 4. Package and Pinout

The SAM4E is available in TFBGA100, LFBGA144, LQFP100, and LQFP144 and packages. These packages respects the recommendations of the NEMI User Group.

### 4.1 100-ball TFBGA Package and Pinout

#### 4.1.1 100-ball TFBGA Package Drawing

The 100-ball TFBGA package has a 0.8 mm ball pitch and respects Green Standards.



**Table 4-1. Device and TFBGA Package Maximum Weight (Preliminary)**

|       |     |    |
|-------|-----|----|
| SAM4E | 150 | mg |
|-------|-----|----|

**Table 4-2. TFBGA Package Reference**

|                         |               |
|-------------------------|---------------|
| JEDEC Drawing Reference | MO-275-DDAC-2 |
| JESD97 Classification   | e8            |

**Table 4-3. TFBGA Package Characteristics**

|                            |   |
|----------------------------|---|
| Moisture Sensitivity Level | 3 |
|----------------------------|---|

#### 4.1.2 100-ball TFBGA Pinout

Table 4-4. SAM4E 100-ball TFBGA Pinout

|     |           |     |             |     |               |     |             |
|-----|-----------|-----|-------------|-----|---------------|-----|-------------|
| A1  | PB9       | C6  | PD29        | F1  | PA19/PGMD11   | H6  | PA14/PGMD6  |
| A2  | PB8       | C7  | PA30        | F2  | PA20/PGMD12   | H7  | PA25        |
| A3  | PB14      | C8  | PB5         | F3  | PD23          | H8  | PA27        |
| A4  | PB10      | C9  | PD10        | F4  | GNDIO         | H9  | PA5/PGMN1   |
| A5  | PD4       | C10 | PA1/PGMRDY  | F5  | GNDIO         | H10 | PA4/PGMN0   |
| A6  | PD7       | D1  | ADVREF      | F6  | GNDIO         | J1  | PA21/PGMD13 |
| A7  | PA31      | D2  | PD1         | F7  | TST           | J2  | PA7/PGMN3   |
| A8  | PA6/PGMN2 | D3  | GNDIO       | F8  | PB12          | J3  | PA22/PGMD14 |
| A9  | PA28      | D4  | GNDIO       | F9  | PA3/PGMNVALID | J4  | PD22        |
| A10 | JTAGSEL   | D5  | PD5         | F10 | PD14          | J5  | PA16/PGMD8  |
| B1  | PD31      | D6  | VDDCORE     | G1  | PA17/PGMD9    | J6  | PA15/PGMD7  |
| B2  | PB13      | D7  | VDDCORE     | G2  | PA18/PGMD10   | J7  | PD28        |
| B3  | VDDPLL    | D8  | PA0/PGMNCMD | G3  | PD26          | J8  | PA11/PGMD3  |
| B4  | PB11      | D9  | PD11        | G4  | PD24          | J9  | PA9/PGMD1   |
| B5  | PD3       | D10 | PA2/PGMNOE  | G5  | PA13/PGMD5    | J10 | PD17        |
| B6  | PD6       | E1  | PB0         | G6  | VDDCORE       | K1  | PD30        |
| B7  | PD8       | E2  | PB1         | G7  | VDDIO         | K2  | PA8/PGMD0   |
| B8  | PD9       | E3  | PD2         | G8  | PB6           | K3  | PD20        |
| B9  | PB4       | E4  | GNDANA      | G9  | PD16          | K4  | PD19        |
| B10 | PD15      | E5  | VDDIO       | G10 | NRST          | K5  | PA23/PGMD15 |
| C1  | PD0       | E6  | VDDIO       | H1  | PB2           | K6  | PD18        |
| C2  | VDDIN     | E7  | GNDIO       | H2  | PB3           | K7  | PA24        |
| C3  | VDDOUT    | E8  | PD13        | H3  | PD25          | K8  | PA26        |
| C4  | GNDPLL    | E9  | PB7         | H4  | PD27          | K9  | PA10/PGMD2  |
| C5  | PA29      | E10 | PD12        | H5  | PD21          | K10 | PA12/PGMD4  |

## 4.2 144-ball LFBGA Package and Pinout

### 4.2.1 144-ball LFBGA Package Outline

The 144-ball LFBGA package has a 0.8 mm ball pitch and respects Green Standards.

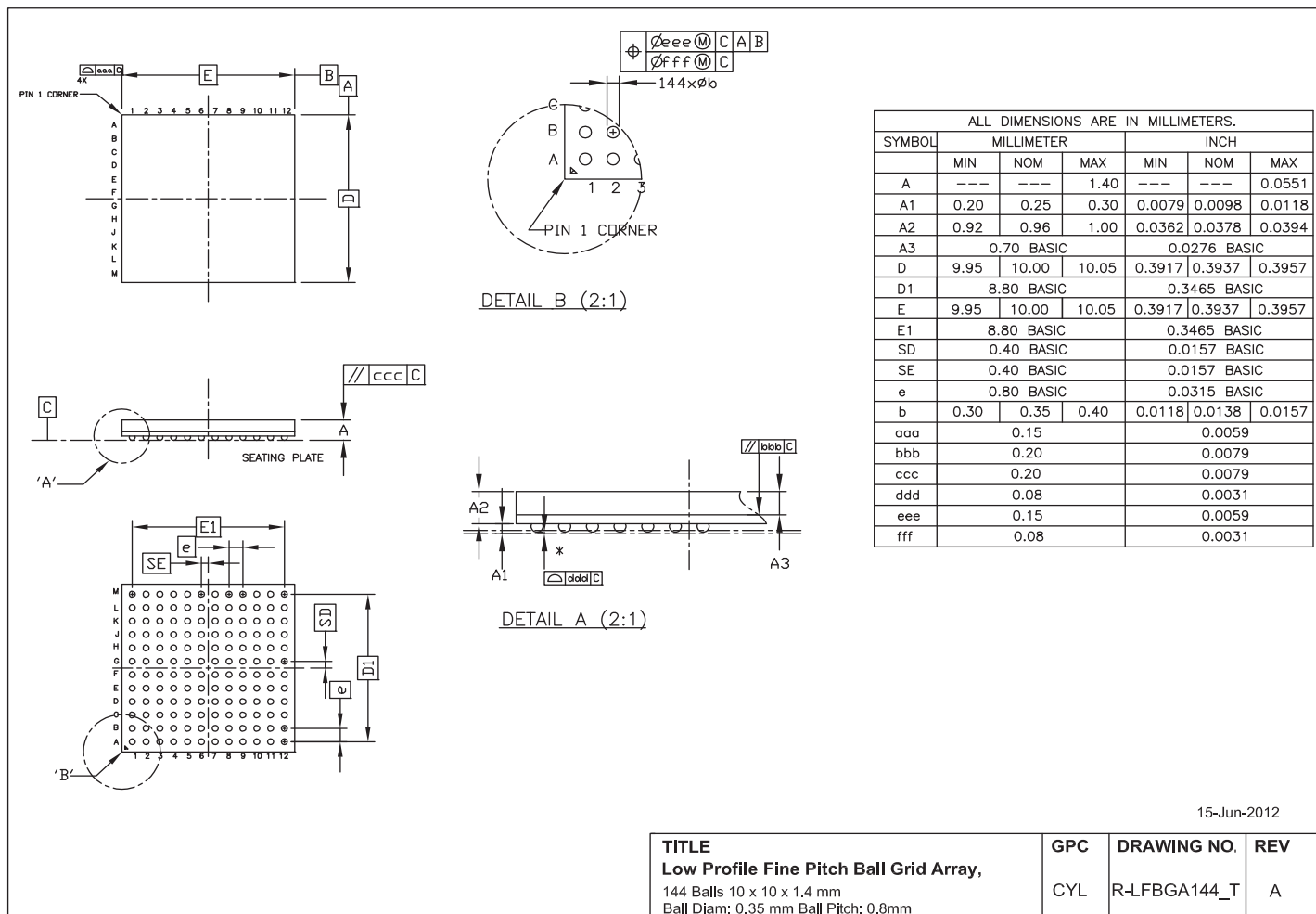


Table 4-5. Device and LFBGA Package Maximum Weight (Preliminary)

|       |     |    |
|-------|-----|----|
| SAM4E | 200 | mg |
|-------|-----|----|

Table 4-6. LFBGA Package Reference

|                         |               |
|-------------------------|---------------|
| JEDEC Drawing Reference | MS-275-EEAD-1 |
| JESD97 Classification   | e8            |

Table 4-7. LFBGA Package Characteristics

|                            |   |
|----------------------------|---|
| Moisture Sensitivity Level | 3 |
|----------------------------|---|

## 4.2.2 144-ball LFBGA Pinout

Table 4-8. SAM4E 144-ball LFBGA Pinout

|     |             |     |               |     |             |     |             |
|-----|-------------|-----|---------------|-----|-------------|-----|-------------|
| A1  | PE1         | D1  | ADVREF        | G1  | PC15        | K1  | PE4         |
| A2  | PB9         | D2  | GNDANA        | G2  | PC13        | K2  | PA21/PGMD13 |
| A3  | PB8         | D3  | PD31          | G3  | PB1         | K3  | PA22/PGMD14 |
| A4  | PB11        | D4  | PD0           | G4  | GNDIO       | K4  | PC2         |
| A5  | PD2         | D5  | GNDPLL        | G5  | GNDIO       | K5  | PA16/PGMD8  |
| A6  | PA29        | D6  | PD4           | G6  | GNDIO6      | K6  | PA14/PGMD6  |
| A7  | PC21        | D7  | PD5           | G7  | GNDIO6      | K7  | PC6         |
| A8  | PD6         | D8  | PC19          | G8  | VDDIO       | K8  | PA25        |
| A9  | PC20        | D9  | PD9           | G9  | PD13        | K9  | PD20        |
| A10 | PA30        | D10 | PD29          | G10 | PD12        | K10 | PD28        |
| A11 | PD15        | D11 | PC16          | G11 | PC9         | K11 | PD16        |
| A12 | PB4         | D12 | PA1/PGMRDY    | G12 | PB12        | K12 | PA4/PGMN0   |
| B1  | PE2         | E1  | PC31          | H1  | PA19/PGMD11 | L1  | PE5         |
| B2  | PB13        | E2  | PC27          | H2  | PA18/PGMD10 | L2  | PA7/PGMN3   |
| B3  | VDDPLL      | E3  | PE3           | H3  | PA20/PGMD12 | L3  | PC3         |
| B4  | PB10        | E4  | PC0           | H4  | PB0         | L4  | PA23/PGMD15 |
| B5  | PD1         | E5  | GNDIO         | H5  | VDDIO       | L5  | PA15/PGMD7  |
| B6  | PC24        | E6  | GNDIO         | H6  | VDDIO       | L6  | PD26        |
| B7  | PD3         | E7  | VDDIO         | H7  | VDDIO       | L7  | PA24        |
| B8  | PD7         | E8  | VDDIO         | H8  | VDDIO       | L8  | PC5         |
| B9  | PA6/PGMN2   | E9  | PD8           | H9  | PD21        | L9  | PA10/PGMD2  |
| B10 | PC18        | E10 | PC14          | H10 | PD14        | L10 | PA12/PGMD4  |
| B11 | JTAGSEL     | E11 | PD11          | H11 | TEST        | L11 | PD17        |
| B12 | PC17        | E12 | PA2/PGMNOE    | H12 | NRST        | L12 | PC28        |
| C1  | VDDIN       | F1  | PC30          | J1  | PA17/PGMD9  | M1  | PD30        |
| C2  | PE0         | F2  | PC26          | J2  | PB2         | M1  | PA8/PGMD0   |
| C3  | VDDOUT      | F3  | PC29          | J3  | PB3         | M3  | PA13/PGMD5  |
| C4  | PB14        | F4  | PC12          | J4  | PC1         | M4  | PC7         |
| C5  | PC25        | F5  | GNDIO         | J5  | PC4         | M5  | PD25        |
| C6  | PC23        | F6  | GNDIO         | J6  | PD27        | M6  | PD24        |
| C7  | PC22        | F7  | GNDIO         | J7  | VDDIO       | M7  | PD23        |
| C8  | PA31        | F8  | VDDIO         | J8  | PA26        | M8  | PD22        |
| C9  | PA28        | F9  | PB7           | J9  | PA11/PGMD3  | M9  | PD19        |
| C10 | PB5         | F10 | PC10          | J10 | PA27        | M10 | PD18        |
| C11 | PA0/PGMNCMD | F11 | PC11          | J11 | PB6         | M11 | PA5/PGMN1   |
| C12 | PD10        | F12 | PA3/PGMNVALID | J12 | PC8         | M12 | PA9/PGMD1   |

4.3 100-lead LQFP Package and Pinout

4.3.1 100-lead LQFP Package Outline

The 100-lead LQFP package has a 0.5 mm ball pitch and respects Green Standards.

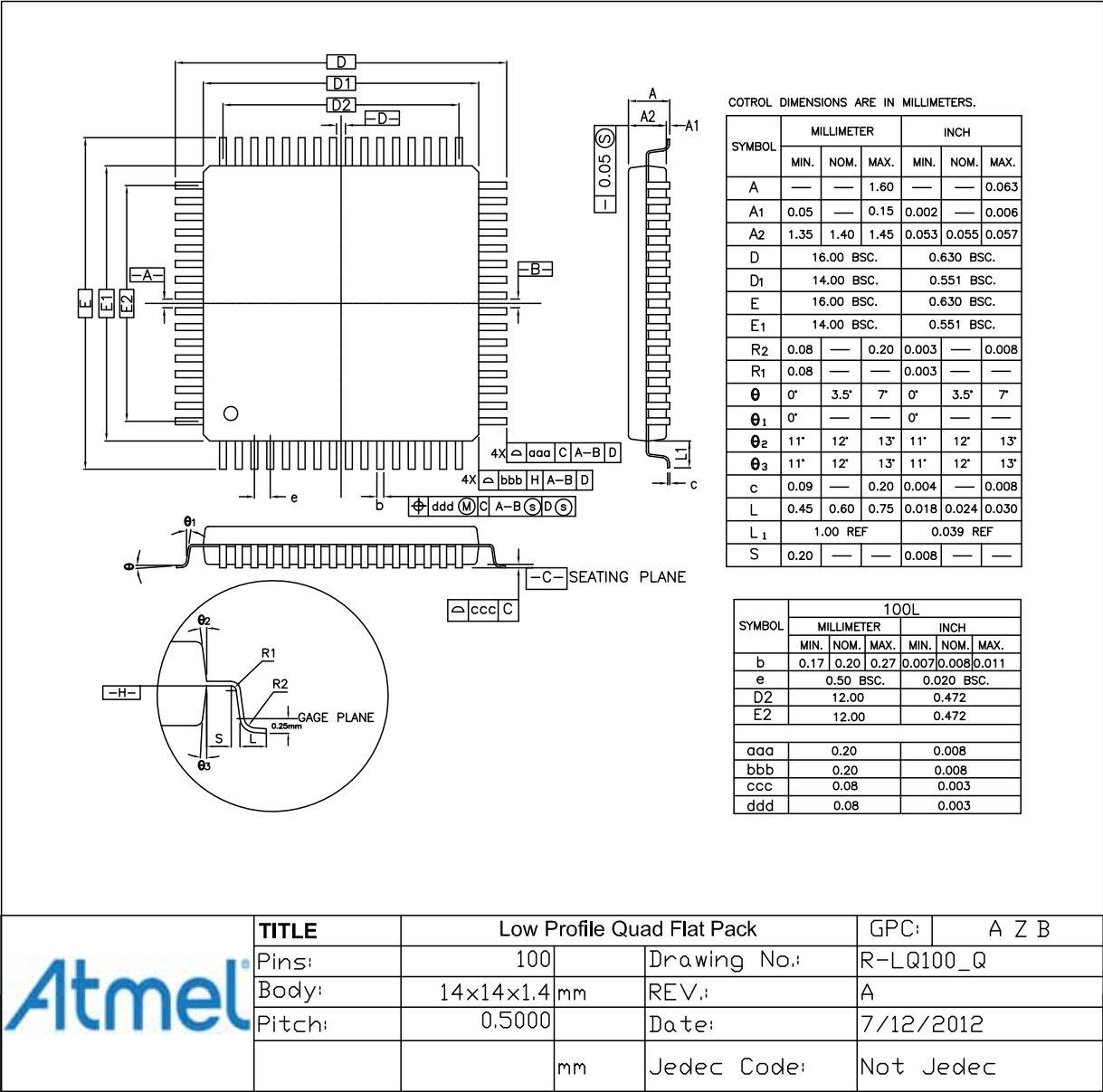


Table 4-9. Device and LQFP Package Maximum Weight (Preliminary)

|       |     |    |
|-------|-----|----|
| SAM4E | 740 | mg |
|-------|-----|----|

Table 4-10. LQFP Package Reference

|                         |        |
|-------------------------|--------|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification   | e3     |

Table 4-11. LQFP Package Characteristics

|                            |   |
|----------------------------|---|
| Moisture Sensitivity Level | 3 |
|----------------------------|---|

### 4.3.2 100-lead LQFP Pinout

Table 4-12. SAM4E 100-lead LQFP Pinout

|    |             |    |             |    |               |     |           |
|----|-------------|----|-------------|----|---------------|-----|-----------|
| 1  | PD0         | 26 | PA22/PGMD14 | 51 | PD28          | 76  | PD29      |
| 2  | PD31        | 27 | PA13/PGMD5  | 52 | PA5/PGMN1     | 77  | PB5       |
| 3  | GND         | 28 | VDDIO       | 53 | PD17          | 78  | PD9       |
| 4  | VDDOUT      | 29 | GND         | 54 | PA9/PGMD1     | 79  | PA28      |
| 5  | VDDIN       | 30 | PA16/PGMD8  | 55 | PA4/PGMN0     | 80  | PD8       |
| 6  | GND         | 31 | PA23/PGMD15 | 56 | PD16          | 81  | PA6/PGMN2 |
| 7  | GND         | 32 | PD27        | 57 | PB6           | 82  | PA30      |
| 8  | GND         | 33 | PA15/PGMD7  | 58 | NRST          | 83  | PA31      |
| 9  | ADVREF      | 34 | PA14/PGMD6  | 59 | PD14          | 84  | PD7       |
| 10 | GND         | 35 | PD25        | 60 | TST           | 85  | PD6       |
| 11 | PB1         | 36 | PD26        | 61 | PB12          | 86  | VDDCORE   |
| 12 | PB0         | 37 | PD24        | 62 | PD13          | 87  | PD5       |
| 13 | PA20/PGMD12 | 38 | PA24        | 63 | PB7           | 88  | PD4       |
| 14 | PA19/PGMD11 | 39 | PD23        | 64 | PA3/PGMNVALID | 89  | PD3       |
| 15 | PA18/PGMD10 | 40 | PA25        | 65 | PD12          | 90  | PA29      |
| 16 | PA17/PGMD9  | 41 | PD22        | 66 | PA2/PGMNNOE   | 91  | PD2       |
| 17 | PB2         | 42 | PA26        | 67 | GND           | 92  | PD1       |
| 18 | VDDCORE     | 43 | PD21        | 68 | VDDIO         | 93  | VDDIO     |
| 19 | VDDIO       | 44 | PA11/PGMD3  | 69 | PD11          | 94  | PB10      |
| 20 | PB3         | 45 | PD20        | 70 | PA1/PGMRDY    | 95  | PB11      |
| 21 | PA21/PGMD13 | 46 | PA10/PGMD2  | 71 | PD10          | 96  | VDDPLL    |
| 22 | VDDCORE     | 47 | PD19        | 72 | PA0           | 97  | PB14      |
| 23 | PD30        | 48 | PA12/PGMD4  | 73 | JTAGSEL       | 98  | PB8       |
| 24 | PA7/PGMN3   | 49 | PD18        | 74 | PB4           | 99  | PB9       |
| 25 | PA8/PGMD0   | 50 | PA27        | 75 | PD15          | 100 | PB13      |



## 4.4 144-lead LQFP Package and Pinout

### 4.4.1 144-lead LQFP Package Outline

The 144-lead LQFP package has a 0.5 mm ball pitch and respects Green Standards.

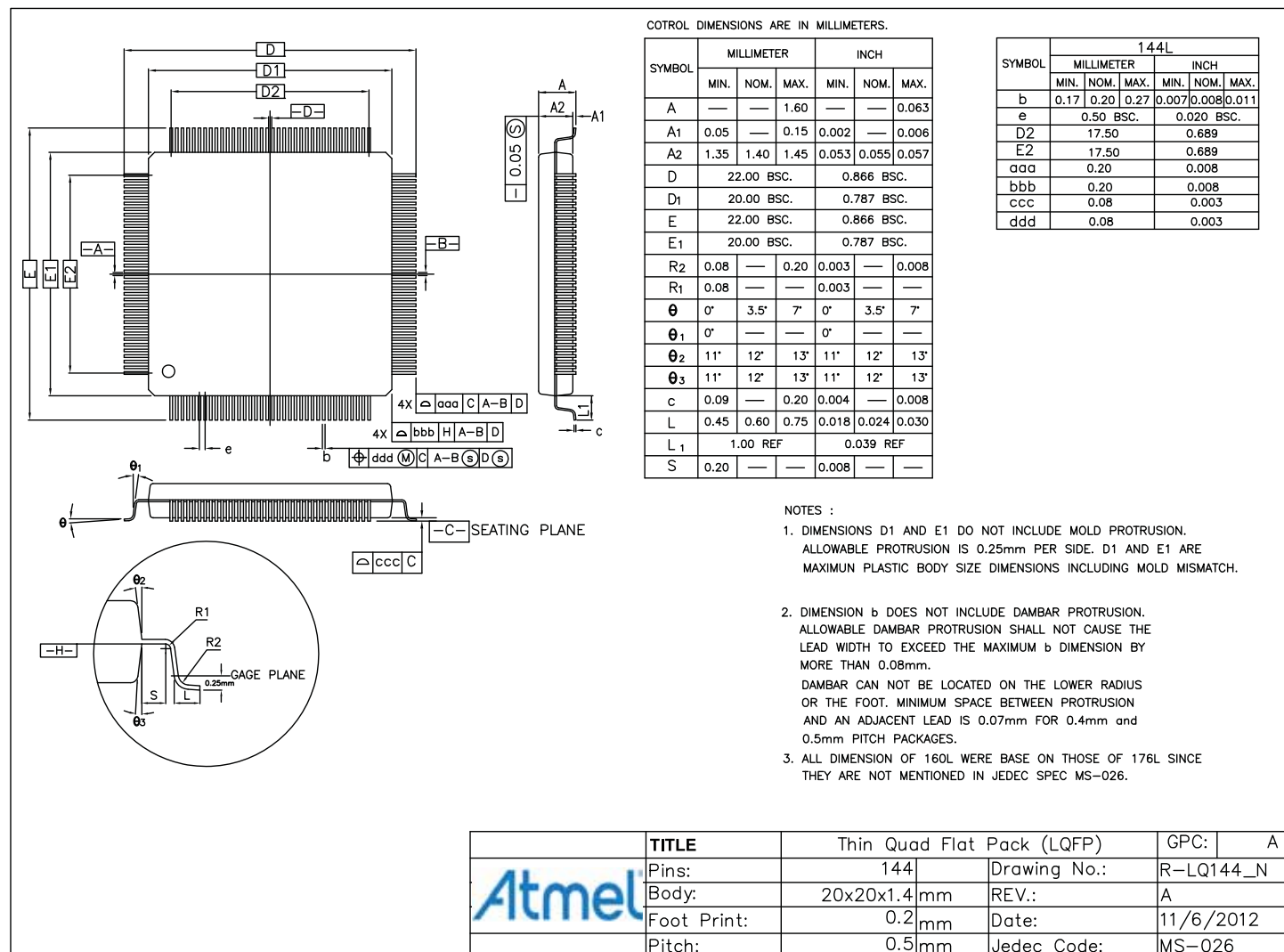


Table 4-13. Device and LQFP Package Maximum Weight (Preliminary)

|       |     |    |
|-------|-----|----|
| SAM4E | 900 | mg |
|-------|-----|----|

Table 4-14. LQFP Package Reference

|                         |          |
|-------------------------|----------|
| JEDEC Drawing Reference | MS-026-C |
| JESD97 Classification   | e3       |

Table 4-15. LQFP Package Characteristics

|                            |   |
|----------------------------|---|
| Moisture Sensitivity Level | 3 |
|----------------------------|---|

## 4.4.2 144-lead LQFP Pinout

Table 4-16. SAM4E 144-lead LQFP Pinout

|    |             |    |             |     |           |     |           |
|----|-------------|----|-------------|-----|-----------|-----|-----------|
| 1  | PD0         | 37 | PA22/PGMD14 | 73  | PA5/PGMN1 | 109 | PB5       |
| 2  | PD31        | 38 | PC1         | 74  | PD17      | 110 | PD9       |
| 3  | VDDOUT      | 39 | PC2         | 75  | PA9/PGMD1 | 111 | PC18      |
| 4  | PE0         | 40 | PC3         | 76  | PC28      | 112 | PA28      |
| 5  | VDDIN       | 41 | PC4         | 77  | PA4/PGMN0 | 113 | PD8       |
| 6  | PE1         | 42 | PA13/PGMD5  | 78  | PD16      | 114 | PA6/PGMN2 |
| 7  | PE2         | 43 | VDDIO       | 79  | PB6       | 115 | GND       |
| 8  | GND         | 44 | GND         | 80  | VDDIO     | 116 | PA30      |
| 9  | ADVREFP     | 45 | PA16/PGMD8  | 81  | VDDCORE   | 117 | PC19      |
| 10 | PE3         | 46 | PA23/PGMD15 | 82  | PC8       | 118 | PA31      |
| 11 | PC0         | 47 | PD27        | 83  | NRST      | 119 | PD7       |
| 12 | PC27        | 48 | PC7         | 84  | PD14      | 120 | PC20      |
| 13 | PC26        | 49 | PA15/PGMD7  | 85  | TEST      | 121 | PD6       |
| 14 | PC31        | 50 | VDDCORE     | 86  | PC9       | 122 | PC21      |
| 15 | PC30        | 51 | PA14/PGMD6  | 87  | PB12      | 123 | VDDCORE   |
| 16 | PC29        | 52 | PD25        | 88  | PD13      | 124 | PC22      |
| 17 | PC12        | 53 | PD26        | 89  | PB7       | 125 | PD5       |
| 18 | PC15        | 54 | PC6         | 90  | PC10      | 126 | PD4       |
| 19 | PC13        | 55 | PD24        | 91  | PA3       | 127 | PC23      |
| 20 | PB1         | 56 | PA24        | 92  | PD12      | 128 | PD3       |
| 21 | PB0         | 57 | PD23        | 93  | PA2       | 129 | PA29      |
| 22 | PA20/PGMD12 | 58 | PC5         | 94  | PC11      | 130 | PC24      |
| 23 | PA19/PGMD11 | 59 | PA25        | 95  | GND       | 131 | PD2       |
| 24 | PA18/PGMD10 | 60 | PD22        | 96  | VDDIO     | 132 | PD1       |
| 25 | PA17/PGMD9  | 61 | GND         | 97  | PC14      | 133 | PC25      |
| 26 | PB2         | 62 | PA26        | 98  | PD11      | 134 | VDDIO     |
| 27 | PE4         | 63 | PD21        | 99  | PA1       | 135 | GND       |
| 28 | PE5         | 64 | PA11/PGMD3  | 100 | PC16      | 136 | PB10      |
| 29 | VDDCORE     | 65 | PD20        | 101 | PD10      | 137 | PB11      |
| 30 | VDDIO       | 66 | PA10/PGMD2  | 102 | PA0       | 138 | GND       |
| 31 | PB3         | 67 | PD19        | 103 | PC17      | 139 | VDDPLL    |
| 32 | PA21/PGMD13 | 68 | PA12/PGMD4  | 104 | JTAGSEL   | 140 | PB14      |
| 33 | VDDCORE     | 69 | PD18        | 105 | PB4       | 141 | PB8       |
| 34 | PD30        | 70 | PA27        | 106 | PD15      | 142 | PB9       |
| 35 | PA7/PGMN3   | 71 | PD28        | 107 | VDDCORE   | 143 | VDDIO     |
| 36 | PA8/PGMD0   | 72 | VDDIO       | 108 | PD29      | 144 | PB13      |

## 5. Ordering Information

Table 5-1. Ordering Codes for SAM4E Devices

| Ordering Code   | MRL | Flash (Kbytes) | RAM (Kbytes) | Package  | Conditioning | Package Type | Temperature Operating Range    |
|-----------------|-----|----------------|--------------|----------|--------------|--------------|--------------------------------|
| ATSAM4E16EA-CU  | A   | 1024           | 128          | LFBGA144 | Tray         | Green        | Industrial<br>(-40°C to 85°C)  |
| ATSAM4E16EA-CUR | A   |                |              |          | Reel         |              |                                |
| ATSAM4E16EA-AU  | A   |                |              | LQFP144  | Tray         |              | Industrial<br>(-40°C to 85°C)  |
| ATSAM4E16EA-AUR | A   |                |              |          | Reel         |              |                                |
| ATSAM4E16EA-AN  | A   |                |              | LQFP144  | Tray         |              | Industrial<br>(-40°C to 105°C) |
| ATSAM4E16EA-ANR | A   |                |              |          | Reel         |              |                                |
| ATSAM4E16CA-CU  | A   |                |              | TFBGA100 | Tray         |              | Industrial<br>(-40°C to 85°C)  |
| ATSAM4E16CA-CUR | A   |                |              |          | Reel         |              |                                |
| ATSAM4E16CA-AU  | A   |                |              | LQFP100  | Tray         |              | Industrial<br>(-40°C to 85°C)  |
| ATSAM4E16CA-AUR | A   |                |              |          | Reel         |              |                                |
| ATSAM4E16CA-AN  | A   |                |              | LQFP100  | Tray         |              | Industrial<br>(-40°C to 105°C) |
| ATSAM4E16CA-ANR | A   |                |              |          | Reel         |              |                                |
| ATSAM4E8EA-CU   | A   | 512            | 128          | LFBGA144 | Tray         | Green        | Industrial<br>(-40°C to 85°C)  |
| ATSAM4E8EA-CUR  | A   |                |              |          | Reel         |              |                                |
| ATSAM4E8EA-AU   | A   |                |              | LQFP144  | Tray         |              | Industrial<br>(-40°C to 85°C)  |
| ATSAM4E8EA-AUR  | A   |                |              |          | Reel         |              |                                |
| ATSAM4E8EA-AN   | A   |                |              | LQFP144  | Tray         |              | Industrial<br>(-40°C to 105°C) |
| ATSAM4E8EA-ANR  | A   |                |              |          | Reel         |              |                                |
| ATSAM4E8CA-CU   | A   |                |              | TFBGA100 | Tray         |              | Industrial<br>(-40°C to 85°C)  |
| ATSAM4E8CA-CUR  | A   |                |              |          | Reel         |              |                                |
| ATSAM4E8CA-AU   | A   |                |              | LQFP100  | Tray         |              | Industrial<br>(-40°C to 85°C)  |
| ATSAM4E8CA-AUR  | A   |                |              |          | Reel         |              |                                |
| ATSAM4E8CA-AN   | A   |                |              | LQFP100  | Tray         |              | Industrial<br>(-40°C to 105°C) |
| ATSAM4E8CA-ANR  | A   |                |              |          | Reel         |              |                                |

## Revision History

In the tables that follow, the most recent version of the document is referenced first.

“rfo” indicates changes requested during the document review and approval loop.

| Doc. Rev | Comments                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Change Request Ref.                                                 |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|
| 11157CS  | <p><b>Introduction</b></p> <p>In “Features” :</p> <ul style="list-style-type: none"> <li>- added information on Two-wire Interface in Peripherals section and Wake-on-LAN for EMAC</li> <li>- changed operating temperature range to 105°C</li> </ul> <p>Updated <a href="#">Table 1-1 “Configuration Summary”</a> with TWI informationIn <a href="#">Section 4. “Package and Pinout”</a>, added the FFPI signals to <a href="#">Table 4-1 “SAM4E 100-ball TFBGA Pinout”</a>, <a href="#">Table 4-2 “SAM4E 144-ball LFBGA Pinout”</a>, <a href="#">Table 4-3 “SAM4E 100-lead LQFP Pinout”</a> and <a href="#">Table 4-4 “SAM4E 144-lead LQFP Pinout”</a>.</p> <p>Removed Section 7. “Processor and Architecture”. Renumbered sections.</p> <p>Removed Sections 11-4 to 11-16.</p> <p><a href="#">Table 5-1, “Ordering Codes for SAM4E Devices”</a> updated with new ordering codes for parts at 105°C and for tape &amp; reel</p> | <p>rfo</p> <p>8992</p> <p>9045</p> <p>rfo</p> <p>rfo</p> <p>rfo</p> |

| Doc. Rev | Comments                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Change Request Ref.                               |
|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|
| 11157BS  | <p>Updated the document structure and added references to 100-ball TFBGA and 100-lead LQFP packages in:</p> <ul style="list-style-type: none"> <li>- <a href="#">Section 1. “Features”</a></li> <li>- <a href="#">Table 1-1 “Configuration Summary”</a></li> <li>- <a href="#">Figure 2-1 “SAM4E 100-pin Block Diagram”</a></li> <li>- <a href="#">Section 4.1 “100-ball TFBGA Package and Pinout”</a></li> <li>- <a href="#">Section 4.3 “100-lead LQFP Package and Pinout”</a></li> <li>- <a href="#">Section 5.1 “100-ball TFBGA Package Drawing”</a></li> <li>- <a href="#">Section 5.3 “100-lead LQFP Package Drawing”</a></li> <li>- <a href="#">Table 5-1 “Ordering Codes for SAM4E Devices”</a></li> </ul> <p>Updated the figure title and added Analog Comparator (ACC) and Reinforced Safety Watchdog Timer (RSWDT) blocks in <a href="#">Figure 2-2 “SAM4E 144-pin Block Diagram”</a>.</p> <p>Removed “AT91SAM” from the document title.</p> <p>Replaced “Cortex™” references with “Cortex®” in <a href="#">“Description”</a> and further on in the entire document.</p> <p>Removed package dimension references in <a href="#">Section 4. “Package and Pinout”</a>.</p> | <p>8580</p> <p>8605/rfo</p> <p>rfo</p> <p>rfo</p> |

| Doc. Rev | Comments         | Change Request Ref. |
|----------|------------------|---------------------|
| 11157AS  | Initial release. |                     |

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