



## ST1S06xx

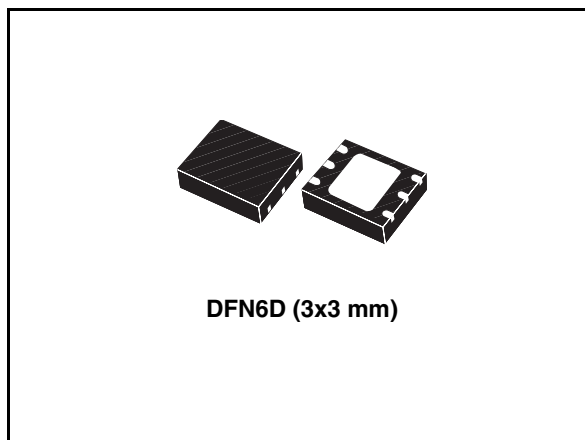
Synchronous rectification with inhibit, 1.5 A, 1.5 MHz fixed or adjustable, step-down switching regulator

### Features

- Step-down current mode PWM (1.5 MHz) DC-DC converter
- 2% DC output voltage tolerance
- Synchronous rectification
- Inhibit function
- Internal soft start
- Typical efficiency: > 90 %
- 1.5 A output current capability
- Not switching quiescent current: max 1.5 mA over temperature range
- $R_{DS(ON)}$  typ. 150 m $\Omega$
- Uses tiny capacitors and inductors
- Operative junction temp. - 30 °C to 125 °C
- Available in DFN6D (3x3 mm) exposed pad

### Description

The ST1S06xx is a step down DC-DC converter optimized for powering low-voltage digital core in HDD applications and, generally, to replace the high current linear solution when the power dissipation may cause an high heating of the application environment. It provides up to 1.5 A over an input voltage range of 2.7 V to 6 V. An high switching frequency (1.5 MHz) allows the use of tiny surface-mount components: as well as the resistor divider to set the output voltage value, only an inductor and two capacitors are required.



Besides, a low output ripple is guaranteed by the current mode PWM topology and by the use of low ESR SMD ceramic capacitors. The device is thermal protected and current limited to prevent damages due to accidental short circuit. The ST1S06xx is available in DFN6D (3x3 mm) package.

**Table 1. Device summary**

| Part numbers | Marking | Order codes | Package          |
|--------------|---------|-------------|------------------|
| ST1S06       | ST1S06  | ST1S06PUR   | DFN6D (3 x 3 mm) |
| ST1S06A      | ST1S06A | ST1S06APUR  | DFN6D (3 x 3 mm) |
| ST1S06XX12   | 1S0612  | ST1S06PU12R | DFN6D (3 x 3 mm) |
| ST1S06XX33   | 1S0633  | ST1S06PU33R | DFN6D (3 x 3 mm) |

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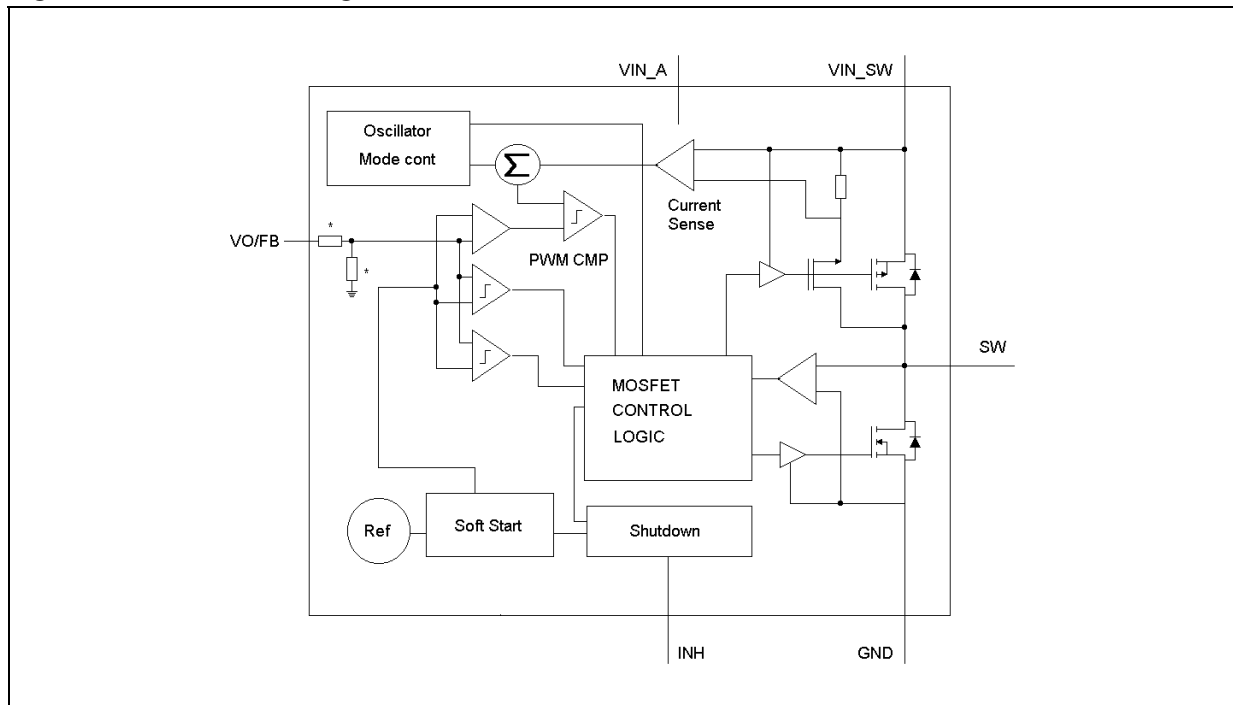
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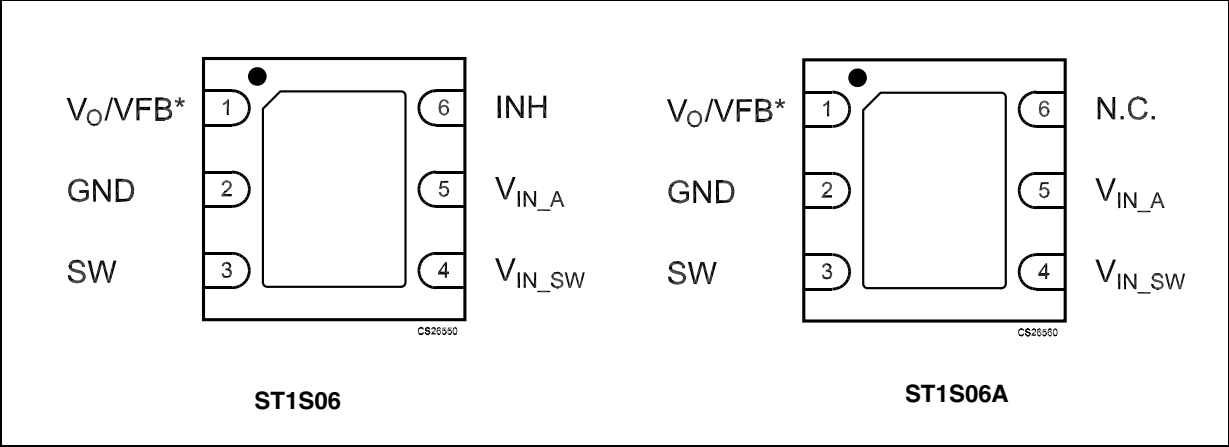
# 1 Diagram

Figure 1. Schematic diagram



## 2 Pin configuration

Figure 2. Pin configuration (top view)



\* Pin 1 is  $V_{FB}$  for ADJ version and  $V_O$  for Fixed version

Table 2. Pin description

| Pin n° | Symbol       | Note                               |
|--------|--------------|------------------------------------|
| 1      | FB/ $V_O$    | Feedback voltage / output voltage  |
| 2      | GND          | System ground                      |
| 3      | SW           | Switching pin                      |
| 4      | $V_{IN\_SW}$ | Power supply for the mosfet switch |
| 5      | $V_{IN\_A}$  | Power supply for analogic circuit  |
| 6      | $V_{INH}$    | Inhibit pin to turn off the device |
|        |              | Exposed pad to be connected to GND |

### 3 Maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol         | Parameter                           | Value               | Unit |
|----------------|-------------------------------------|---------------------|------|
| $V_{IN\_SW}$   | Positive power supply voltage       | -0.3 to 7           | V    |
| $V_{IN\_A}$    | Positive power supply voltage       | -0.3 to 7           | V    |
| $V_{INH}$      | Inhibit voltage                     | -0.3 to $V_I + 0.3$ | V    |
| SWITCH voltage | Max. voltage of output pin          | -0.3 to 7           | V    |
| $V_{FB}/V_O$   | Feedback voltage                    | -0.3 to 2.5         | V    |
| $V_O$          | Output voltage (for $V_O > 1.6$ V)  | -0.3 to 6           | V    |
| $T_J$          | Max junction temperature            | -40 to 150          | °C   |
| $T_{STG}$      | Storage temperature range           | -65 to 150          | °C   |
| $T_{LEAD}$     | Lead temperature (soldering) 10 sec | 260                 | °C   |

*Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.*

**Table 4. Thermal data**

| Symbol     | Parameter                           | Value | Unit |
|------------|-------------------------------------|-------|------|
| $R_{thJA}$ | Thermal resistance junction-ambient | 55    | °C/W |
| $R_{thJC}$ | Thermal resistance junction-case    | 10    | °C/W |

## 4 Electrical characteristics

$V_{IN\_SW} = V_{IN\_A} = V_{INH} = 5\text{ V}$ ,  $V_O = 1.2\text{ V}$ ,  $C_I = 4.7\text{ }\mu\text{F}$ ,  $C_O = 22\text{ }\mu\text{F}$ ,  $L1 = 3.3\text{ }\mu\text{H}$ ,  $T_J = -30\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$  unless otherwise specified. Typical values are referred to  $T_J = 25\text{ }^\circ\text{C}$ .

**Table 5. Electrical characteristics for ST1S06**

| Symbol             | Parameter                         | Test conditions                                                                                                          | Min. | Typ. | Max. | Unit               |
|--------------------|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------|------|------|------|--------------------|
| FB                 | Feedback voltage                  |                                                                                                                          | 784  | 800  | 816  | mV                 |
| $I_{FB}$           | $V_{FB}$ pin bias current         |                                                                                                                          |      |      | 600  | nA                 |
| $V_I$              | Minimum input voltage             | $I_O = 10\text{mA}$ to $1.5\text{A}$                                                                                     | 2.7  |      |      | V                  |
| $I_Q$              | Quiescent current                 | $V_{INH} > 1.2\text{V}$                                                                                                  |      |      | 1.5  | mA                 |
|                    |                                   | $V_{INH} < 0.4\text{V}$ , $T_J = -30^\circ\text{C}$ to $85^\circ\text{C}$                                                |      |      | 1    | $\mu\text{A}$      |
| $I_O$              | Output current                    | $V_I = 2.7$ to $5.5\text{V}$ <a href="#">Note 1</a>                                                                      | 1.5  |      |      | A                  |
| $V_{INH}$          | Inhibit threshold                 | Device ON, $V_I = 2.7$ to $5.5\text{V}$                                                                                  | 1.3  |      |      | V                  |
|                    |                                   | Device ON, $V_I = 2.7$ to $5\text{V}$                                                                                    | 1.2  |      |      |                    |
|                    |                                   | Device OFF                                                                                                               |      |      | 0.4  |                    |
| $I_{INH}$          | Inhibit pin current               |                                                                                                                          |      |      | 2    | $\mu\text{A}$      |
| $\%V_O/\Delta V_I$ | Reference line regulation         | $V_I = 2.7\text{V}$ to $5.5\text{V}$ <a href="#">Note 1</a>                                                              |      | 0.2  | 0.3  | $\%V_O/\Delta V_I$ |
| $\%V_O/\Delta I_O$ | Reference load regulation         | $I_O = 10\text{mA}$ to $1.5\text{A}$ <a href="#">Note 1</a>                                                              |      | 0.2  | 0.3  | $\%V_O/\Delta I_O$ |
| $\text{PWMf}_S$    | PWM switching frequency           | $V_{FB} = 0.8\text{V}$                                                                                                   | 1.2  | 1.5  | 1.8  | MHz                |
| $D_{MAX}$          | Maximum duty cycle                |                                                                                                                          | 80   | 87   |      | %                  |
| $R_{DS(on)-N}$     | NMOS switch on resistance         | $I_{SW} = 750\text{ mA}$                                                                                                 |      | 0.12 |      | $\Omega$           |
| $R_{DS(on)-P}$     | PMOS switch on resistance         | $I_{SW} = 750\text{ mA}$                                                                                                 |      | 0.15 |      | $\Omega$           |
| $I_{SWL}$          | Switching current limitation      | <a href="#">Note 1</a>                                                                                                   |      | 2.3  |      | A                  |
| $\eta$             | Efficiency <a href="#">Note 1</a> | $I_O = 10\text{mA}$ to $100\text{mA}$ , $V_O = 3.3\text{V}$                                                              | 65   |      |      | %                  |
|                    |                                   | $I_O = 100\text{mA}$ to $1.5\text{A}$ , $V_O = 3.3\text{V}$                                                              | 85   | 90   |      |                    |
| $T_{SHDN}$         | Thermal shutdown                  |                                                                                                                          | 130  | 150  |      | $^\circ\text{C}$   |
| $T_{HYS}$          | Thermal shutdown hysteresis       |                                                                                                                          |      | 15   |      | $^\circ\text{C}$   |
| $\%V_O/\Delta I_O$ | Load transient response           | $I_O = 100\text{mA}$ to $750\text{mA}$ , $T_J = 25^\circ\text{C}$ $t_R = t_F \geq 200\text{ns}$ , <a href="#">Note 1</a> | -5   |      | +5   | $\%V_O$            |
| $\%V_O/\Delta I_O$ | Short circuit removal response    | $I_O = 10\text{mA}$ to $I_O = \text{short}$ , $T_J = 25^\circ\text{C}$ <a href="#">Note 1</a>                            | -10  |      | +10  | $\%V_O$            |

**Note:** 1 Guaranteed by design, but not tested in production

$V_{IN\_SW} = V_{IN\_A} = V_{INH} = 5\text{ V}$ ,  $V_O = 1.2\text{ V}$ ,  $C_I = 4.7\text{ }\mu\text{F}$ ,  $C_O = 22\text{ }\mu\text{F}$ ,  $L1 = 3.3\text{ }\mu\text{H}$ ,  $T_J = -30\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$  unless otherwise specified. Typical values are referred to  $T_J = 25\text{ }^{\circ}\text{C}$ .

**Table 6. Electrical characteristics for ST1S06PM12**

| Symbol             | Parameter                      | Test conditions                                                                                                      | Min.  | Typ. | Max.  | Unit               |
|--------------------|--------------------------------|----------------------------------------------------------------------------------------------------------------------|-------|------|-------|--------------------|
| OUT                | Output feedback pin            |                                                                                                                      | 1.176 | 1.2  | 1.224 | V                  |
| $I_O$              | $I_O$ pin bias current         | $V_O = 1.5\text{ V}$                                                                                                 |       | 15   | 20    | $\mu\text{A}$      |
| $V_I$              | Minimum input voltage          | $I_O = 10\text{ mA}$ to $1.5\text{ A}$                                                                               | 2.7   |      |       | V                  |
| $I_Q$              | Quiescent current              | $V_{INH} > 1.2\text{ V}$                                                                                             |       |      | 1.5   | $\text{mA}$        |
|                    |                                | $V_{INH} < 0.4\text{ V}$ , $T_J = -30^{\circ}\text{C}$ to $85^{\circ}\text{C}$                                       |       |      | 1     | $\mu\text{A}$      |
| $I_O$              | Output current                 | $V_I = 2.7$ to $5.5\text{ V}$ <i>Note 1</i>                                                                          | 1.5   |      |       | A                  |
| $V_{INH}$          | Inhibit threshold              | Device ON, $V_I = 2.7$ to $5.5\text{ V}$                                                                             | 1.3   |      |       | V                  |
|                    |                                | Device ON, $V_I = 2.7$ to $5\text{ V}$                                                                               | 1.2   |      |       |                    |
|                    |                                | Device OFF                                                                                                           |       |      | 0.4   |                    |
| $I_{INH}$          | Inhibit pin current            |                                                                                                                      |       |      | 2     | $\mu\text{A}$      |
| $\%V_O/\Delta V_I$ | Reference line regulation      | $V_I = 2.7\text{ V}$ to $5.5\text{ V}$ <i>Note 1</i>                                                                 |       | 0.2  | 0.3   | $\%V_O/\Delta V_I$ |
| $\%V_O/\Delta I_O$ | Reference load regulation      | $I_O = 10\text{ mA}$ to $1.5\text{ A}$ <i>Note 1</i>                                                                 |       | 0.2  | 0.3   | $\%V_O/\Delta I_O$ |
| $\text{PWM}f_S$    | PWM switching frequency        | $V_{FB} = 0.8\text{ V}$                                                                                              | 1.2   | 1.5  | 1.8   | MHz                |
| $D_{MAX}$          | Maximum duty cycle             |                                                                                                                      | 80    | 87   |       | %                  |
| $R_{DS(on)-N}$     | NMOS switch on resistance      | $I_{SW} = 750\text{ mA}$                                                                                             |       | 0.12 |       | $\Omega$           |
| $R_{DS(on)-P}$     | PMOS switch on resistance      | $I_{SW} = 750\text{ mA}$                                                                                             |       | 0.15 |       | $\Omega$           |
| $I_{SWL}$          | Switching current limitation   | <i>Note 1</i>                                                                                                        |       | 2.3  |       | A                  |
| $\eta$             | Efficiency <i>Note 1</i>       | $I_O = 10\text{ mA}$ to $100\text{ mA}$ , $V_O = 1.2\text{ V}$                                                       | 60    |      |       | %                  |
|                    |                                | $I_O = 100\text{ mA}$ to $1.5\text{ A}$ , $V_O = 1.2\text{ V}$                                                       | 80    | 85   |       |                    |
| $T_{SHDN}$         | Thermal shutdown               |                                                                                                                      | 130   | 150  |       | $^{\circ}\text{C}$ |
| $T_{HYS}$          | Thermal shutdown hysteresis    |                                                                                                                      |       | 15   |       | $^{\circ}\text{C}$ |
| $\%V_O/\Delta I_O$ | Load transient response        | $I_O = 100\text{ mA}$ to $750\text{ mA}$ , $T_J = 25^{\circ}\text{C}$ $t_R = t_F \geq 200\text{ ns}$ , <i>Note 1</i> | -5    |      | +5    | $\%V_O$            |
| $\%V_O/\Delta I_O$ | Short circuit removal response | $I_O = 10\text{ mA}$ to $I_O = \text{short}$ , $T_J = 25^{\circ}\text{C}$ <i>Note 1</i>                              | -10   |      | +10   | $\%V_O$            |

*Note: 1 Guaranteed by design, but not tested in production*

$V_{IN\_SW} = V_{IN\_A} = V_{INH} = 5\text{ V}$ ,  $V_O = 3.3\text{ V}$ ,  $C_I = 4.7\text{ }\mu\text{F}$ ,  $C_O = 22\text{ }\mu\text{F}$ ,  $L1 = 3.3\text{ }\mu\text{H}$ ,  $T_J = -30\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$  unless otherwise specified. Typical values are referred to  $T_J = 25\text{ }^\circ\text{C}$ .

**Table 7. Electrical characteristics for ST1S06PM33**

| Symbol             | Parameter                      | Test conditions                                                                                                            | Min. | Typ. | Max. | Unit               |
|--------------------|--------------------------------|----------------------------------------------------------------------------------------------------------------------------|------|------|------|--------------------|
| OUT                | Output feedback pin            |                                                                                                                            | 3.23 | 3.3  | 3.37 | V                  |
| $I_O$              | $I_O$ pin bias current         | $V_O = 3.5\text{ V}$                                                                                                       |      | 15   | 20   | $\mu\text{A}$      |
| $V_I$              | Minimum input voltage          | $I_O = 10\text{ mA}$ to $1.5\text{ A}$                                                                                     | 4.2  |      |      | V                  |
| $I_Q$              | Quiescent current              | $V_{INH} > 1.2\text{ V}$                                                                                                   |      |      | 1.5  | $\text{mA}$        |
|                    |                                | $V_{INH} < 0.4\text{ V}$ , $T_J = -30\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$                                 |      |      | 1    | $\mu\text{A}$      |
| $I_O$              | Output current                 | $V_I = 4.2$ to $5.5\text{ V}$ <i>Note 1</i>                                                                                | 1.5  |      |      | A                  |
| $V_{INH}$          | Inhibit threshold              | Device ON, $V_I = 4.2$ to $5.5\text{ V}$                                                                                   | 1.3  |      |      | V                  |
|                    |                                | Device ON, $V_I = 4.2$ to $5\text{ V}$                                                                                     | 1.2  |      |      |                    |
|                    |                                | Device OFF                                                                                                                 |      |      | 0.4  |                    |
| $I_{INH}$          | Inhibit pin current            |                                                                                                                            |      |      | 2    | $\mu\text{A}$      |
| $\%V_O/\Delta V_I$ | Reference line regulation      | $V_I = 4.2\text{ V}$ to $5.5\text{ V}$ <i>Note 1</i>                                                                       |      | 0.2  | 0.3  | $\%V_O/\Delta V_I$ |
| $\%V_O/\Delta I_O$ | Reference load regulation      | $I_O = 10\text{ mA}$ to $1.5\text{ A}$ <i>Note 1</i>                                                                       |      | 0.2  | 0.3  | $\%V_O/\Delta I_O$ |
| $\text{PWM}f_S$    | PWM switching frequency        | $V_{FB} = 0.8\text{ V}$                                                                                                    | 1.2  | 1.5  | 1.8  | MHz                |
| $D_{MAX}$          | Maximum duty cycle             |                                                                                                                            | 80   | 87   |      | %                  |
| $R_{DS(on)-N}$     | NMOS switch on resistance      | $I_{SW} = 750\text{ mA}$                                                                                                   |      | 0.12 |      | $\Omega$           |
| $R_{DS(on)-P}$     | PMOS switch on resistance      | $I_{SW} = 750\text{ mA}$                                                                                                   |      | 0.15 |      | $\Omega$           |
| $I_{SWL}$          | Switching current limitation   | <i>Note 1</i>                                                                                                              |      | 2.3  |      | A                  |
| $\eta$             | Efficiency <i>Note 1</i>       | $I_O = 10\text{ mA}$ to $100\text{ mA}$ , $V_O = 3.3\text{ V}$                                                             | 65   |      |      | %                  |
|                    |                                | $I_O = 100\text{ mA}$ to $1.5\text{ A}$ , $V_O = 3.3\text{ V}$                                                             | 85   | 90   |      |                    |
| $T_{SHDN}$         | Thermal shutdown               |                                                                                                                            | 130  | 150  |      | $^\circ\text{C}$   |
| $T_{HYS}$          | Thermal shutdown hysteresis    |                                                                                                                            |      | 15   |      | $^\circ\text{C}$   |
| $\%V_O/\Delta I_O$ | Load transient response        | $I_O = 100\text{ mA}$ to $750\text{ mA}$ , $T_J = 25\text{ }^\circ\text{C}$ $t_R = t_F \geq 200\text{ ns}$ , <i>Note 1</i> | -5   |      | +5   | $\%V_O$            |
| $\%V_O/\Delta I_O$ | Short circuit removal response | $I_O = 10\text{ mA}$ to $I_O = \text{short}$ , $T_J = 25\text{ }^\circ\text{C}$ <i>Note 1</i>                              | -10  |      | +10  | $\%V_O$            |

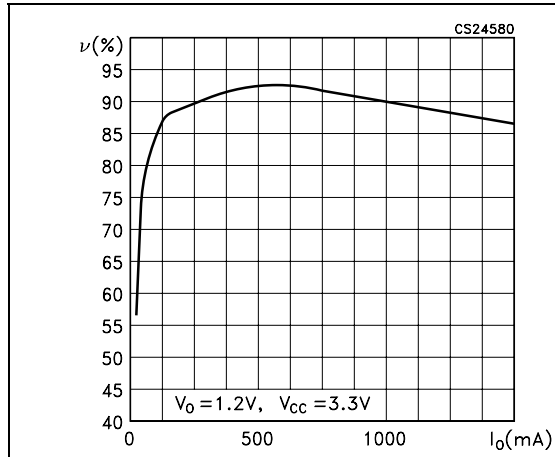
*Note: 1 Guaranteed by design, but not tested in production*



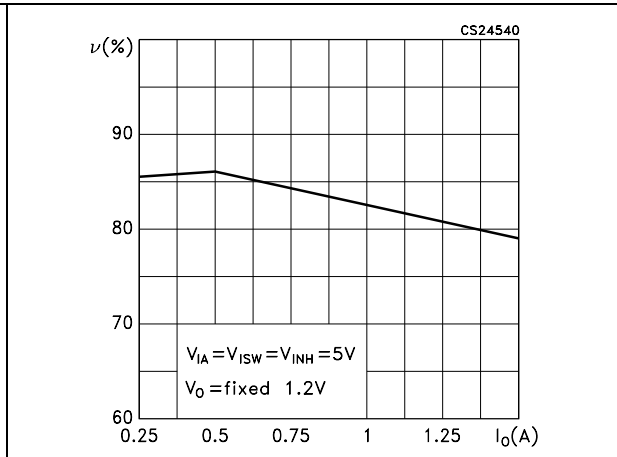
## 5 Typical performance characteristics

$V_{IN\_SW} = V_{IN\_A} = V_{INH} = 5\text{ V}$ ,  $C_I = 4.7\text{ }\mu\text{F}$ ,  $C_O = 22\text{ }\mu\text{F}$ ,  $L_1 = 3.3\text{ }\mu\text{H}$ , unless otherwise specified. Typical values are referred to  $25\text{ }^\circ\text{C}$ .

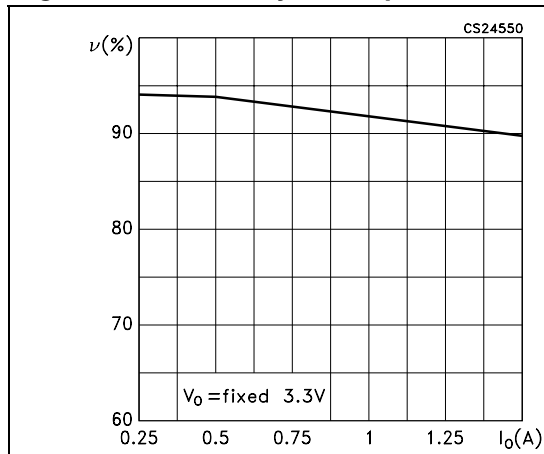
**Figure 3. Efficiency vs. output current**



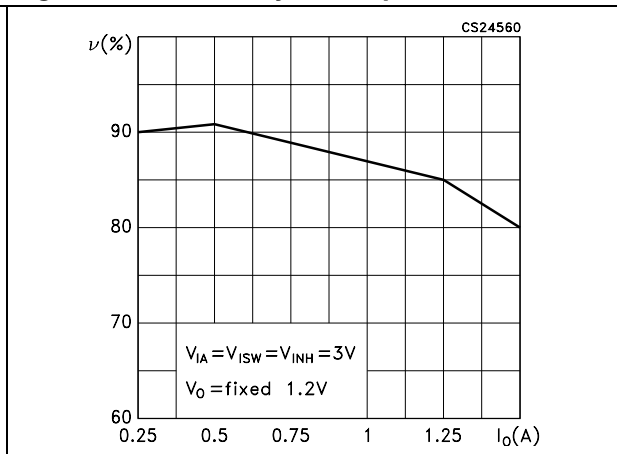
**Figure 4. Efficiency vs. output current**



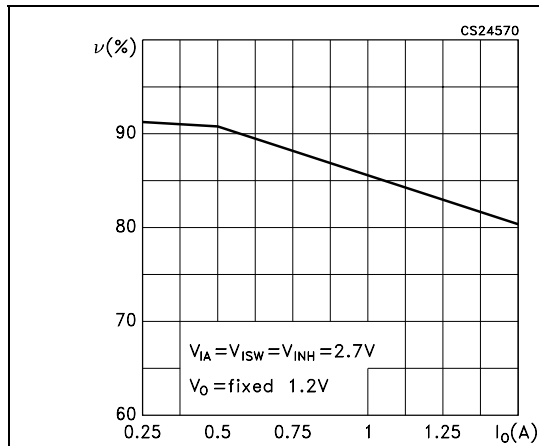
**Figure 5. Efficiency vs. output current**



**Figure 6. Efficiency vs. output current**



**Figure 7. Efficiency vs. output current**



**Figure 8. Efficiency vs. inductor**

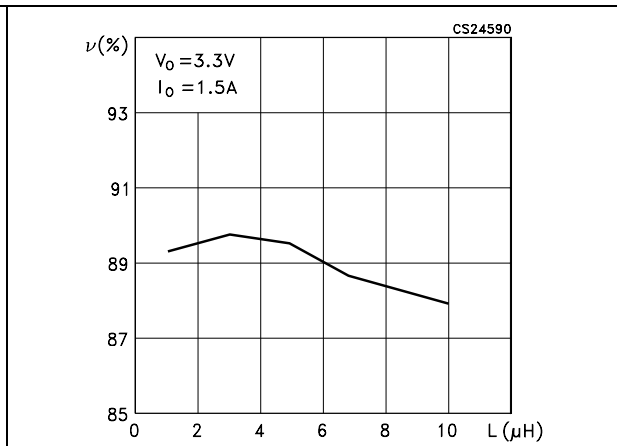


Figure 9. Voltage feedback vs. temperature

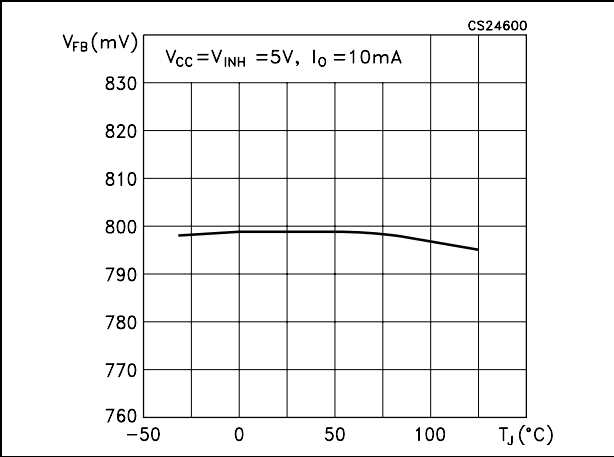


Figure 10. Input voltage vs. output voltage

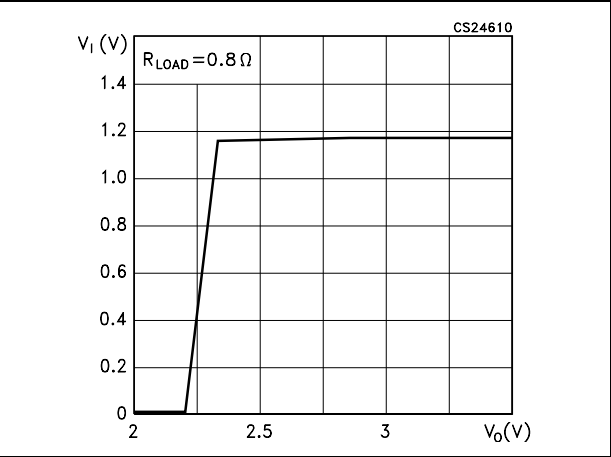


Figure 11. Feedback pin bias current vs. temperature

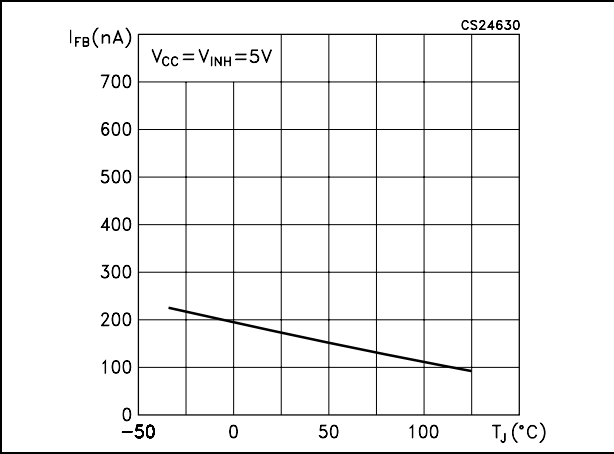


Figure 12. Quiescent current vs. temperature

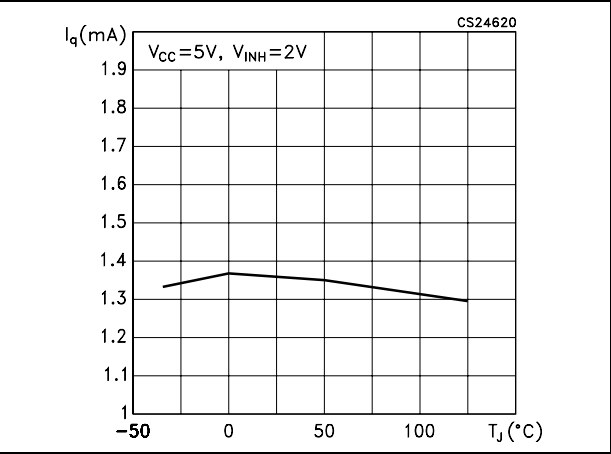


Figure 13. Quiescent current vs. temperature

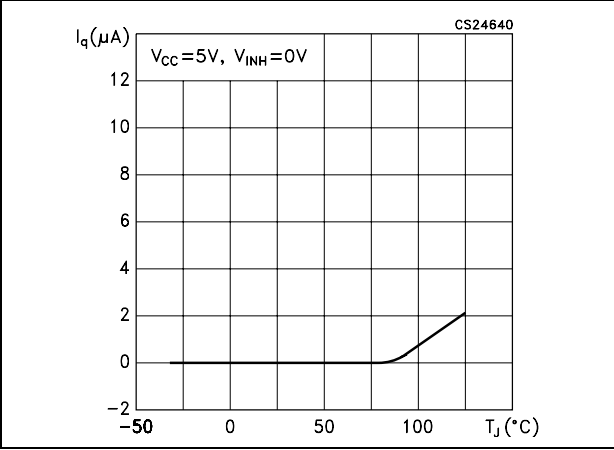


Figure 14. Inhibit voltage vs. input voltage

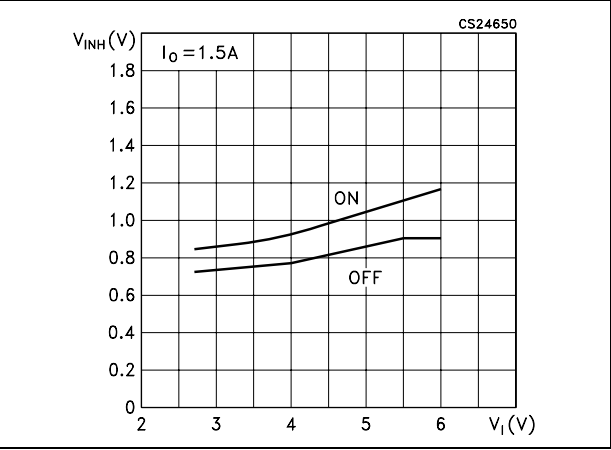


Figure 15. Inhibit voltage vs. temperature

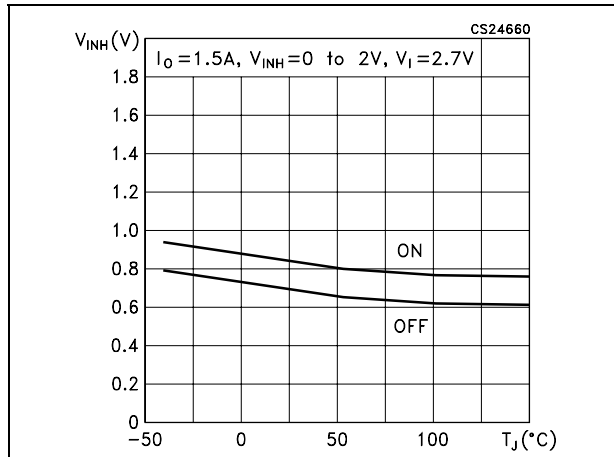


Figure 16. Inhibit voltage vs. temperature

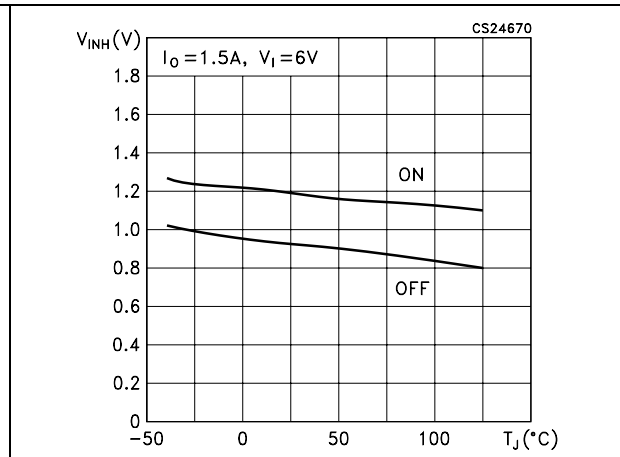


Figure 17. Line regulation vs. temperature

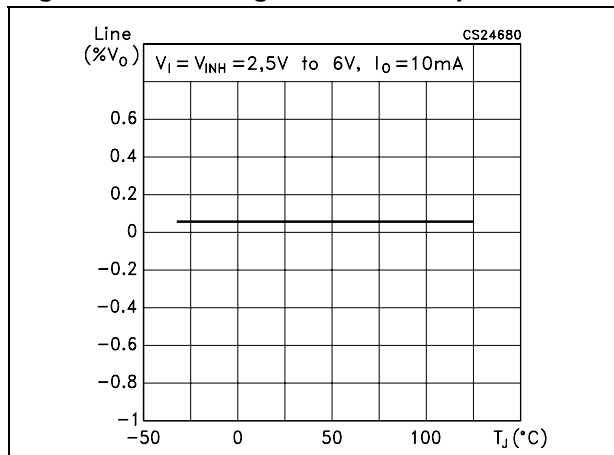


Figure 18. Load regulation vs. temperature

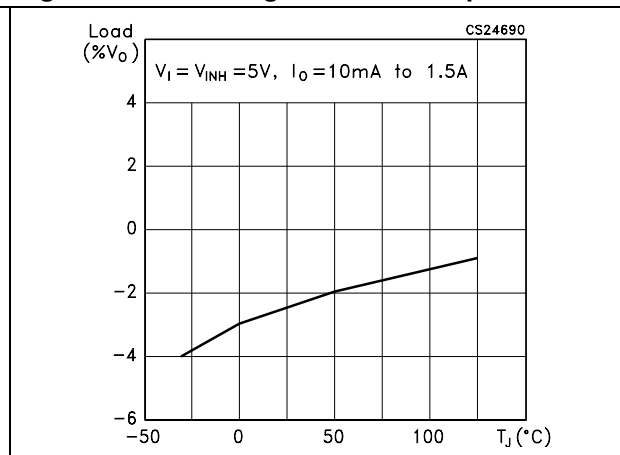


Figure 19. PWM switching frequency vs. temperature

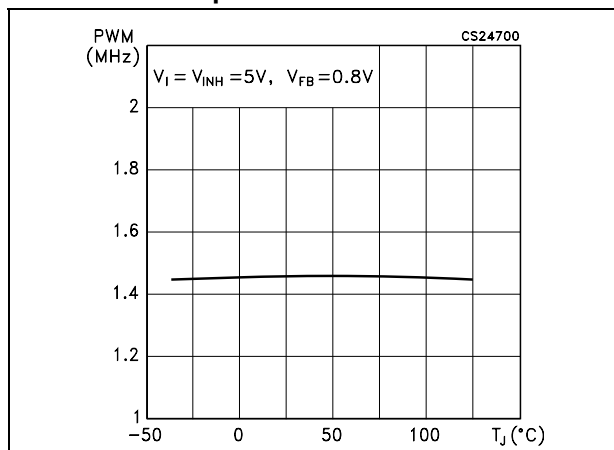


Figure 20. NMOS switch on resistance vs. temperature

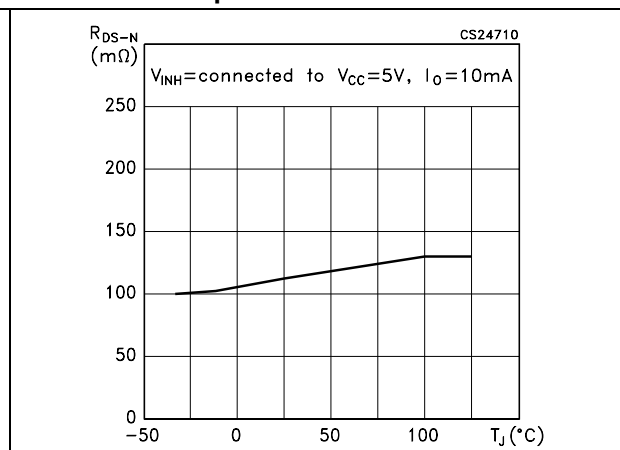


Figure 21. PMOS switch on resistance vs. temperature

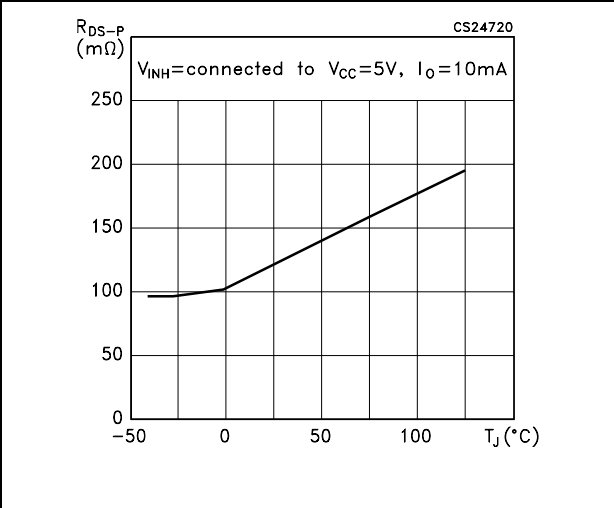


Figure 22. Inhibit transient

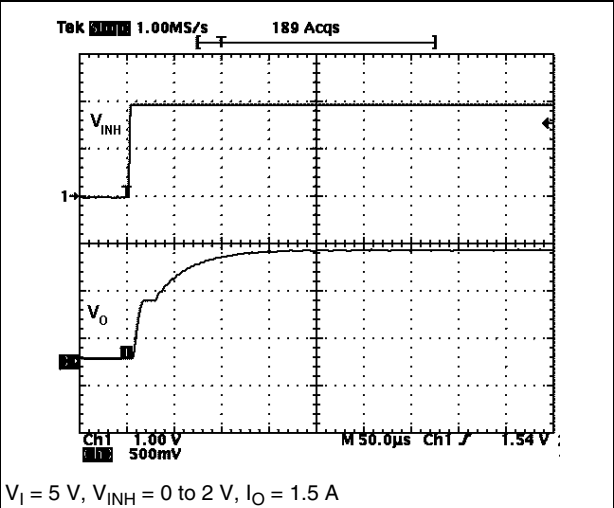
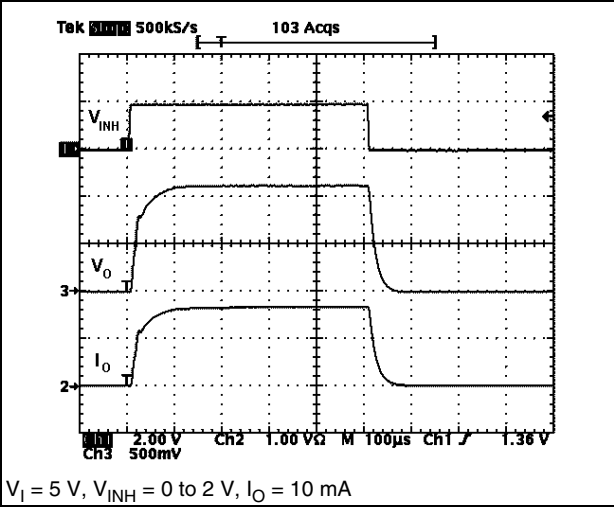
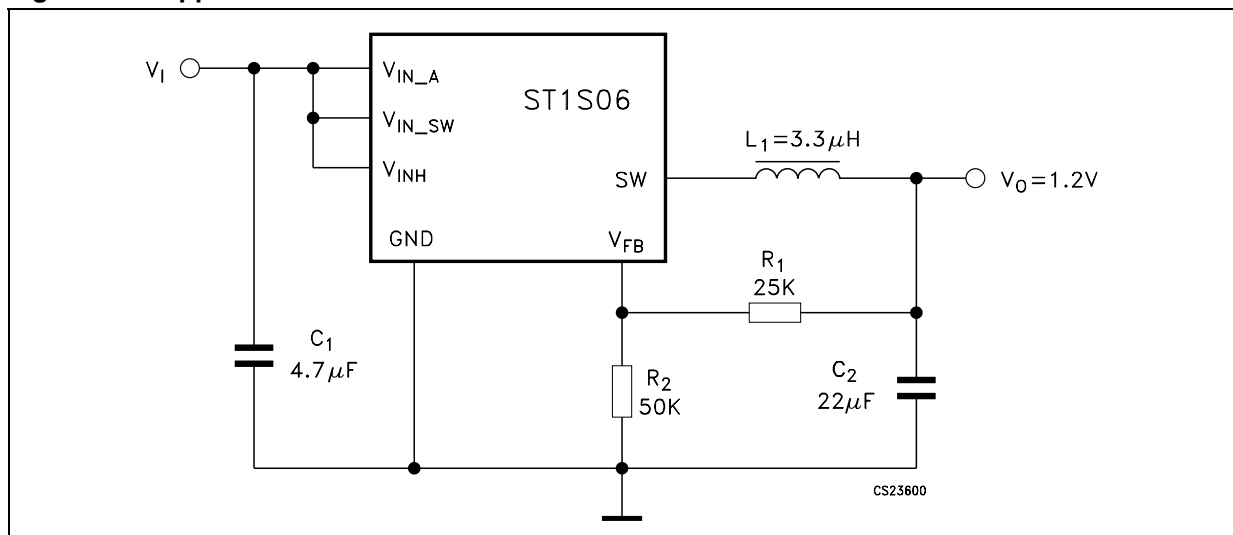


Figure 23. Inhibit transient



## 6 Typical application

Figure 24. Application circuit



## 7 Application notes

The ST1S06xx is an adjustable current mode PWM step-down DC-DC converter with internal 1.5 A power switch, packaged in a 6-lead DFN 3x3.

It's a complete 1.5 A switching regulator with its internal compensation eliminating additional component.

The constant frequency, current mode, PWM architecture and stable operation with ceramic capacitors results in low, predictable output ripple. However, in order to maximize the power conversion efficiency with light load, the regulator reduces automatically the switching frequency when the output load becomes less than 250 mA typically.

To clamp the error amplifier reference voltage a soft start control block generating a voltage ramp, has been implemented. Besides an on-chip power on reset of 50 = 100  $\mu$ s ensure the proper operation when switching on the power supply. Other circuits fitted to the device protection are the thermal shut down block which turn off the regulator when the junction temperature exceeds 150 °C typically and the cycle-by-cycle current limiting that provides protection against shorted outputs.

Being the ST1S06xx an adjustable regulator, the output voltage is determined by an external resistor divider. The desired value is given by the following equation:

$$V_O = V_{FB} [1 + R_1 / R_2]$$

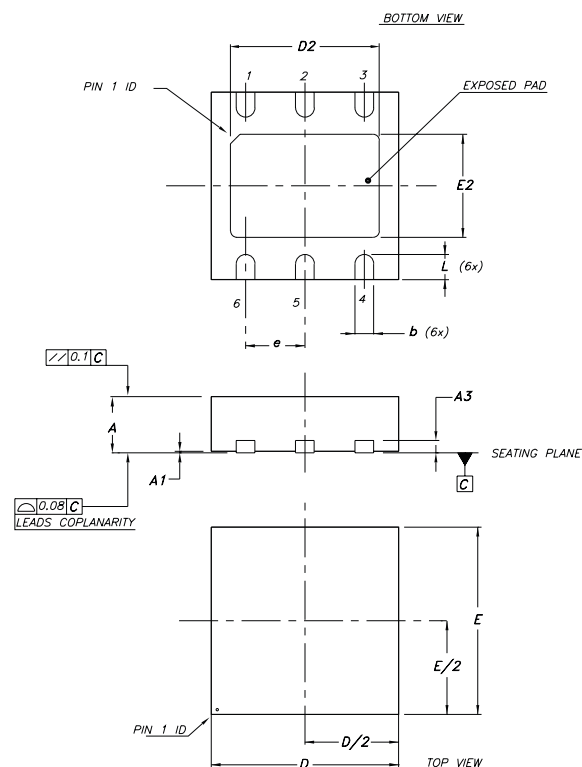
To make the device working, only few component are required: an inductor and two capacitors and the resistor divider. The chosen inductor must be able to not saturate at the peak current level. Besides, its value can be selected keeping in account that a large inductor value increases the efficiency at low output current and reduces output voltage ripple, while a smaller inductor can be chosen when it is important to reduce the package size and the total cost of the application. Finally, the ST1S06xx has been designed to work properly with X5R or X7R SMD ceramic capacitors both at the input and at the output. this kind of capacitors, thanks to their very low series resistance (ESR), minimize the output voltage ripple. Other low ESR capacitors can be used according to the need of the application without invalidate the right functioning of the device.

## 8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## DFN6D (3x3 mm) mechanical data

| Dim. | mm.  |      |      | inch. |       |       |
|------|------|------|------|-------|-------|-------|
|      | Min. | Typ. | Max. | Min.  | Typ.  | Max.  |
| A    | 0.80 |      | 1.00 | 0.031 |       | 0.039 |
| A1   | 0    | 0.02 | 0.05 | 0     | 0.001 | 0.002 |
| A3   |      | 0.20 |      |       | 0.008 |       |
| b    | 0.23 |      | 0.45 | 0.009 |       | 0.018 |
| D    | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| D2   | 2.23 |      | 2.50 | 0.088 |       | 0.098 |
| E    | 2.90 | 3.00 | 3.10 | 0.114 | 0.118 | 0.122 |
| E2   | 1.50 |      | 1.75 | 0.059 |       | 0.069 |
| e    |      | 0.95 |      |       | 0.037 |       |
| L    | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |

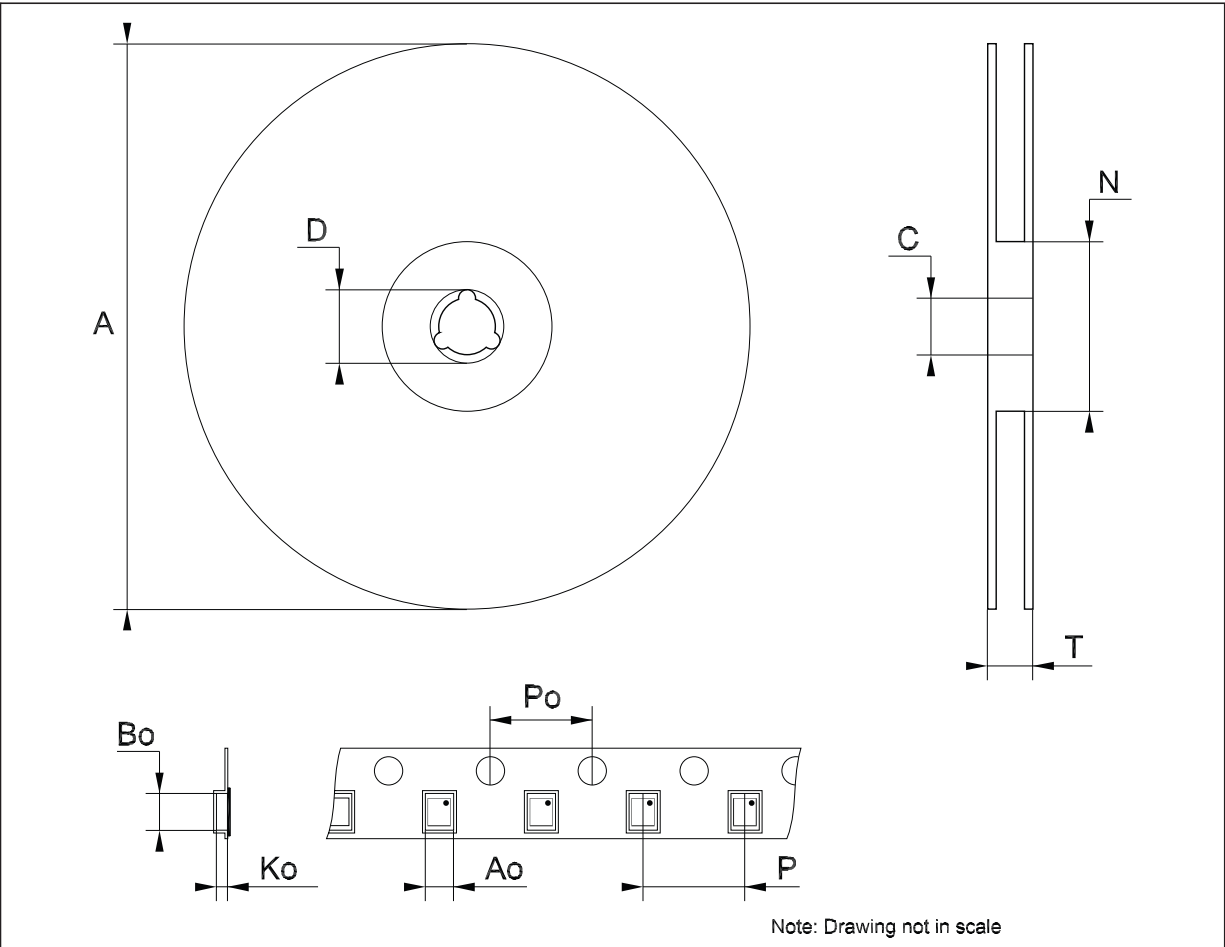


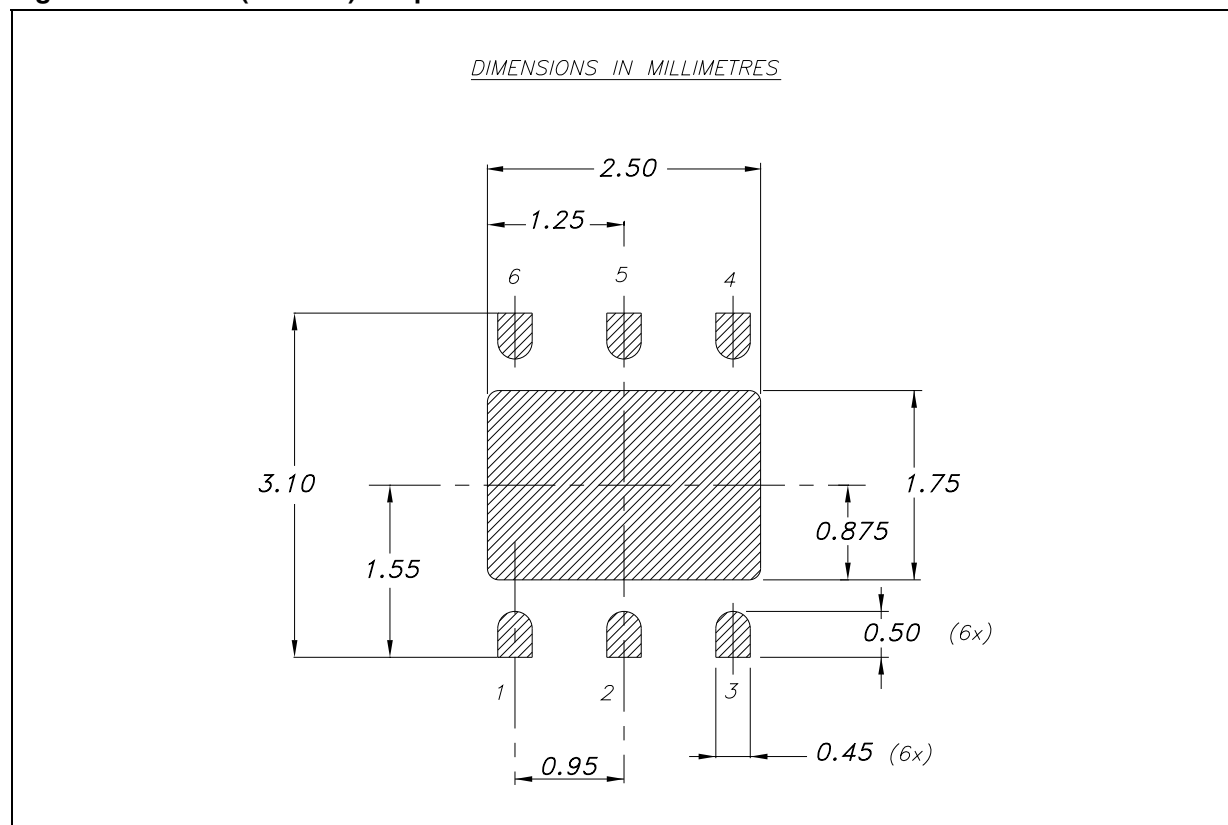
7946637B



Tape and reel QFNxx/DFNxx (3x3 mm) mechanical data

| Dim. | mm.  |      |      | inch. |       |        |
|------|------|------|------|-------|-------|--------|
|      | Min. | Typ. | Max. | Min.  | Typ.  | Max.   |
| A    |      |      | 330  |       |       | 12.992 |
| C    | 12.8 |      | 13.2 | 0.504 |       | 0.519  |
| D    | 20.2 |      |      | 0.795 |       |        |
| N    | 60   |      |      | 2.362 |       |        |
| T    |      |      | 18.4 |       |       | 0.724  |
| Ao   |      | 3.3  |      |       | 0.130 |        |
| Bo   |      | 3.3  |      |       | 0.130 |        |
| Ko   |      | 1.1  |      |       | 0.043 |        |
| Po   |      | 4    |      |       | 0.157 |        |
| P    |      | 8    |      |       | 0.315 |        |



**Figure 25. DFN6 (3x3 mm) footprint recommended data**

## 9 Revision history

**Table 8. Document revision history**

| Date        | Revision | Changes                                            |
|-------------|----------|----------------------------------------------------|
| 08-May-2006 | 1        | Initial release.                                   |
| 06-Jun-2006 | 2        | <a href="#">Table 3</a> updated.                   |
| 16-Oct-2006 | 3        | Add new mechanical data DFN6D.                     |
| 09-Nov-2006 | 4        | Mechanical data information for DFN6 update.       |
| 03-Apr-2007 | 5        | Tape and reel updated.                             |
| 12-Mar-2008 | 6        | Added: <a href="#">Table 1 on page 1</a> .         |
| 15-Apr-2008 | 7        | Modified: <a href="#">Figure 6 on page 9</a> .     |
| 10-Apr-2009 | 8        | Modified: <a href="#">Table 3 on page 5</a> .      |
| 06-May-2009 | 9        | Added: marking <a href="#">Table 1 on page 1</a> . |

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