CY23S08

3.3V Zero Delay Buffer

Features

- **Zero input-output propagation delay, adjustable by capacitive load on FBK input**
- **Multiple configurations, see *Table 2***
- **Multiple low-skew outputs**
  - **Output-output skew less than 200 ps**
  - **Device-device skew less than 700 ps**
  - **Two banks of four outputs, three-stateable by two select inputs**
- **10-MHz to 133-MHz operating range**
- **Low jitter, less than 200 ps cycle-cycle (–1, –1H, –4)**
- **Advanced 0.65μ CMOS technology**
- **Space-saving 16-pin 150-mil SOIC package**
- **3.3V operation**
- **Spread Aware™**

Functional Description

The CY23S08 is a 3.3V zero delay buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high-performance applications.

The part has an on-chip PLL which locks to an input clock presented on the REF pin. The PLL feedback is required to be driven into the FBK pin, and can be obtained from one of the outputs. The input-to-output propagation delay is guaranteed to be less than 350 ps, and output-to-output skew is guaranteed to be less than 250 ps.

The CY23S08 has two banks of four outputs each, which can be controlled by the Select inputs as shown in *Table 1*. If all output clocks are not required, Bank B can be three-stated. The select inputs also allow the input clock to be directly applied to the output for chip and system testing purposes.

The CY23S08 PLL enters a power-down state when there are no rising edges on the REF input. In this mode, all outputs are three-stated and the PLL is turned off, resulting in less than 50 μA of current draw. The PLL shuts down in two additional cases as shown in *Table 1*.

Multiple CY23S08 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 700 ps.

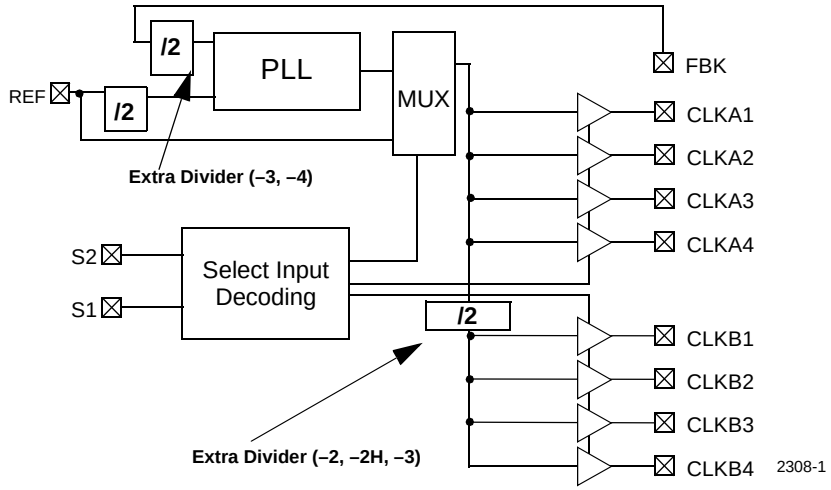
The CY23S08 is available in five different configurations, as shown in the *Table 2*. The CY23S08–1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path. The CY23S08–1H is the high-drive version of the –1, and rise and fall times on this device are much faster.

The CY23S08–2 allows the user to obtain 2X and 1X frequencies on each output bank. The exact configuration and output frequencies depends on which output drives the feedback pin. The CY23S08–2H is the high-drive version of the –2, and rise and fall times on this device are much faster.

The CY23S08–3 allows the user to obtain 4X and 2X frequencies on the outputs.

The CY23S08–4 enables the user to obtain 2X clocks on all outputs. Thus, the part is extremely versatile, and can be used in a variety of applications.

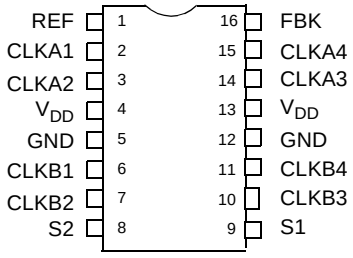
Block Diagram



2308-1

Pin Configuration

SOIC
Top View



2308-2

Table 1. Select Input Decoding.

S2	S1	CLOCK A1–A4	CLOCK B1–B4	Output Source	PLL Shutdown
0	0	Three-State	Three-State	PLL	Y
0	1	Driven	Three-State	PLL	N
1	0	Driven	Driven	Reference	Y
1	1	Driven	Driven	PLL	N

Table 2. Available CY23S08 Configurations.

Device	Feedback From	Bank A Frequency	Bank B Frequency
CY2308–1	Bank A or Bank B	Reference	Reference
CY2308–1H	Bank A or Bank B	Reference	Reference
CY2308–2	Bank A	Reference	Reference/2
CY2308–2H	Bank A	Reference	Reference/2
CY2308–2	Bank B	2 X Reference	Reference
CY2308–2H	Bank B	2 X Reference	Reference
CY2308–3	Bank A	2 X Reference	Reference or $\overline{\text{Reference}}$[1]
CY2308–3	Bank B	4 X Reference	2 X Reference
CY2308–4	Bank A or Bank B	2 X Reference	2 X Reference

Spread Aware™

Many systems being designed now utilize a technology called Spread Spectrum Frequency Timing Generation. Cypress has been one of the pioneers of SSFTG development, and we designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, please see Cypress's Application Note "EMI Suppression Techniques with Spread Spectrum Frequency Timing Generator (SSFTG) ICs."

Note:

1. Output phase is indeterminant (0° or 180° from input clock). If phase integrity is required, use the CY23S08–2.

Pin Description

Pin	Signal	Description
1	REF[2]	Input reference frequency, 5V tolerant input
2	CLKA1[3]	Clock output, Bank A
3	CLKA2[3]	Clock output, Bank A
4	V_{DD}	3.3V supply
5	GND	Ground
6	CLKB1[3]	Clock output, Bank B
7	CLKB2[3]	Clock output, Bank B
8	S2[4]	Select input, bit 2
9	S1[4]	Select input, bit 1
10	CLKB3[3]	Clock output, Bank B
11	CLKB4[3]	Clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3V supply
14	CLKA3[3]	Clock output, Bank A
15	CLKA4[3]	Clock output, Bank A
16	FBK	PLL feedback input

Maximum Ratings

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Input Voltage (Except Ref).....–0.5V to V_{DD} + 0.5V

DC Input Voltage REF.....–0.5 to 7V

Storage Temperature ..... –65°C to +150°C

Max. Soldering Temperature (10 sec.) ..... 260°C

Junction Temperature ..... 150°C

Static Discharge Voltage
(per MIL-STD-883, Method 3015) ..... >2000V

Notes:

2. Weak pull-down.
3. Weak pull-down on all outputs.
4. Weak pull-ups on these inputs.

Operating Conditions for CY23S08SC-XX Commercial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, below 100 MHz		30	pF
	Load Capacitance, from 100 MHz to 133 MHz		15	pF
C_{IN}	Input Capacitance[5]		7	pF

Electrical Characteristics for CY23S08SC-XX Commercial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	µA
V_{OL}	Output LOW Voltage[6]	I_{OL} = 8 mA (–1, –2, –3, –4) I_{OL} = 12 mA (-1H, -2H)		0.4	V
V_{OH}	Output HIGH Voltage[6]	I_{OH} = –8 mA (–1, –2, –3, –4) I_{OH} = –12mA (–1H, –2H)	2.4		V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		12.0	µA
I_{DD}	Supply Current	Unloaded outputs, 100-MHz REF, Select inputs at V_{DD} or GND		45.0	mA
				70.0 (-1H, -2H)	mA
		Unloaded outputs, 66-MHz REF (–1,–2,–3,–4)		32.0	mA
		Unloaded outputs, 33-MHz REF (–1,–2,–3,–4)		18.0	mA

Notes:

5. Applies to both Ref Clock and FBK.
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics for CY23S08SC-XX Commercial Temperature Devices [7]

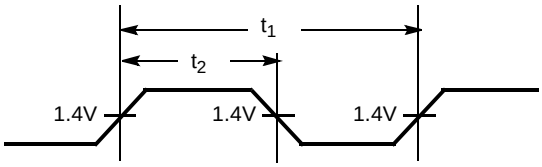
Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t_1	Output Frequency	30-pF load, All devices	10		100	MHz
t_1	Output Frequency	20-pF load, –1H device	10		133.3	MHz
t_1	Output Frequency	15-pF load, –1, –2, –3, –4 devices	10		133.3	MHz
	Duty Cycle[6] = $t_2 \div t_1$ (–1,–2,–3,–4,–1H, -2H)	Measured at 1.4V, F_{OUT} =66.66 MHz 30-pF load	40.0	50.0	60.0	%
	Duty Cycle[6] = $t_2 \div t_1$ (–1,–2,–3,–4,–1H, -2H)	Measured at 1.4V, F_{OUT} <50.0 MHz 15-pf load	45.0	50.0	55.0	%
t_3	Rise Time[6] (–1, –2, –3, –4)	Measured between 0.8V and 2.0V, 30-pF load			2.20	ns
t_3	Rise Time[6] (–1, –2, –3, –4)	Measured between 0.8V and 2.0V, 15-pF load			1.50	ns
t_3	Rise Time[6] (–1H, -2H)	Measured between 0.8V and 2.0V, 30-pF load			1.50	ns
t_4	Fall Time[6] (–1, –2, –3, –4)	Measured between 0.8V and 2.0V, 30-pF load			2.20	ns
t_4	Fall Time[6] (–1, –2, –3, –4)	Measured between 0.8V and 2.0V, 15-pF load			1.50	ns
t_4	Fall Time[6] (–1H, 2H)	Measured between 0.8V and 2.0V, 30-pF load			1.25	ns
t_5	Output to Output Skew on same Bank (–1,–2,–3,–4)[6]	All outputs equally loaded			200	ps
	Output to Output Skew (–1H, -2H)	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (–1,–4)	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (–2,–3)	All outputs equally loaded			400	ps
t_6	Delay, REF Rising Edge to FBK Rising Edge[6]	Measured at $V_{DD}/2$		0	±250	ps
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the FBK pins of devices		0	700	ps
t_8	Output Slew Rate[6]	Measured between 0.8V and 2.0V on –1H, -2H device using Test Circuit #2	1			V/ns
t_J	Cycle to Cycle Jitter[6] (–1, –1H, –4)	Measured at 66.67 MHz, loaded outputs, 15-pF load			200	ps
		Measured at 66.67 MHz, loaded outputs, 30-pF load			200	ps
		Measured at 133.3 MHz, loaded outputs, 15-pF load			100	ps
t_J	Cycle to Cycle Jitter[6] (–2, -2H, –3)	Measured at 66.67 MHz, loaded outputs 30-pF load			400	ps
		Measured at 66.67 MHz, loaded outputs 15-pF load			400	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clocks presented on REF and FBK pins			1.0	ms

Notes:

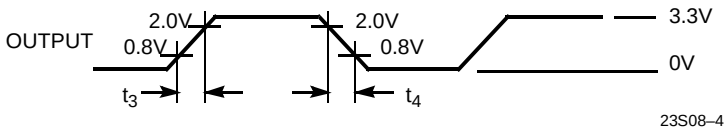
7. All parameters are specified with loaded outputs.

Switching Waveforms

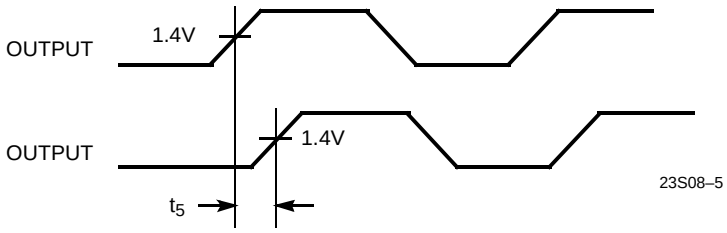
Duty Cycle Timing



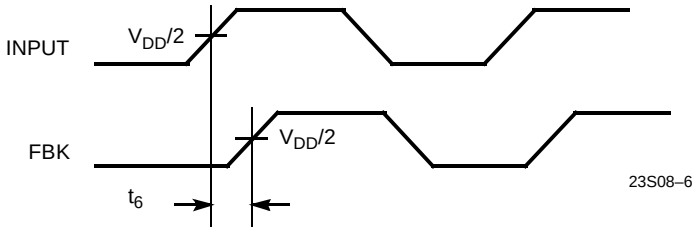
All Outputs Rise/Fall Time



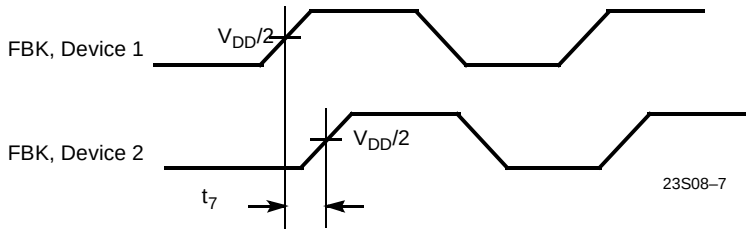
Output-Output Skew



Input-Output Propagation Delay

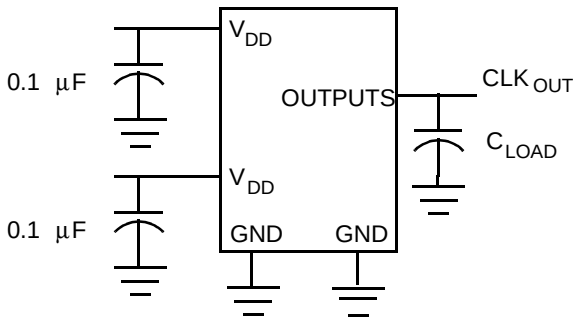


Device-Device Skew



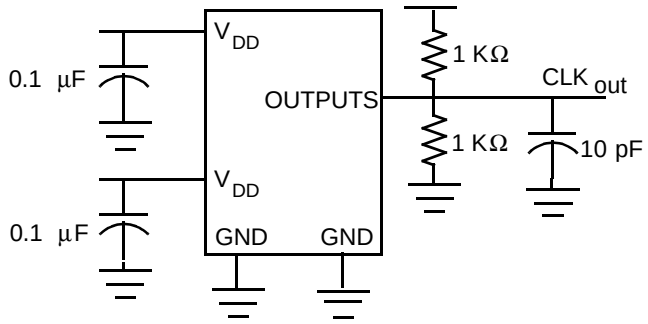
Test Circuits

Test Circuit # 1



Test Circuit for all parameters except t_8

Test Circuit # 2



Test Circuit for t_8, Output slew rate on –1H device

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY23S08SC–1	S16	16-pin 150-mil SOIC	Commercial
CY23S08SC–1H	S16	16-pin 150-mil SOIC	Commercial
CY23S08ZC–1H	Z16	16-pin 150-mil TSSOP	Commercial
CY23S08SC–2	S16	16-pin 150-mil SOIC	Commercial
CY23S08SC–2H	S16	16-pin 150-mil SOIC	Commercial
CY23S08SC–3	S16	16-pin 150-mil SOIC	Commercial
CY23S08SC–4	S16	16-pin 150-mil SOIC	Commercial

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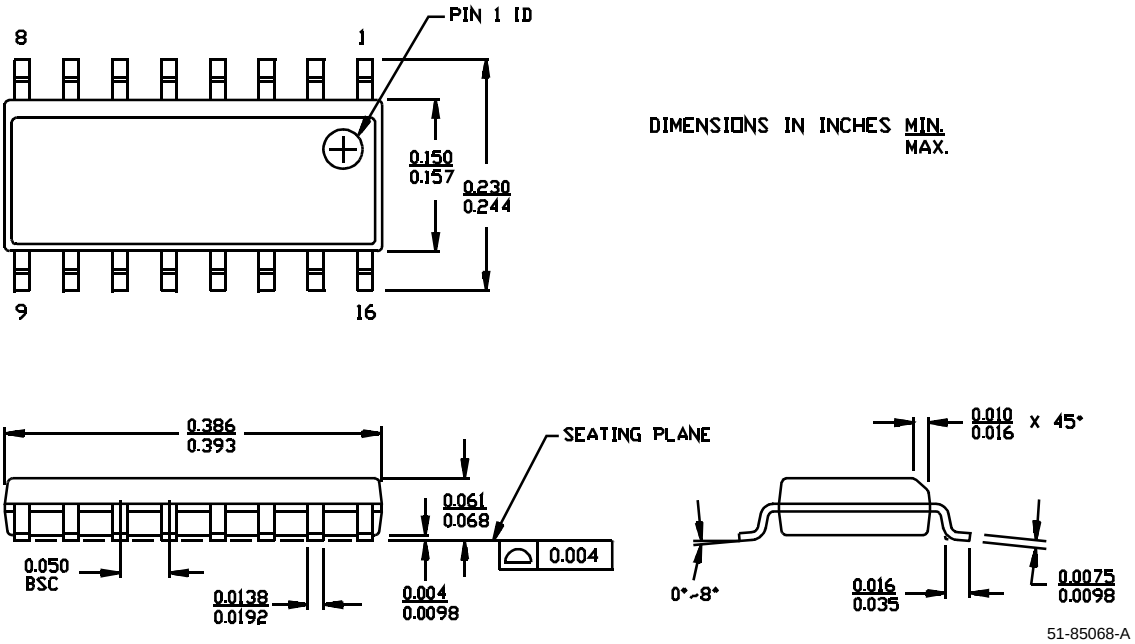
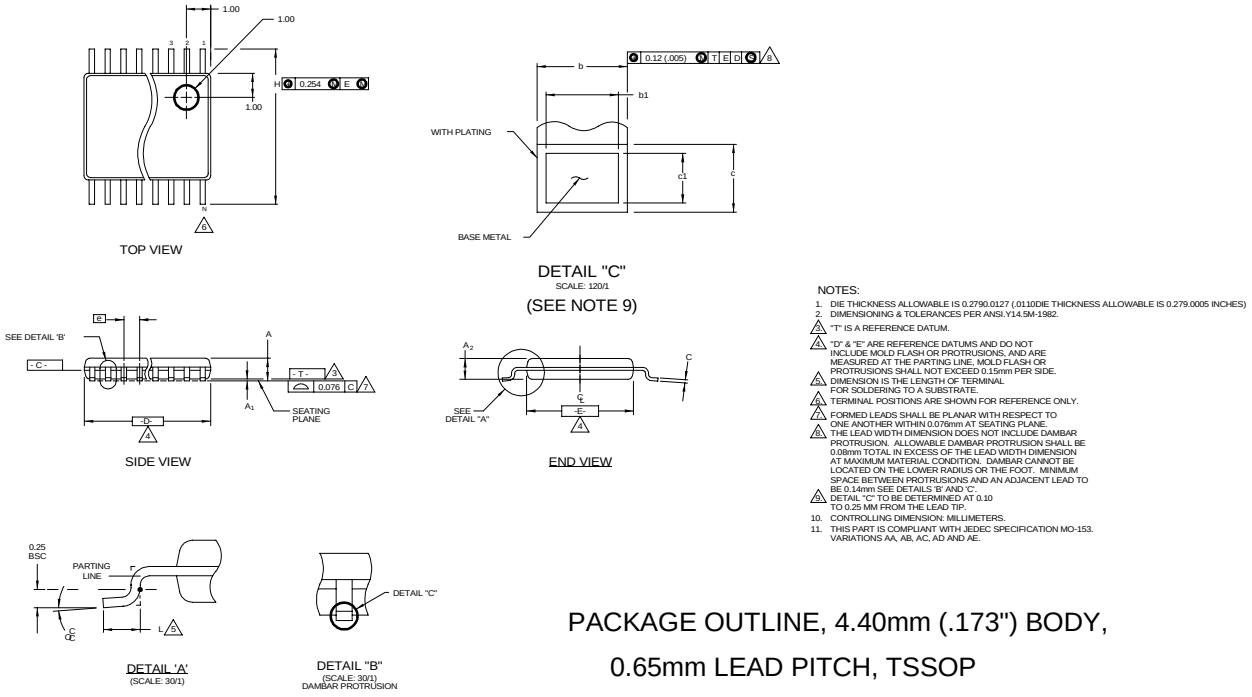
Package Diagrams

16-Lead (150-Mil) Molded SOIC S16



51-85068-A

16-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16



PACKAGE OUTLINE, 4.40mm (.173") BODY,
0.65mm LEAD PITCH, TSSOP