TPS22908 3.6-V, 1-A, 28-mΩ On-Resistance Load Switch with Controlled Rise Time

1 Features

- Integrated P-Channel Load Switch
- Input Voltage: 1 V to 3.6 V
- 1 A Maximum Continuous Switch Current
- On-Resistance (Typical Values)
  - R_{ON} = 28 mΩ at V_{IN} = 3.6 V
  - R_{ON} = 33 mΩ at V_{IN} = 2.5 V
  - R_{ON} = 42 mΩ at V_{IN} = 1.8 V
  - R_{ON} = 70 mΩ at V_{IN} = 1.2 V
- Maximum Quiescent Current = 1 µA
- Maximum Shutdown Current = 1 µA
- Low Control Input Thresholds Enable Use of 1.2-V, 1.8-V, 2.5-V, and 3.3-V Logic
- Controlled Slew Rate to Avoid Inrush Currents
  - t_R = 105 µs at V_{IN} = 3.6V
- Four Terminal Wafer-Chip-Scale Package (WCSP)
  - Nominal Dimensions - See Addendum for Details
  - 0.9 mm × 0.9 mm, 0.5-mm Pitch, 0.6-mm Height
- Quick Output Discharge (QOD)

2 Applications

- Battery Powered Equipment
- Portable Industrial Equipment
- Portable Medical Equipment
- Portable Media Players
- Point of Sale Terminal
- GPS Devices
- Digital Cameras
- Portable Instrumentation
- Smartphones and Tablets

3 Description

The TPS22908 is a small, low R_{ON} load switch with controlled turn on. The device contains a P-channel MOSFET that operates over an input voltage range of 1 V to 3.6 V. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals.

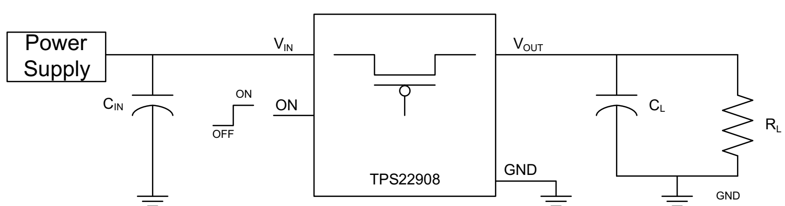
The TPS22908 is available in a space-saving 4-terminal WCSP with 0.5 mm pitch (YZT). The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22908	DSBGA (4)	0.9mm x 0.9mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2013) to Revision C — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision A (August 2012) to Revision B — **Page**

- Updated FEATURES. 1
- Added Layout graphic. 16

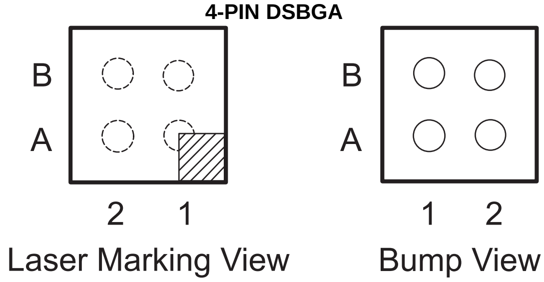
5 Device Options

FEATURE	VALUE
Device	TPS22908
R_{ON} (Typical) VIN = 3.6 V	28 mΩ
Rise Time (Typical) VIN = 3.6 V	105 µs
Quick Output Discharge(1)	Yes
Maximum Current	1 A
Enable	Active high

(1) This feature discharges the output of the switch to ground through an 80-Ω resistor, preventing the output from floating.

6 Pin Configuration and Functions

YZT PACKAGE
4-PIN DSBGA



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	V_{OUT}	O	Switch Output
A2	V_{IN}	I	Switch input, bypass capacitor recommended for minimizing V_{IN} dip. See *Application Information*.
B1	GND	—	Ground
B2	ON	I	Switch control input, active high. Do not leave floating.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT(2)
V_{IN}	Supply voltage	–0.3	4	V
V_{OUT}	Output voltage	–0.3	(V_{IN} + 0.3)	V
V_{ON}	Input voltage	–0.3	4	V
I_{MAX}	Maximum Continuous Switch Current for $V_{IN} \geq 1.2$ V		1	A
	Maximum Continuous Switch Current at V_{IN} = 1 V		0.6	
T_J	Maximum junction temperature(3)		125	°C
T_{LEAD}	Maximum lead temperature (10-s soldering time)		300	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [TA(max)] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A(max)} = T_{J(max)} – (R_{\theta JA} \times P_{D(max)})$

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage	1	3.6	V
V_{ON}	ON voltage	0	3.6	V
V_{OUT}	Output voltage	0	V_{IN}	V
V_{IH}	High-level input voltage, ON	0.85	3.6	V
V_{IL}	Low-level input voltage, ON	0	0.4	V
T_A	Operating free-air temperature range	-40	85	°C
C_{IN}	Input capacitor	1(1)		µF

(1) Refer to application section.

7.4 Thermal Information

THERMAL METRIC(1)		TPS22908 YZT (DSBGA) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	188	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	2	
$R_{\theta JB}$	Junction-to-board thermal resistance	33	
ψ_{JT}	Junction-to-top characterization parameter	9.1	
ψ_{JB}	Junction-to-board characterization parameter	33	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Unless otherwise noted the specification applies over the operating ambient temp –40°C ≤ T_A ≤ 85°C. Typical values are for V_{IN} = 3.6 V, and T_A = 25°C unless otherwise noted.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
I_{IN}	Quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON}		Full		0.19	1	µA
$I_{IN(OFF)}$	OFF-state supply current	V_{ON} = 0 V, V_{OUT} = Open		Full		0.12	1	µA
$I_{IN(LEAK)}$	OFF-state supply current	V_{ON} = 0 V, V_{OUT} = 0 V		Full		0.12	1	µA
I_{ON}	ON pin input leakage current	V_{ON} = 1.1 V to 3.6 V		Full		0.01	0.1	µA
RESISTANCE AND SWITCH CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA	V_{IN} = 3.6 V	25°C		28.2	32.1	mΩ
				Full			34.9	
			V_{IN} = 2.5 V	25°C		33.1	37.5	mΩ
				Full			40.6	
			V_{IN} = 1.8 V	25°C		41.5	50.3	mΩ
				Full			54.0	
			V_{IN} = 1.2 V	25°C		69.7	87.3	mΩ
				Full			91.2	
			V_{IN} = 1.0 V	25°C		112	155	mΩ
				Full			156	
R_{PD}	Output pulldown resistance	V_{IN} = 3.3 V, V_{ON} = 0 V, I_{OUT} = 30 mA		25°C		80	100	Ω

7.6 Switching Characteristics

PARAMETER		TEST CONDITION	TPS22908			UNIT
			MIN	TYP	MAX	
V_{IN} = 3.6 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF		110		µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF		5		µs
t_R	V_{OUT} Rise time	R_L = 10 Ω, C_L = 0.1 µF		105		µs
t_F	V_{OUT} Fall time	R_L = 10 Ω, C_L = 0.1 µF		2		µs
V_{IN} = 1.0 V, T_A = 25°C (unless otherwise noted)						
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF		493		µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF		7		µs
t_R	V_{OUT} Rise time	R_L = 10 Ω, C_L = 0.1 µF		442		µs
t_F	V_{OUT} Fall time	R_L = 10 Ω, C_L = 0.1 µF		2		µs

7.7 Typical Characteristics

7.7.1 Typical DC Characteristics

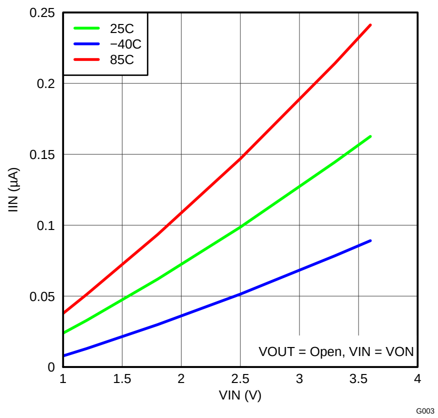


Figure 1. V_{IN} vs. Quiescent Current (I_{IN})

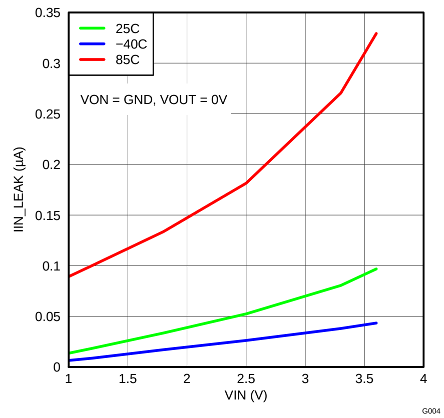


Figure 2. V_{IN} vs. $I_{IN(LEAK)}$

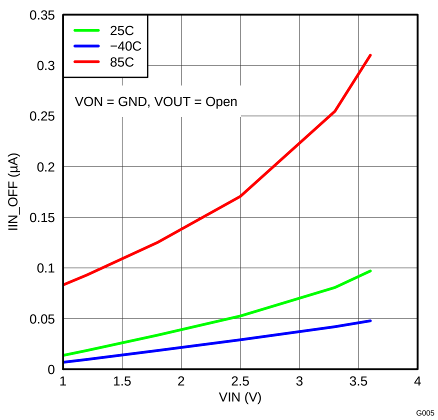


Figure 3. V_{IN} vs. $I_{IN(OFF)}$

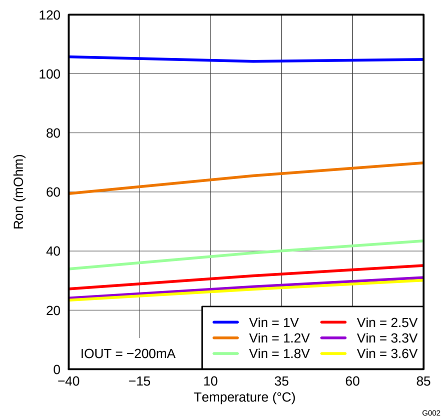


Figure 4. Temperature vs. R_{ON}

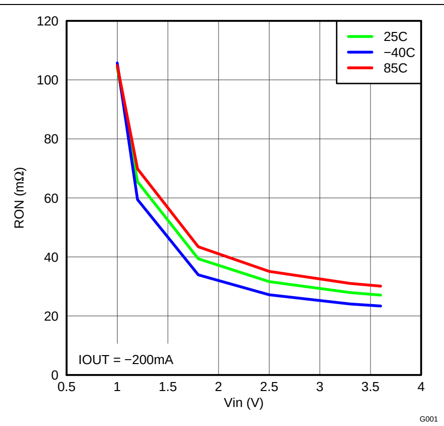


Figure 5. V_{IN} vs. R_{ON}

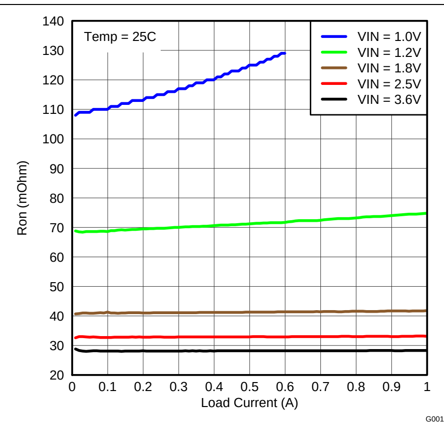


Figure 6. R_{ON} vs. Load Current (Various V_{IN} at T_A = 25°C)

Typical DC Characteristics (continued)

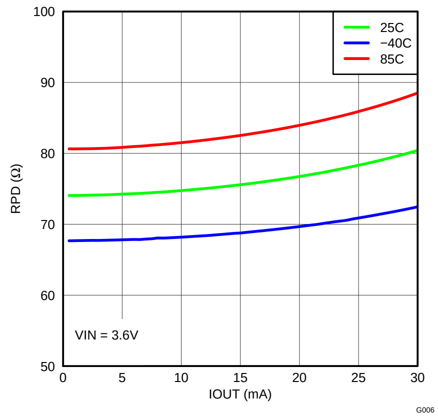


Figure 7. I_{OUT} vs. R_{PD}

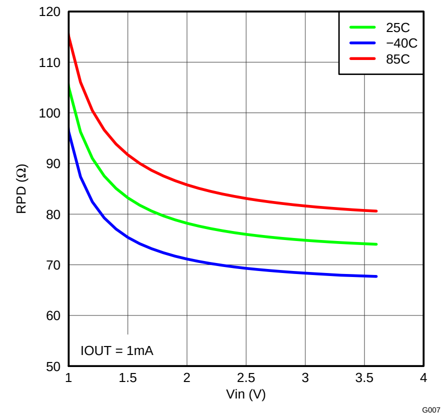


Figure 8. V_{IN} vs. R_{PD}

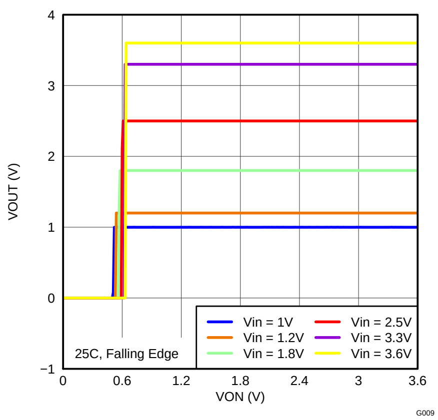


Figure 9. V_{ON} Threshold vs. V_{OUT} (ON pin Voltage Decreasing)

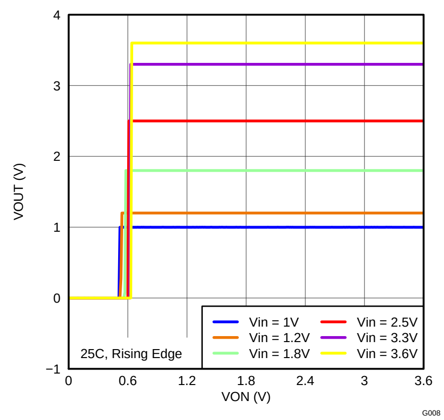


Figure 10. V_{ON} Threshold vs. V_{OUT} (ON Pin Voltage Increasing)

7.7.2 Typical Switching Characteristics

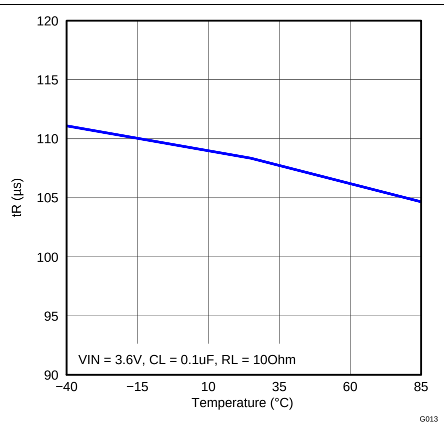


Figure 11. Rise Time vs. Temperature (V_{IN} = 3.6 V)

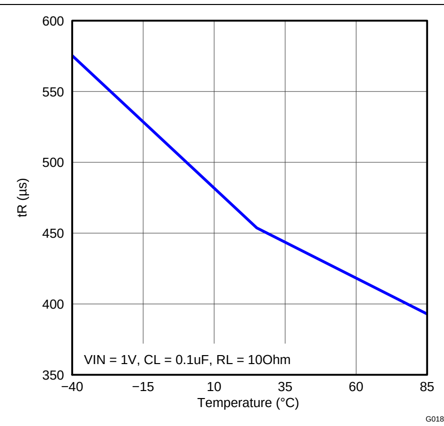


Figure 12. Rise Time vs. Temperature (V_{IN} = 1 V)

Typical Switching Characteristics (continued)

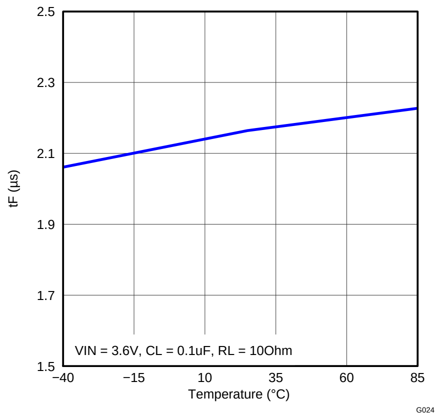


Figure 13. Fall Time vs. Temperature (V_{IN} = 3.6 V)

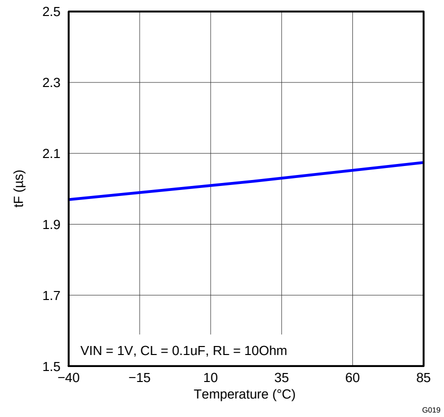


Figure 14. Fall Time vs. Temperature (V_{IN} = 1 V)

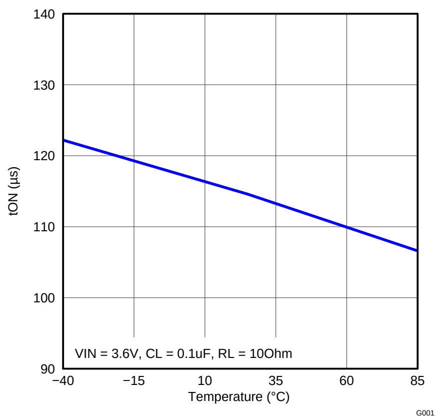


Figure 15. Turnon Time vs. Temperature (V_{IN} = 3.6 V)

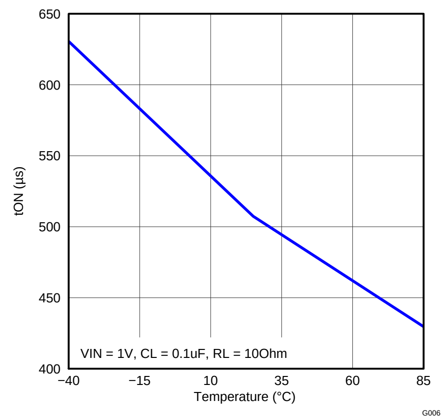


Figure 16. Turnon Time vs. Temperature (V_{IN} = 1 V)

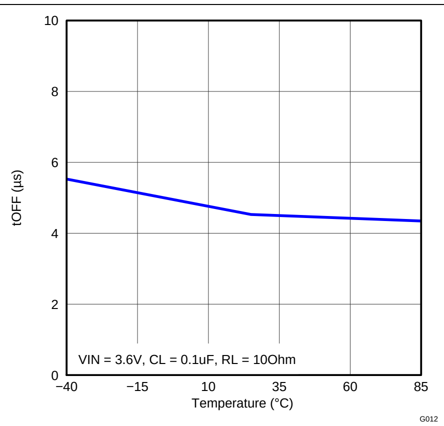


Figure 17. Turnoff Time vs. Temperature (V_{IN} = 3.6 V)

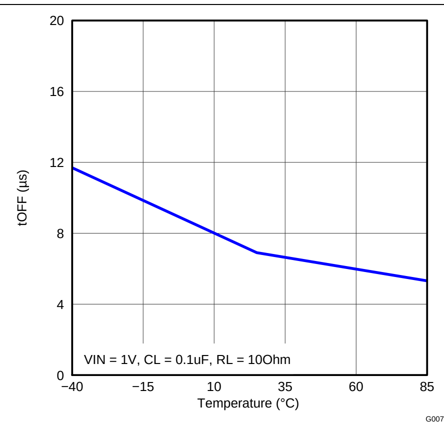


Figure 18. Turnoff Time vs. Temperature (V_{IN} = 1 V)

Typical Switching Characteristics (continued)

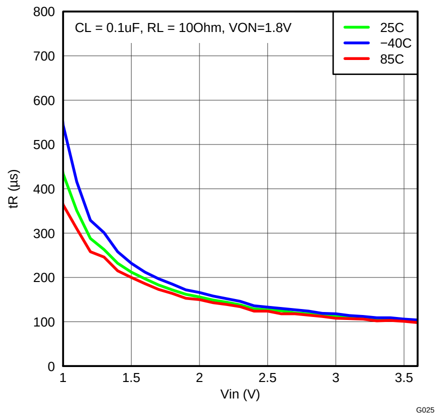


Figure 19. Rise Time vs. V_{IN} (C_L = 0.1 µF)

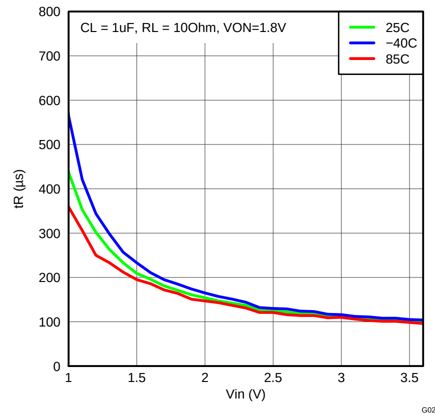


Figure 20. Rise Time vs. V_{IN} (C_L = 1 µF)

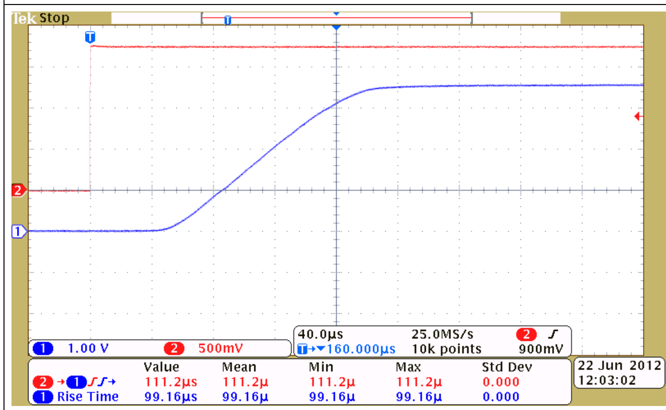


Figure 21. Turn on Response Time (V_{IN} = 3.6 V, C_{IN} = 10 µF, C_L = 1 µF, R_L = 10 Ω)

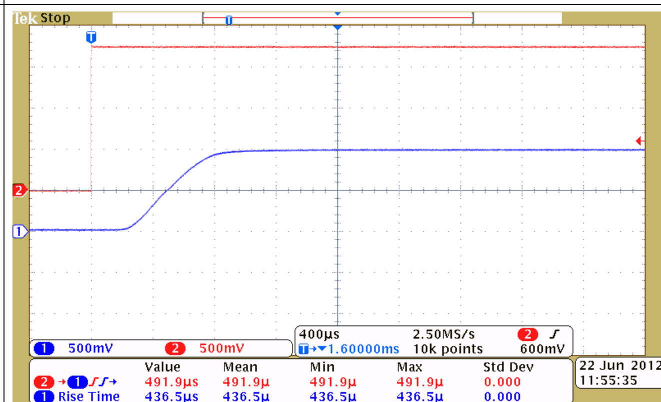


Figure 22. Turn on Response Time (V_{IN} = 1 V, C_{IN} = 10 µF, C_L = 1 µF, R_L = 10 Ω)

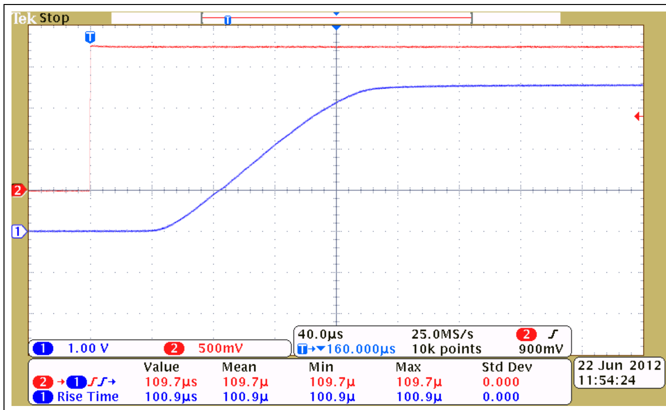


Figure 23. Turn on Response Time (V_{IN} = 3.6 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

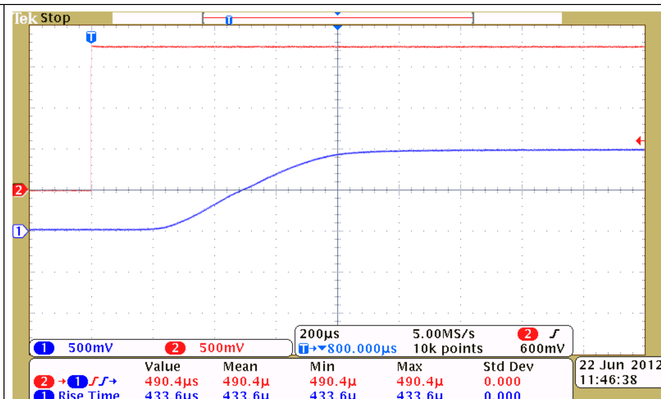


Figure 24. Turn on Response Time (V_{IN} = 1 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

Typical Switching Characteristics (continued)

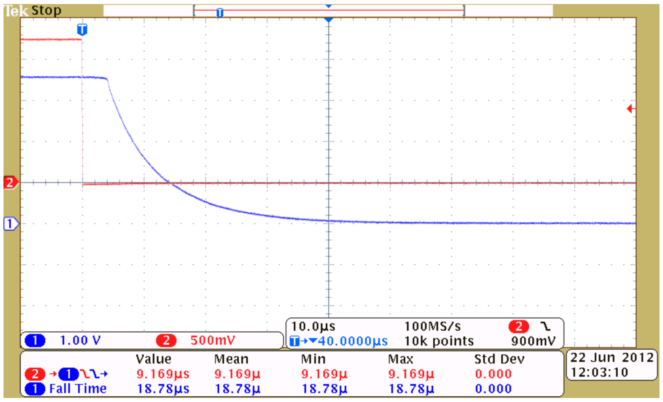


Figure 25. Turn off Response Time (V_{IN} = 3.6 V, C_{IN} = 10 µF, C_L = 1 µF, R_L = 10 Ω)

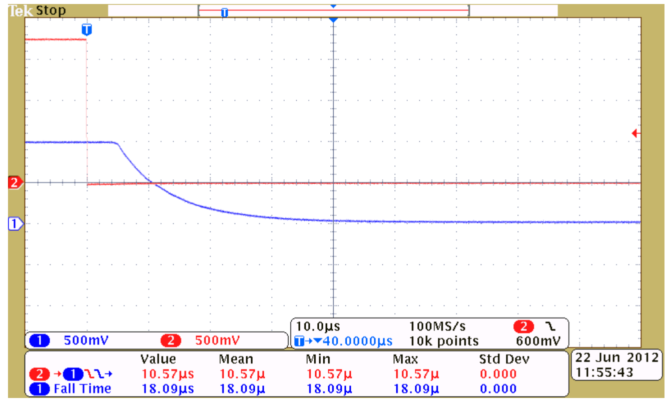


Figure 26. Turn off Response Time (V_{IN} = 1 V, C_{IN} = 10 µF, C_L = 1 µF, R_L = 10 Ω)

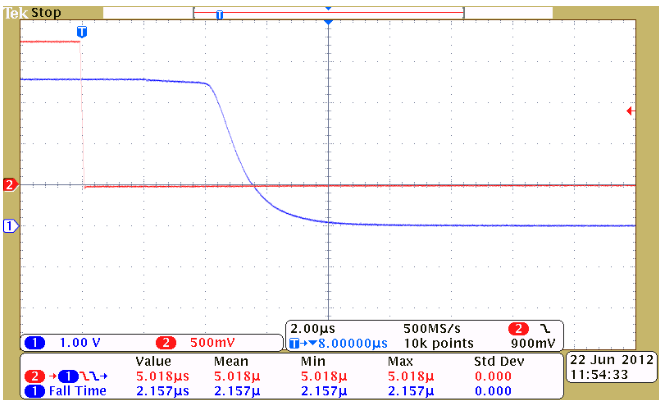


Figure 27. Turn off Response Time (V_{IN} = 3.6 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

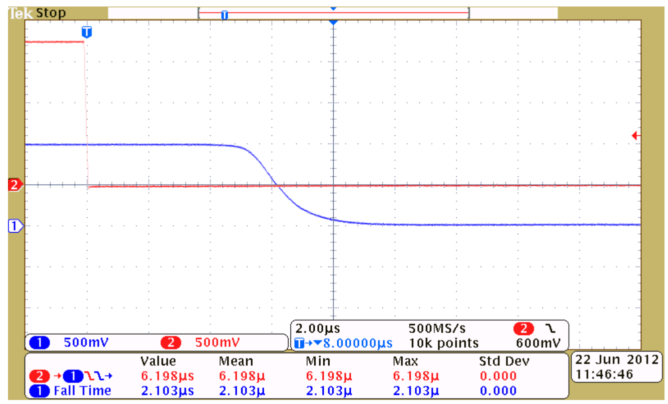
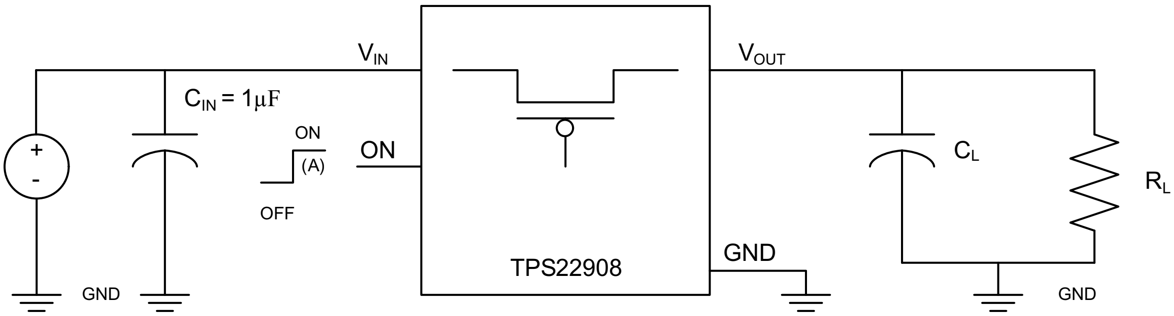
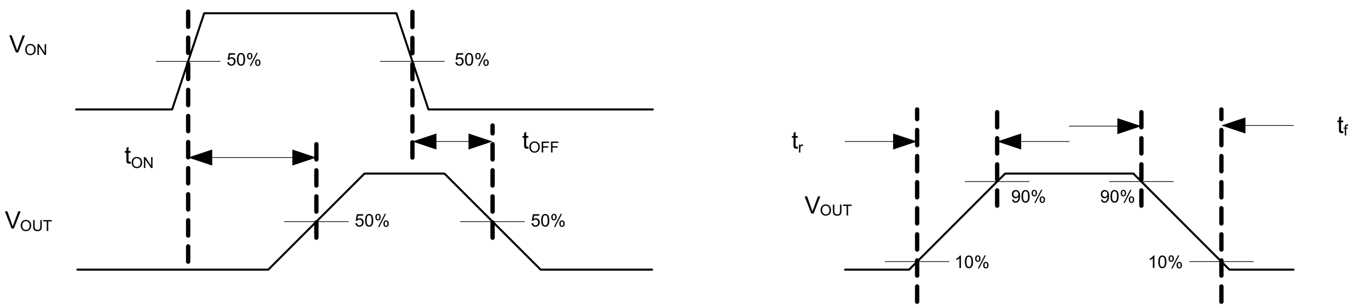


Figure 28. Turn off Response Time (V_{IN} = 1 V, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω)

8 Parameter Measurement Information



TEST CIRCUIT



t_{ON}/t_{OFF} WAVEFORMS

A. Rise and fall times of the control signal is 100 ns.

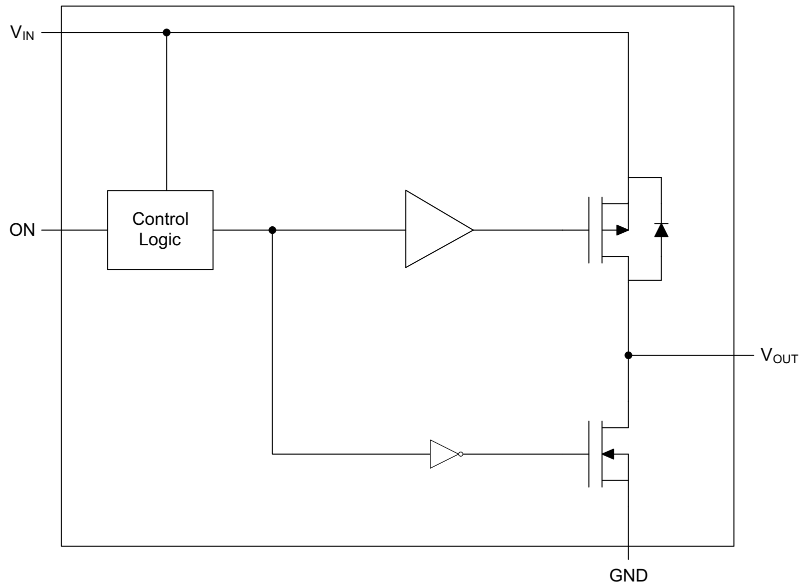
Figure 29. Test Circuit and t_{ON}/t_{OFF} Waveforms

9 Detailed Description

9.1 Overview

The TPS22908 is a single channel, 1 A load switch in a small, space-saving DSBGA-4 package. This device implements a P-channel MOSFET to provide a low on-resistance for a low voltage drop across the device. A controlled rise time is used in applications to limit the inrush current.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 ON/OFF Control

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state. ON is active high and has a low threshold making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold, and it can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs.

9.3.2 Quick Output Discharge

The TPS22908 includes the Quick Output Discharge (QOD) feature. When the switch is disabled, a discharge resistance with a typical value of 80 Ω is connected between the output and ground. This resistance pulls down the output and prevents it from floating when the device is disabled.

9.4 Device Functional Modes

Table 1. Functional Table

ON	V_{IN} to V_{OUT}	V_{OUT} to GND
L	OFF	ON
H	ON	OFF

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor can be placed between V_{IN} and GND. A 1 µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

10.1.2 Output Capacitor (Optional)

Due to the integrated body diode of the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of at least 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip at turn on due to inrush currents.

10.2 Typical Application

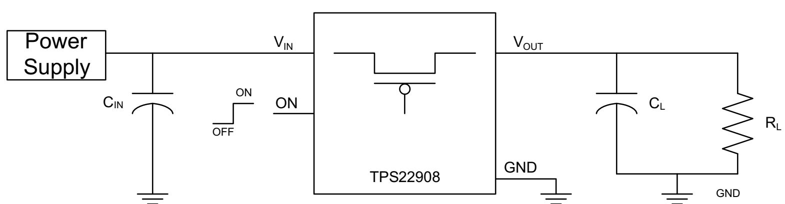


Figure 30. Typical Application Schematic

10.2.1 Design Requirements

The following input parameters will be used in these design examples.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.8 V
C_L	10 µF
Load current	500 mA
Ambient Temperature	25 °C
Maximum inrush current	200 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Managing Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (1.8 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using Equation 1:

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt}$$

where:

- C_L = Output capacitance
- dV_{OUT} = Output voltage
- dt = Rise time (1)

The TPS22908 offers a controlled rise time for minimizing inrush current. This device can be selected based upon the minimum acceptable rise time which can be calculated using the design requirements and the inrush current equation. An output capacitance of 4.7 µF will be used since the amount of inrush current increases with output capacitance:

200 mA = 10 µF × 1.8V / dt

dt = 90 µs (2)

To ensure an inrush current of less than 200 mA, a device with a rise time greater than 90 µs must be used. The TPS22908 has a typical rise time of 160 µs at 1.8 V which meets the above design requirements.

10.2.2.2 VIN to VOUT Voltage Drop

The voltage drop from VIN to VOUT is determined by the ON-resistance of the device and the load current. R_{ON} can be found in *Electrical Characteristics* and is dependent on temperature. When the value of R_{ON} is found, the following equation can be used to calculate the voltage drop across the device:

$\Delta V = I_{LOAD} \times R_{ON}$

where:

- ΔV = Voltage drop across the device
- I_{LOAD} = Load current
- R_{ON} = ON-resistance of the device (3)

At V_{IN} = 1.8 V, the TPS22908 has an R_{ON} value of 42 mΩ. Using this value and the defined load current, the above equation can be evaluated:

ΔV = 500 mA × 42 mΩ

ΔV = 21 mV (4)

Therefore, the voltage drop across the device will be 21 mV.

10.2.3 Application Curve

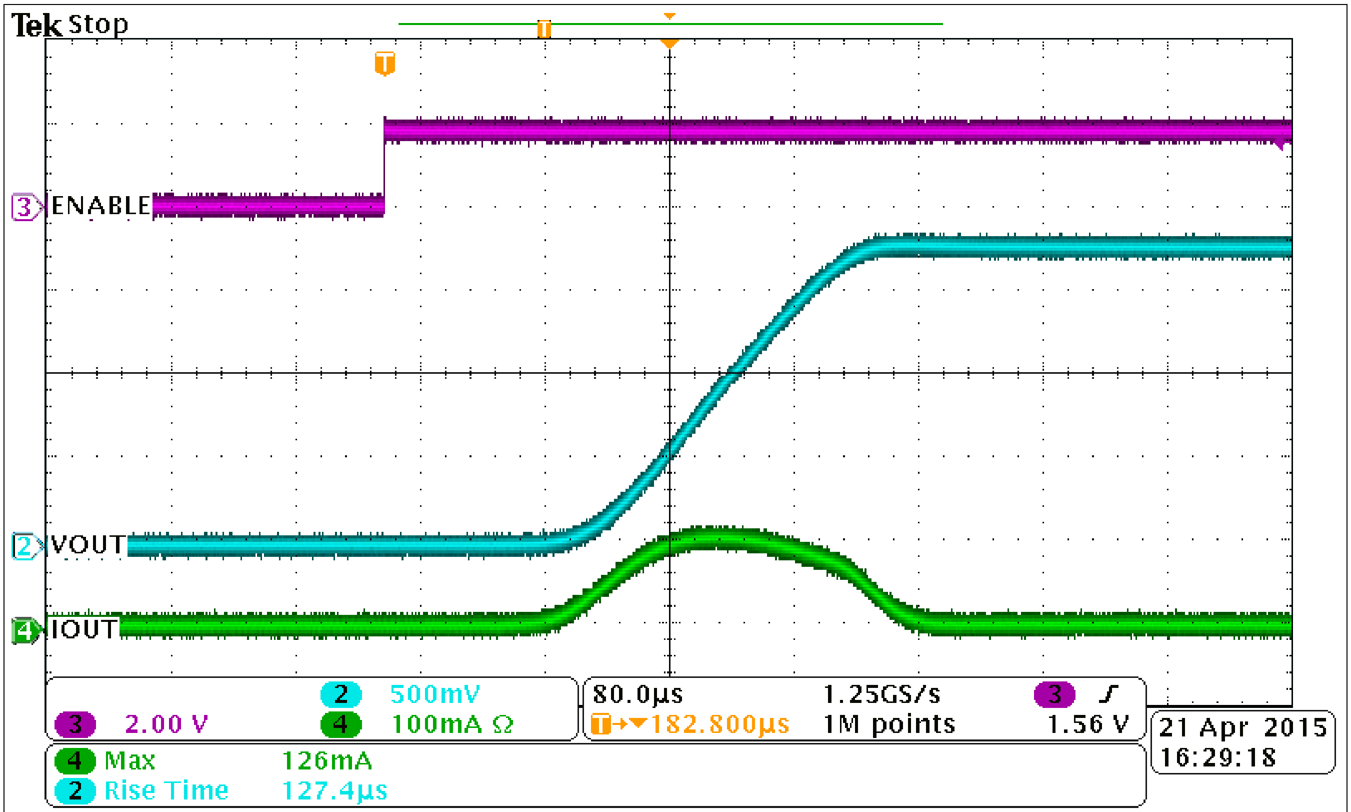


Figure 31. Inrush Current with a Load Capacitance of 10µF (V_{IN} = 1.8 V, T_A = 25°C)

11 Power Supply Recommendations

The device is designed to operate with a VIN range of 1 V to 3.6 V. This supply must be well regulated and placed as close to the device terminals as possible. It must also be able to withstand all transient and load currents, using a recommended input capacitance of 1 µF if necessary. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient.

12 Layout

12.1 Layout Guidelines

For best performance, VIN, VOUT, and GND traces should be as short and wide as possible to help minimize the parasitic electrical effects. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation.

12.2 Layout Example

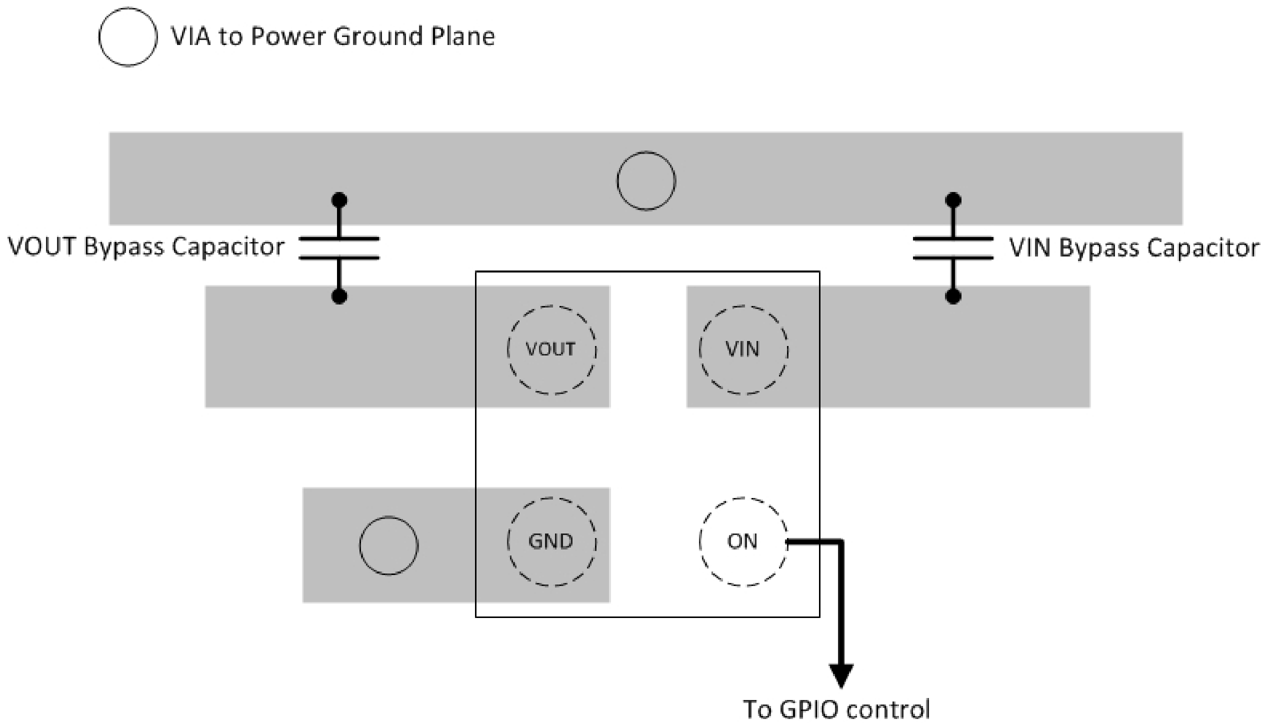


Figure 32. Layout Example

12.3 Thermal Considerations

For higher reliability, the maximum IC junction temperature, $T_{J(max)}$, should be restricted to 125˚C under normal operating conditions. Junction temperature is directly proportional to power dissipation in the device and the two are related by:

$$T_J = T_A + R_{\theta JA} \times P_D \quad (5)$$

where:

- T_J = Junction temperature of the device
- T_A = Ambient temperature
- P_D = Power dissipation inside the device
- $R_{\theta JA}$ = Junction to ambient thermal resistance. See *Thermal Information* for more information. This parameter is highly dependent on board layout.

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22908YZTR	ACTIVE	DSBGA	YZT	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AT	Samples
TPS22908YZTT	ACTIVE	DSBGA	YZT	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(AT ~ ATF)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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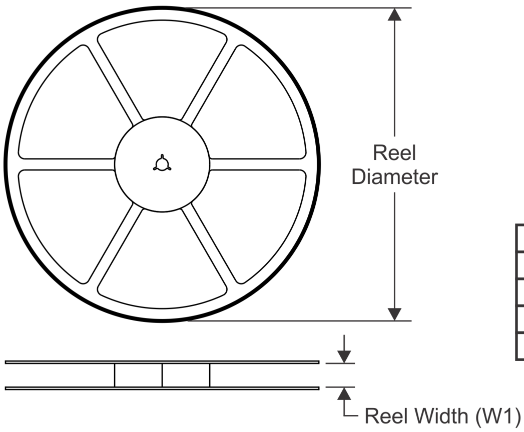
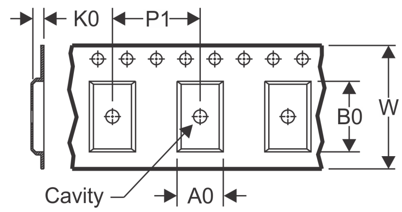
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

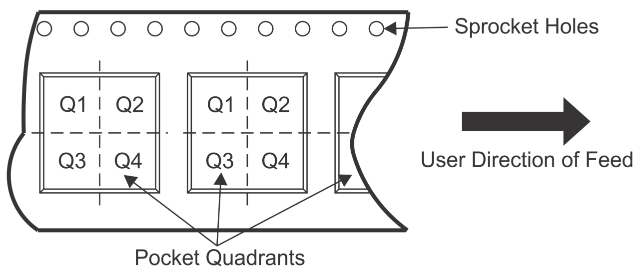


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

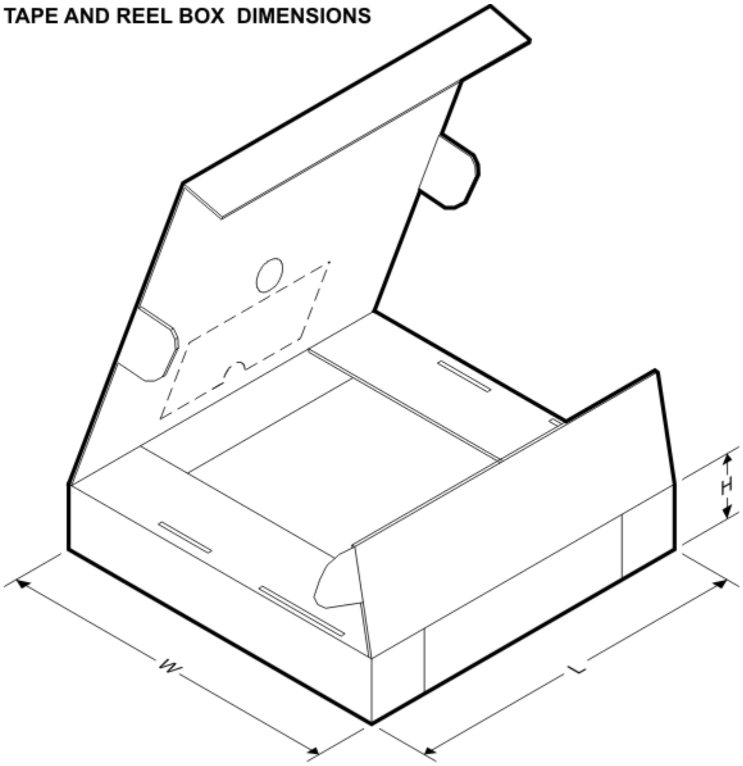
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

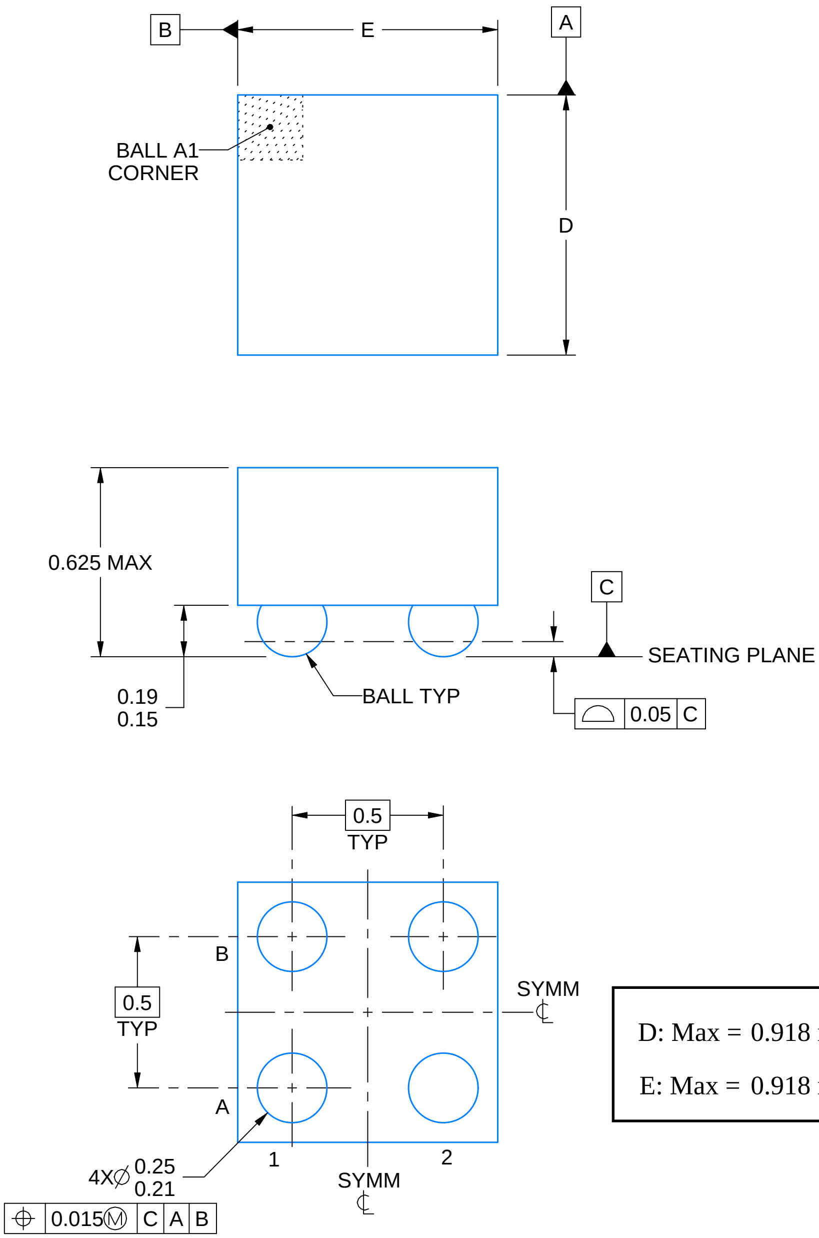
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22908YZTR	DSBGA	YZT	4	3000	180.0	8.4	0.99	0.99	0.69	4.0	8.0	Q1
TPS22908YZTR	DSBGA	YZT	4	3000	178.0	9.2	1.0	1.0	0.73	4.0	8.0	Q1
TPS22908YZTT	DSBGA	YZT	4	250	180.0	8.4	0.99	0.99	0.69	4.0	8.0	Q1
TPS22908YZTT	DSBGA	YZT	4	250	178.0	9.2	1.0	1.0	0.73	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22908YZTR	DSBGA	YZT	4	3000	182.0	182.0	20.0
TPS22908YZTR	DSBGA	YZT	4	3000	220.0	220.0	35.0
TPS22908YZTT	DSBGA	YZT	4	250	182.0	182.0	20.0
TPS22908YZTT	DSBGA	YZT	4	250	220.0	220.0	35.0



D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

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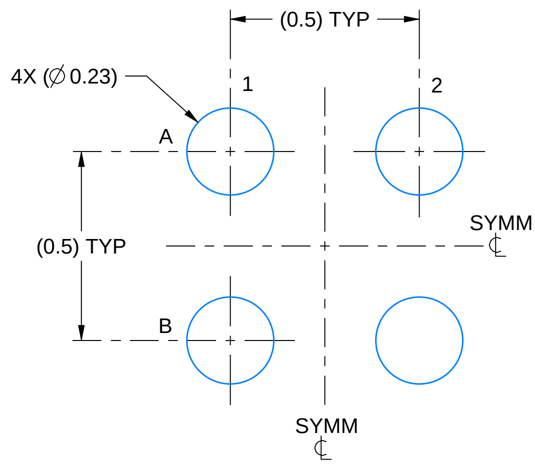
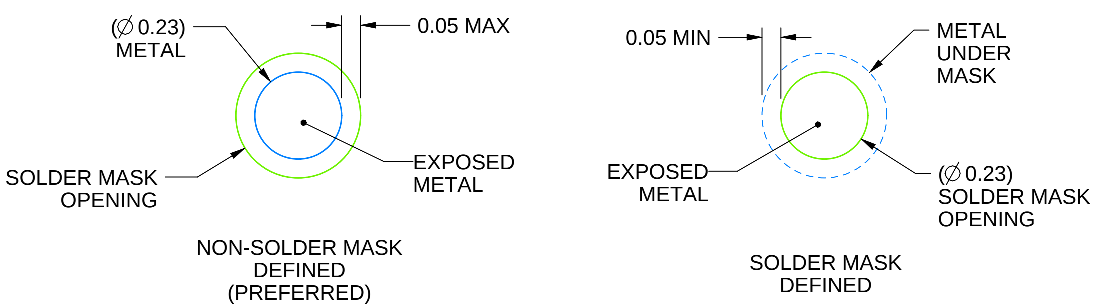
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

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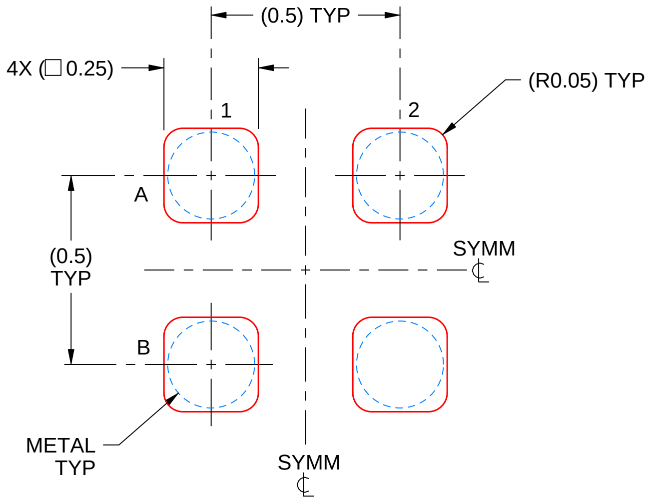
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.