

FDS8817NZ

N-Channel PowerTrench® MOSFET 30V, 15A, 7.0mΩ

Features

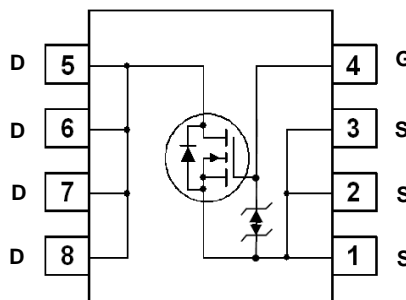
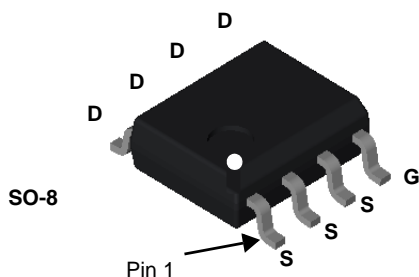
- Max $r_{DS(on)}$ = 7mΩ at V_{GS} = 10V, I_D = 15A
- Max $r_{DS(on)}$ = 10mΩ at V_{GS} = 4.5V, I_D = 12.6A
- HBM ESD protection level of 3.8kV typical (note 3)
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability
- RoHS compliant



General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|----------------|--|-------------|------------------|
| V_{DS} | Drain to Source Voltage | 30 | V |
| V_{GS} | Gate to Source Voltage | ± 20 | V |
| I_D | Drain Current -Continuous | 15 | A |
| | -Pulsed | 60 | |
| E_{AS} | Single Pulse Avalanche Energy | 181 | mJ |
| P_D | Power Dissipation | 2.5 | W |
| | Power Dissipation | 1.0 | |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | $^\circ\text{C}$ |

Thermal Characteristics

| | | | | |
|-----------------|---|-----------|-----|--------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | (Note 1) | 25 | $^\circ\text{C/W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1a) | 50 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1b) | 125 | |

Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape Width | Quantity |
|----------------|-----------|-----------|------------|------------|
| FDS8817NZ | FDS8817NZ | 13" | 12mm | 2500 units |

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | |
|--------------------------------------|---|---|----|----|----------|----------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\mu\text{A}$, referenced to 25°C | | 20 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 24\text{V}$, $V_{GS} = 0\text{V}$ | | | 1 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$ | | | ± 10 | μA |

On Characteristics (Note 2)

| | | | | | | |
|--|--|--|---|-----|----|----------------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ | 1 | 1.8 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250\mu\text{A}$, referenced to 25°C | | -6 | | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS} = 10\text{V}$, $I_D = 15\text{A}$ | | 5.4 | 7 | m Ω |
| | | $V_{GS} = 4.5\text{V}$, $I_D = 12.6\text{A}$ | | 7.0 | 10 | |
| | | $V_{GS} = 10\text{V}$, $I_D = 15\text{A}$, $T_J = 125^\circ\text{C}$ | | 7.5 | 11 | |
| g_{FS} | Forward Transconductance | $V_{DS} = 5\text{V}$, $I_D = 15\text{A}$ | | 54 | | S |

Dynamic Characteristics

| | | | | | | |
|-----------|------------------------------|---|--|------|------|----------|
| C_{iss} | Input Capacitance | $V_{DS} = 15\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ | | 1805 | 2400 | pF |
| C_{oss} | Output Capacitance | | | 335 | 445 | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 200 | 300 | pF |
| R_g | Gate Resistance | $f = 1\text{MHz}$ | | 1.4 | | Ω |

Switching Characteristics

| | | | | | | |
|--------------|-------------------------------|---|---|----|----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 15\text{V}$, $I_D = 15\text{A}$ $V_{GS} = 10\text{V}$, $R_{GEN} = 6\Omega$ | | 11 | 22 | ns |
| t_r | Rise Time | | | 13 | 26 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 25 | 40 | ns |
| t_f | Fall Time | | | 7 | 14 | ns |
| Q_g | Total Gate Charge | $V_{GS} = 0\text{V}$ to 10V | $V_{DD} = 15\text{V}$ $I_D = 15\text{A}$ | 32 | 45 | nC |
| Q_g | Total Gate Charge | $V_{GS} = 0\text{V}$ to 5V | | 17 | 24 | nC |
| Q_{gs} | Gate to Source Charge | | | 6 | | nC |
| Q_{gd} | Gate to Drain "Miller" Charge | | | 7 | | nC |

Drain-Source Diode Characteristics

| | | | | | | |
|----------|---------------------------------------|--|--|-----|-----|----|
| V_{SD} | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{V}$, $I_S = 2.1\text{A}$ (Note 2) | | 0.8 | 1.2 | V |
| t_{rr} | Reverse Recovery Time | $I_F = 15\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$ | | 24 | 36 | ns |
| Q_{rr} | Reverse Recovery Charge | | | 15 | 23 | nC |

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) $50^\circ\text{C}/\text{W}$ when mounted on a 1in^2 pad of 2 oz copper.



b) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

- Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty Cycle $< 2\%$.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
- Starting $T_J = 25^\circ\text{C}$, $L = 3\text{mH}$, $I_{AS} = 11\text{A}$, $V_{DD} = 30\text{V}$, $V_{GS} = 10\text{V}$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

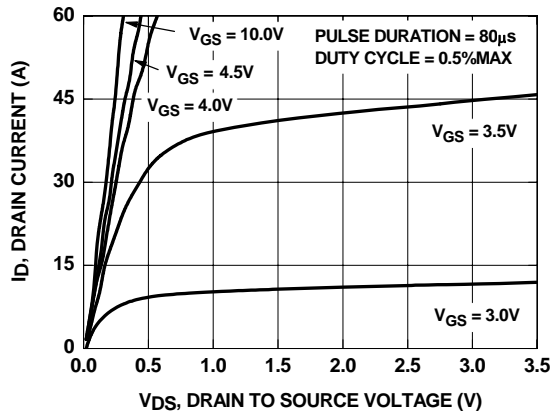


Figure 1. On-Region Characteristics

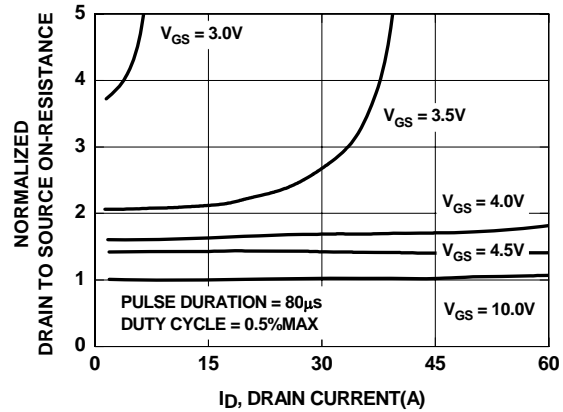


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

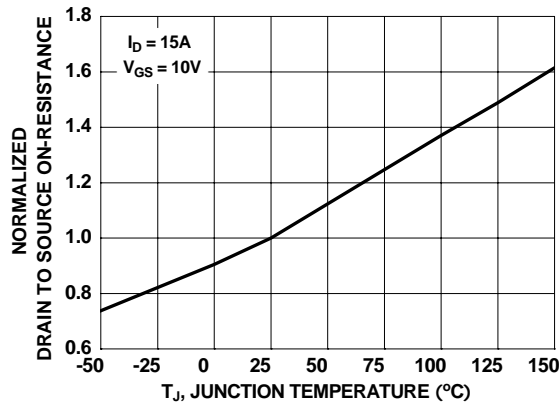


Figure 3. Normalized On-Resistance vs Junction Temperature

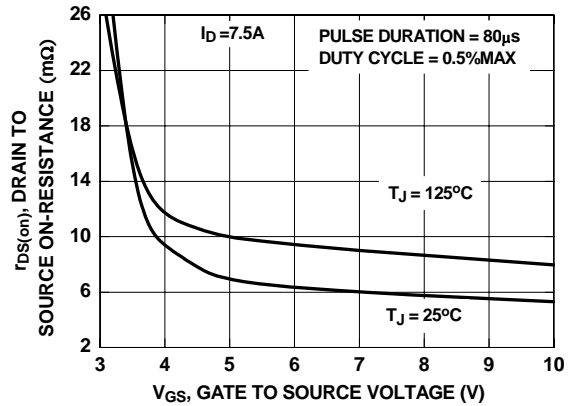


Figure 4. On-Resistance vs Gate to Source Voltage

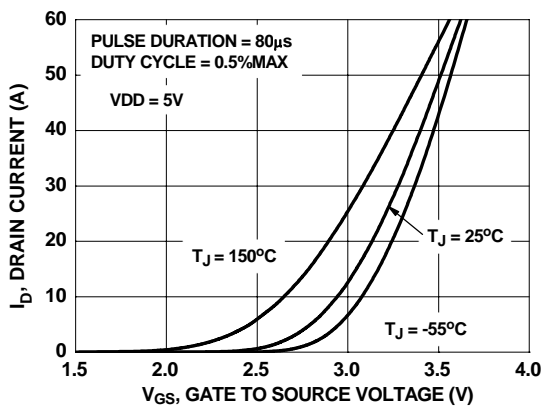


Figure 5. Transfer Characteristics

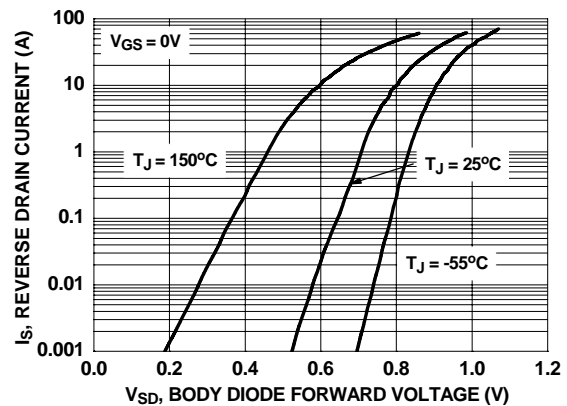


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

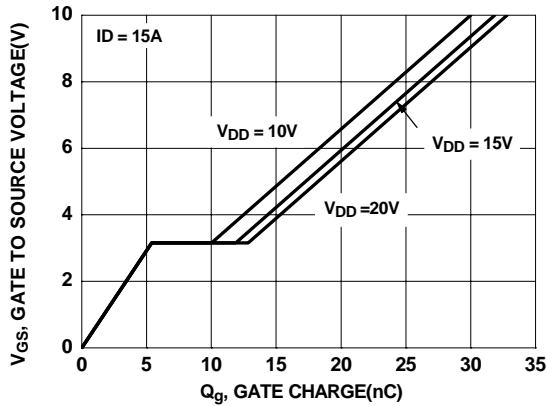


Figure 7. Gate Charge Characteristics

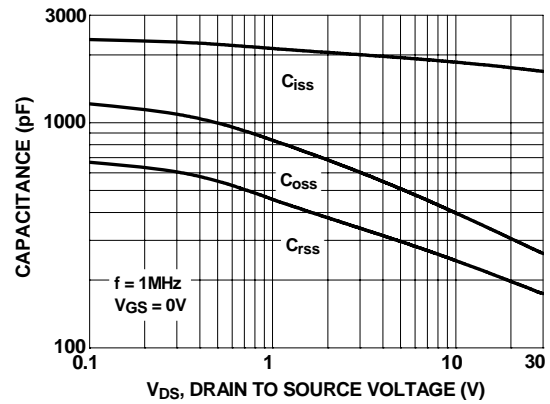


Figure 8. Capacitance vs Drain to Source Voltage

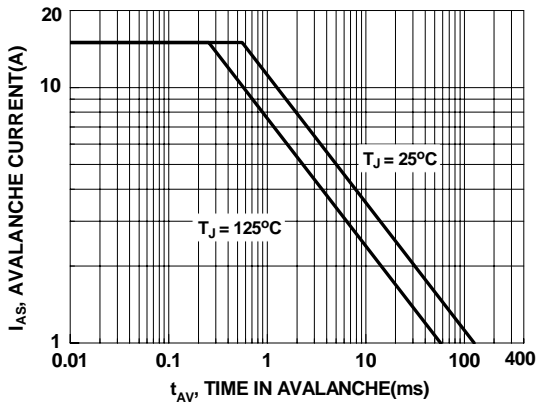


Figure 9. Unclamped Inductive Switching Capability

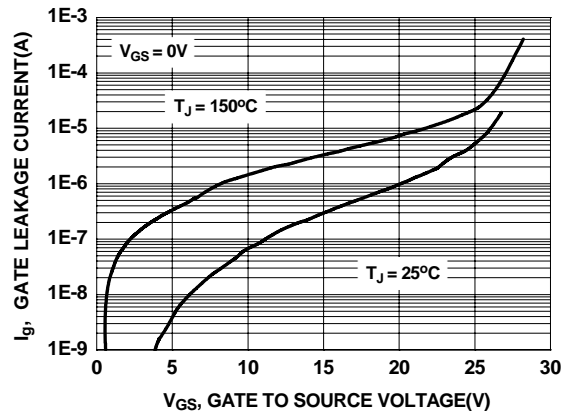


Figure 10. Gate Leakage Current vs Gate to Source Voltage

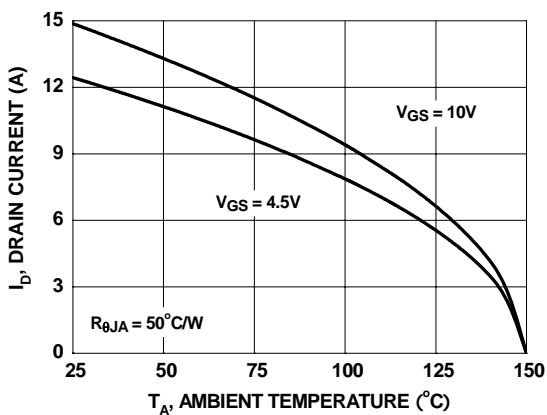


Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

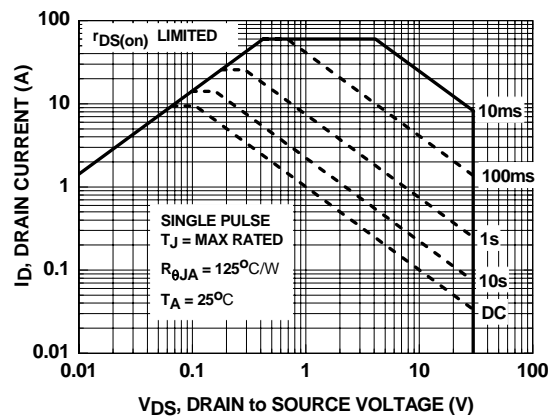


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

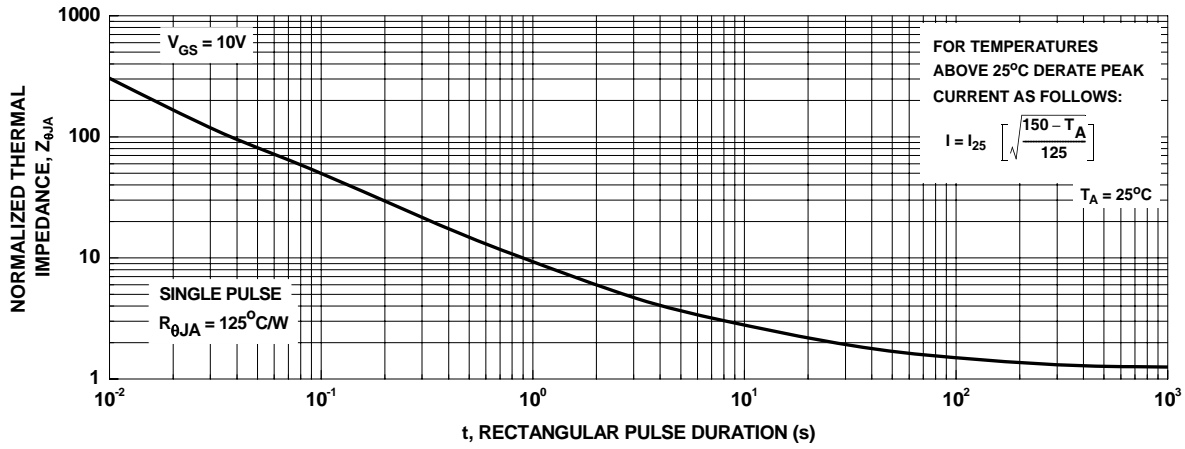


Figure 13. Single Pulse Maximum Power Dissipation

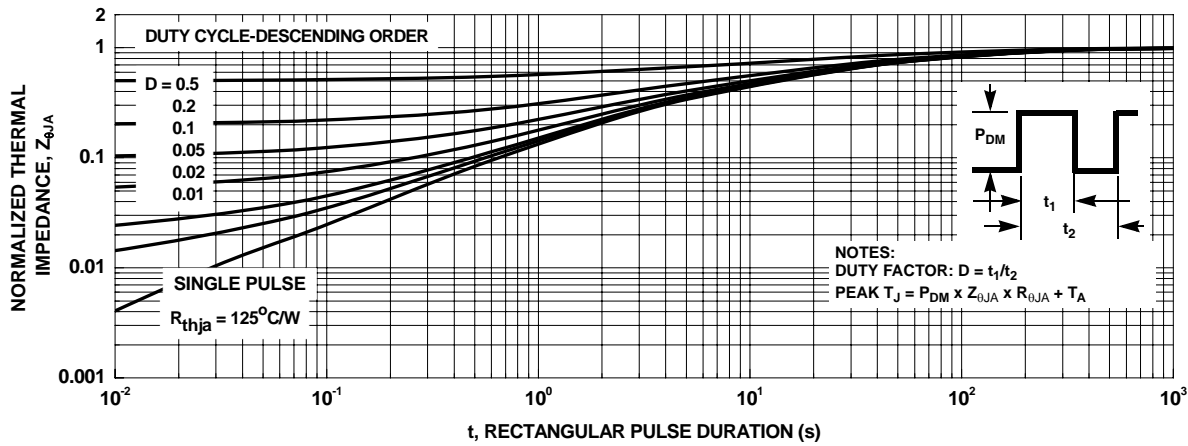



Figure 14. Transient Thermal Response Curve



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