Micro Linear

ML2271

µP Compatible High-Speed 10-Bit A/D Converter with S/H

GENERAL DESCRIPTION

The ML2271 is a high speed, µP compatible 10-bit A/D converter. A three step flash technique is used to achieve a conversion time of 1.65µs.* The ML2271 operates from a single 5V supply and has an analog input range from GND to V_{CC}.

The ML2271 has a true internal sample and hold and can digitize sinusoid signals as high as 150kHz without conversion errors.

The ML2271 digital interface has been designed so that the device appears as a memory location or I/O port to a µP, eliminating the need for external interfacing logic. The data outputs are latched and have three state control, allowing direct connection to a µP bus or I/O port. The addition of an internal timing generator also allows the device to easily operate in stand alone applications.

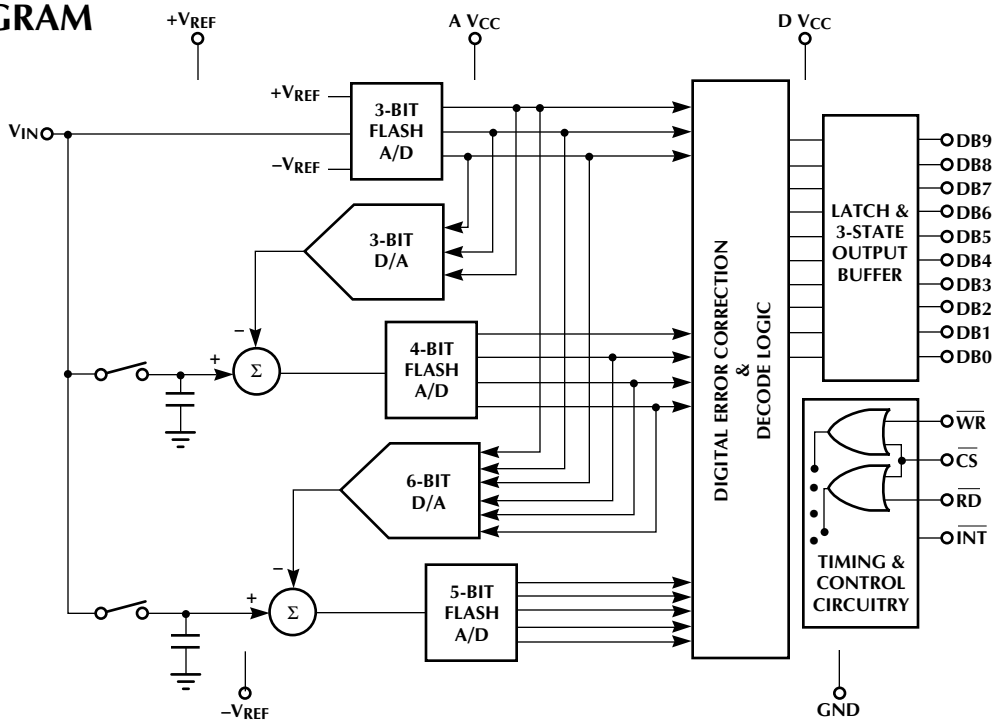
The ML2271 is pin and function compatible with the ADC1061.

* For higher speed and higher accuracy versions, contact the factory

FEATURES

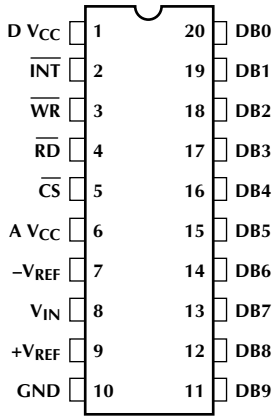
- Conversion time over temperature and supply voltage tolerance 1.8µs*
- Linearity error ±1LSB*
- Full scale error ±1LSB*
- Zero error ±1LSB*
- Capable of digitizing a 5V, 150kHz sine wave
- No missing codes
- 0V to 5V analog input range with single 5V power supply
- Analog input protection — 25mA min
- Operates ratiometrically or with up to 5V voltage reference
- No external clock required
- Easy interface to µP, or operates stand-alone
- Latched, 3-state data outputs
- Power-on reset circuitry
- Low power — 175mW max
- Standard 20-pin DIP or surface mount SOIC
- 0°C to 70°C, –40°C to +85°C operating temperature range

BLOCK DIAGRAM



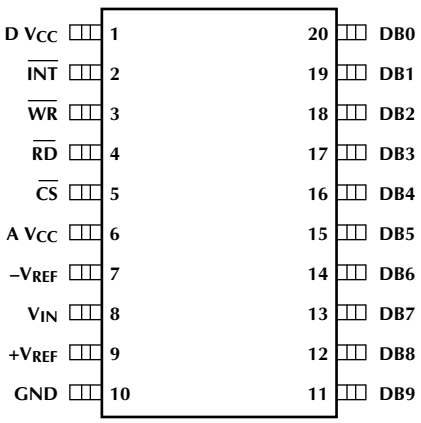
PIN CONFIGURATION

20-Pin DIP



TOP VIEW

20-Pin SOIC



TOP VIEW

PIN DESCRIPTION

PIN#	NAME	FUNCTION
1	D V_{CC}	Digital supply. +5V ±5%. Connect to A V_{CC}.
2	$\overline{INT}$	Interrupt output. This output signals the end of a conversion and indicates that data is valid on the data outputs. See Digital Interface section.
3	$\overline{WR}$	Write input. Input which initiates a conversion. See Digital Interface section.
4	$\overline{RD}$	Read input. This input latches data into the output latches. See Digital Interface section.
5	$\overline{CS}$	Chip select input. This input must be held low during $\overline{WR}$ and $\overline{RD}$ for the device to perform a conversion.
6	A V_{CC}	Analog supply. +5V ±5%. Connect to D V_{CC}.
7	$-V_{REF}$	Negative reference input voltage for A/D converter.
8	V_{IN}	Analog input.
9	$+V_{REF}$	Positive reference input voltage for A/D converter.
10	GND	Ground.
11	DB9	Data output — bit 9 (MSB)
12	DB8	Data output — bit 8
13	DB7	Data output — bit 7
14	DB6	Data output — bit 6
15	DB5	Data output — bit 5
16	DB4	Data output — bit 4
17	DB3	Data output — bit 3
18	DB2	Data output — bit 2
19	DB1	Data output — bit 1
20	DB0	Data output — bit 0 (LSB)

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage, A V_{CC}, D V_{CC} 6.5V
Voltage
  Logic Inputs ..... –0.3V to V_{CC} + 0.3V
  Analog Inputs ..... –0.3V to V_{CC} + 0.3
Input Current per Pin (Note 2) ..... ±25mA
Storage Temperature ..... –65°C to +150°C
Package Dissipation
  at T_A = 25°C (Board Mount) 875mW
Lead Temperature (Soldering 10 sec.)
  Dual-In-Line Package (Molded) ..... 260°C
  Molded Small Outline IC Package
    Vapor Phase (60 sec.) ..... 215°C
    Infrared (15 sec.) ..... 220°C

OPERATING CONDITIONS

Temperature Range (Note 3) ..... $T_{MIN} \le T_A \le T_{MAX}$
  ML2271CCS ..... 0°C to +70°C
  ML2271CCP ..... 0°C to +70°C
  ML2271CIS ..... –40°C to +85°C
  ML2271CIP ..... –40°C to +85°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, D V_{CC} = A V_{CC} = $+V_{REF}$ = 5V ±5%, and $–V_{REF}$ = GND

PARAMETER	CONDITIONS	ML2271CCX			ML2271CIX			UNITS
		MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
Converter								
Integral Linearity Error ML2271CXX	V_{REF} = V_{CC} (Notes 5,7)			±1			±1.5	LSB
Differential Linearity Error ML2271CXX	V_{REF} = V_{CC} (Note 5)			±1			±1	LSB
Full Scale Error ML2271CXX	(Note 5)			±1			±1	LSB
Zero Scale Error ML2271CXX	(Note 5)			±1			±1	LSB
Total Unadjusted Error ML2271CXX	(Note 5)			±1.5			±2.0	LSB
$+V_{REF}$ Voltage Range	(Note 6)	$–V_{REF}$		V_{CC}+0.1	$–V_{REF}$		V_{CC}+0.1	V
$–V_{REF}$ Voltage Range	(Note 6)	GND–0.1		$+V_{REF}$	GND–0.1		$+V_{REF}$	V
Reference Input Resistance	(Note 5)	0.9	1.3	1.7	0.9	1.3	1.7	kΩ
Analog Input Range	(Notes 5,8)	$–V_{REF}$		$+V_{REF}$	$–V_{REF}$		$+V_{REF}$	V
Power Supply Sensitivity	DC V_{CC} = 5V ± 5%, V_{REF} = 4.75V (Note 5)		±1/32	±1/4		±1/32	±1/4	LSB
	100mV_{P-P}, 100kHz sine on V_{CC}, V_{IN} = 0 (Note 5)		±1/16			±1/16		LSB
Analog Input Leakage Current	Converter Idle (Notes 5,9)	–2		+2	–2		+2	µA
Analog Input Capacitance	During Acquisition Period		25			25		pF

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, D V_{CC} = A V_{CC} = $+V_{REF}$ = 5V ±5%, and $-V_{REF}$ = GND

PARAMETER	CONDITIONS	ML2271CCX			ML2271CIX			UNITS
		MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
Digital and DC								
$V_{IN(1)}$, Logical "1" Input Voltage	(Note 5)	2.0			2.0			V
$V_{IN(0)}$, Logical "0" Input Voltage	(Note 5)			0.8			0.8	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN} = V_{CC}$ (Note 5)			1			1	µA
$I_{IN(0)}$, Logical "0" Input Current	V_{IN} = 0V (Note 5)	–1			–1			µA
$V_{OUT(1)}$, Logical "1" Output Voltage	I_{OUT} = –2mA (Note 5)	4.0			4.0			V
$V_{OUT(0)}$, Logical "0" Output Voltage	I_{OUT} = 2mA (Note 5)			0.4			0.4	V
I_{OUT}, Three-State	V_{OUT} = 0V (Note 5)	–1			–1			µA
Output Current	$V_{OUT} = V_{CC}$ (Note 5)			1			1	µA
C_{OUT}, Logic Output Capacitance			5			5		pF
C_{IN}, Logic Input Capacitance			5			5		pF
I_{CC}, Supply Current, Analog Plus Digital	$\overline{CS} = \overline{WR} = \overline{RD}$ = 0 No Output Load (Note 5)			32			35	mA
AC and Dynamic Performance (Note 9)								
t_{CONV}, Conversion Time, Interrupt Mode	Figure 2 t_{WR} = 250ns (Note 6)			1.65			1.8	µs
t_{CWRD}, Conversion Time, Write-Read Mode	Figure 3 (Note 5)			1.9			2.0	µs
t_{CRD}, Conversion Time, Write-Read Mode	Figure 4 (Note 6)			1.9			2.0	µs
SNR, Signal to Noise Ratio	V_{IN} = 5V, 150kHz Noise is sum of all nonfundamental components from 0–300kHz. $f_{SAMPLING}$ = 600kHz		60			60		dB
HD, Harmonic Distortion	V_{IN} = 5V, 150kHz THD is sum of 2–5th harmonics or aliases relative to fundamental. $f_{SAMPLING}$ = 600kHz		–60			–60		dB
IMD, Intermodulation Distortion	fa = 2.5V, 150kHz fb = 2.5V, 148kHz IMB is (fa + fb), (fa – fb), (2fa + fb), (2fa – fb), relative to fundamental. $f_{SAMPLING}$ = 600kHz		–60			–60		dB
FR, Frequency Response	V_{IN} = 5V, 0–150kHz Relative to 1kHz $f_{SAMPLING}$ = 600kHz		±0.1			±0.1		dB
SR, Slew Rate Tracking			2.36			2.36		V/µs

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, $T_A = T_{MIN}$ to T_{MAX}, D V_{CC} = A V_{CC} = $+V_{REF}$ = 5V ±5%, and $-V_{REF}$ = GND

PARAMETER	CONDITIONS	ML2271CCX			ML2271CIX			UNITS
		MIN	TYP (Note 4)	MAX	MIN	TYP (Note 4)	MAX	
AC Performance, Figures 2, 3, 4, and 5								
t_{CSS}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Setup Time	(Note 5)	0			0			ns
t_{CSH}, $\overline{CS}$ to $\overline{RD}$, $\overline{WR}$ Hold Time	(Note 5)	0			0			ns
t_{WR}, $\overline{WR}$ Pulse Width	(Note 5)	250		50K	250		50K	ns
t_{ACC2}, $\overline{WR}$ to Data Valid	(Note 5)			2.05			2.05	µs
t_{RD}, Read Pulse Width	(Note 5)	100			100			ns
t_{WRL}, $\overline{WR}\uparrow$ to $\overline{RD}\downarrow$	(Note 6)	0			0			ns
t_{INTH}, $\overline{RD}\uparrow$ to $\overline{INT}\uparrow$	(Note 5)	10		55	10		55	ns
t_{ACC1}, Data Access Time, $\overline{RD}\downarrow$ to Data Valid	(Note 5)	0		55	0		55	ns
t_{ID}, Data Access Time, $\overline{INT}\downarrow$ to Data Valid	(Note 5)	0		50	0		50	ns
t_{1H}, t_{0H}, $\overline{RD}\uparrow$ to Data High Impedance State	Figure 1 (Note 5)	10		50	10		60	ns
t_P, Delay From End of Conversion to Next Conversion	(Note 6)			20			20	ns
t_{IC}, $\overline{INT}\downarrow$ to Start of Next Conversion	(Note 5)	500			500			ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: When the voltage at any pin exceeds the power supply rails (V_{IN} < or GND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25mA or less.

Note 3: 0°C to +70°C and –40°C to +85°C operating temperature range devices are 100% tested with temperature limits guaranteed by 100% testing, sampling, or by correlation with worst-case test conditions.

Note 4: Typicals are parametric norm at 25°C.

Note 5: Parameter guaranteed and 100% production tested.

Note 6: Parameter guaranteed. Parameters not 100% tested are not in outgoing quality level calculation.

Note 7: Total unadjusted error includes offset, full scale, linearity, and sample and hold errors.

Note 8: For $-V_{REF} \geq V_{IN}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to the analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct — especially at elevated temperatures, and cause errors for analog inputs near full scale. The spec allows 100mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 100mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of $4.900V_{DC}$ over temperature variations, initial tolerance and loading.

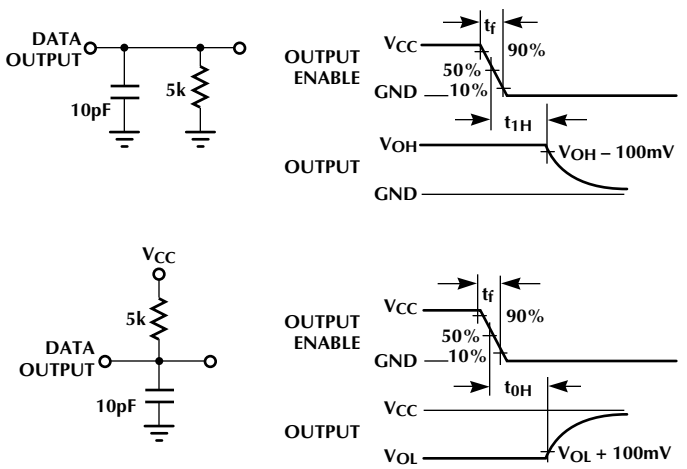


Figure 1. High Impedance Test Circuits and Waveforms

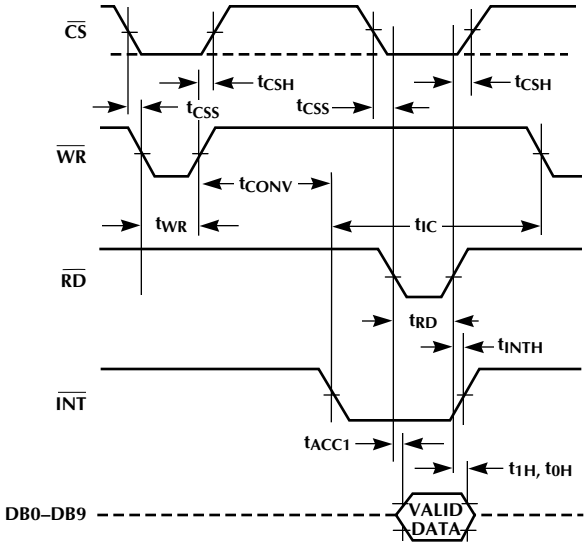


Figure 2. Interrupt Mode Timing

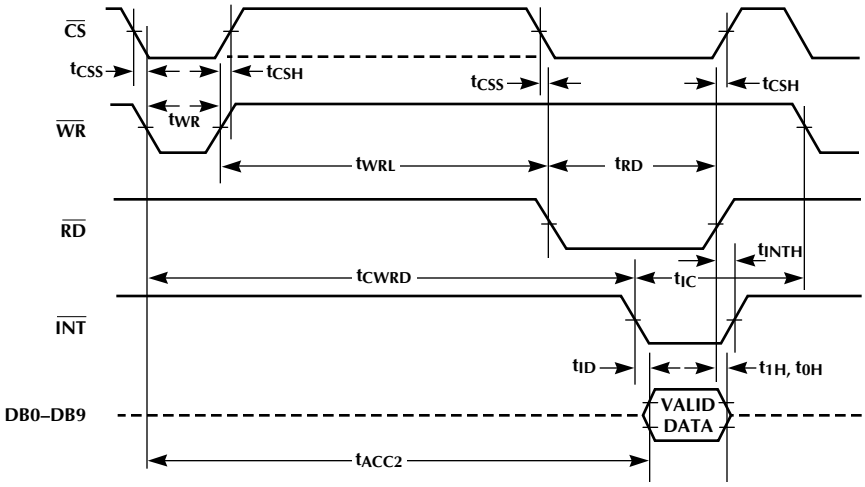
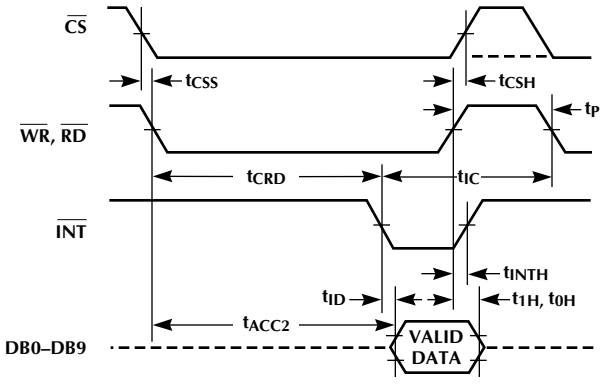


Figure 3. WR-RD Mode Timing



READ IS TIED TO WRITE

Figure 4. RD Mode Timing

1.0 FUNCTIONAL DESCRIPTION

The ML2271 uses a three step flash technique for A/D conversion. This technique first performs a 3 bit flash conversion on V_{IN} to determine the 3 most significant bits (MSB decision). These 3 MSB's are then cycled through an internal DAC to recreate the analog input. This reconstructed analog input signal from the DAC is then subtracted from the input, and the difference voltage is converted by a second 3 bit flash conversion providing the next 3 significant bits, called intermediate significant bits (ISB decision). This procedure is then performed again to provide the final 4 least significant bits (LSB decision).

The ML2271 has a true internal sample and hold. The internal operating sequence is shown in Figure 5. The falling edge of $\overline{WR}$ opens the S/H sampling switch, ends the acquisition time for the analog input, and starts the conversion on the internally sample and held signal. Then the MSB, ISB, and LSB decisions are made. $\overline{INT}$ goes low at end of conversion and $\overline{RD}$ controls the data outputs. This falling edge of $\overline{INT}$ also closes the sampling switch and starts the acquisition period for the next conversion.

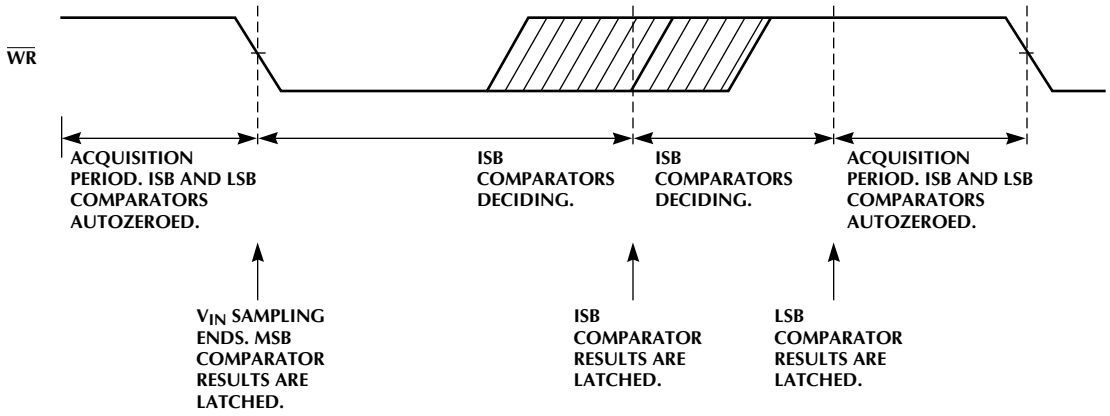


Figure 5. Operating Sequence

1.1 ANALOG INPUT

The analog input on the ML2271 behaves differently than inputs on conventional converters. The analog input current requirements change while the conversion is in progress, and the amount of input current depends on what cycle the converter is in.

The input circuit for the converter is shown in Figure 6A with the equivalent input circuit shown in Figure 6B. The acquisition period for the S/H starts on $\overline{INT}$ falling edge and ends on $\overline{WR}$ falling edge.

The critical period for charging up the analog input occurs during the acquisition period and the source of the external signal on V_{IN} must adequately charge up the analog voltage during this time. To do this, the input must settle within the required analog accuracy tolerance 100ns before the end of the acquisition period so that the sampling capacitors have adequate time to store the input signal. If more time is needed due to finite charging or settling time of the external source, the $\overline{WR}$ high period can be extended as long as is required.

1.2 SAMPLE AND HOLD

The ML2271 does not have the limitation of an equivalent circuit implemented with a track/hold. An internal sample and hold acquires the analog signal, holds it internally, and then a conversion is performed on the sample and held signal. Since this is a true sample and hold function, the ML2271 can sample and hold signals with frequencies as high as 150kHz @ 5V (slew rates as high as 2.36V/µs) without sacrificing conversion accuracy.

1.3 REFERENCE

The $+V_{REF}$ and $-V_{REF}$ inputs are the reference voltages that determine the full scale and zero input voltages, respectively, for the A/D converter. Thus, $+V_{REF}$ defines the analog input which produces a full scale output and $-V_{REF}$ defines the analog input which produces an output code of all zeroes. The transfer function for the A/D converter is shown in Figure 7.

$+V_{REF}$ and $-V_{REF}$ can be set to any voltage between GND and V_{CC}. This means that the reference voltages can be offset from GND and the difference between $+V_{REF}$ and $-V_{REF}$ can be made small to increase the resolution of the conversion. Note that the linearity error increases when $[+V_{REF} - (-V_{REF})]$ decreases.

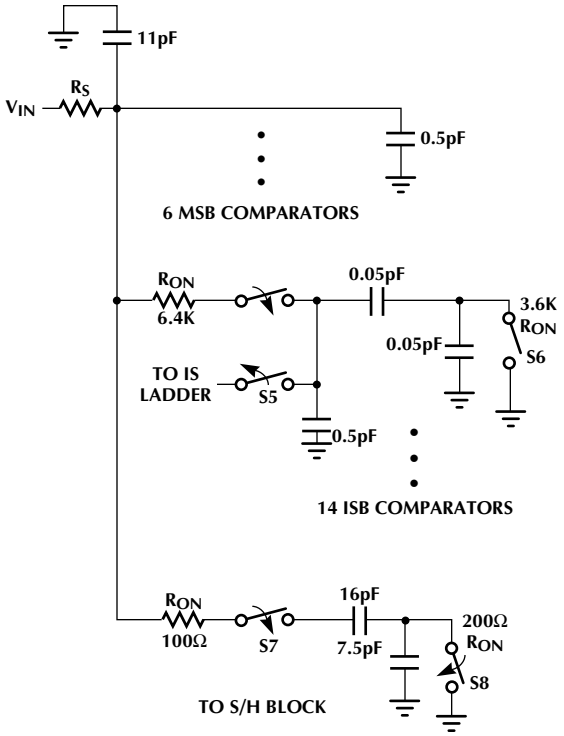


Figure 6A. Converter Input Circuit

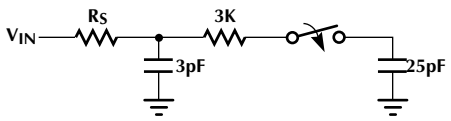


Figure 6B. Converter Equivalent Input Circuit

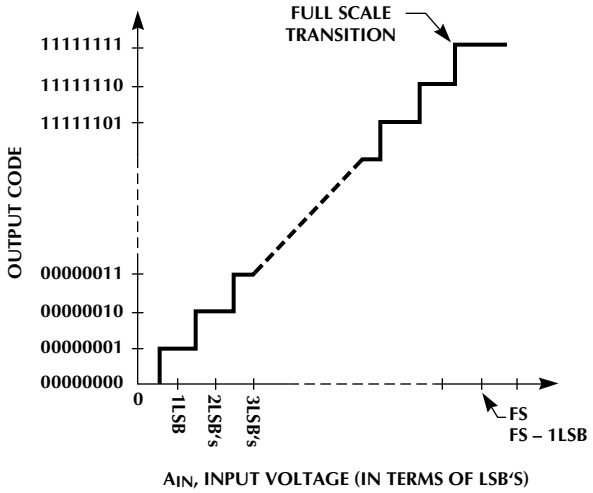


Figure 7. A/D Transfer Characteristic

1.4 POWER SUPPLY AND REFERENCE DECOUPLING

0.1µF in parallel with 0.01µF ceramic disc capacitors are recommended to bypass A V_{CC} to GND, as well as D V_{CC} to GND, using the shortest lead lengths possible.

If $+V_{REF}$ and $-V_{REF}$ inputs are driven by long lines, they should be bypassed by 0.1µF in parallel with 0.01µF ceramic disc capacitors at the reference input pins.

1.5 DYNAMIC PERFORMANCE

1.5.1 Sinusoidal Inputs

Since the ML2271 has an internal sample and hold, the device can digitize high frequency sinusoids with little or no signal degradations. Using the Nyquist criteria, the highest frequency input to the converter could theoretically by 1/2 the sampling rate (f_S). Any frequency components above $f_S/2$ will be aliased below $f_S/2$. In most applications, these aliased components cause unacceptable distortion and must be filtered out of the input. If the input frequency is too close to $f_S/2$, then the requirements on the antialias filter become difficult or impossible to realize with standard component and tolerances. In most practical applications, the highest input frequency has to be limited to 1/3 to 1/4 of f_S in order to relax the filtering requirements enough to make a realizable antialias filter.

The maximum sampling rate (f_{MAX}) for the ML2271 can be calculated as follows:

$$f_{MAX} = \frac{1}{t_{CONT} + t_P}$$

$$f_{MAX} = \frac{1}{1.45\mu s + 0.300\mu s}$$

f_{MAX} = 570kHz

t_{WR} = Write Pulse Width

t_{WRD} = Write to Data Delay

t_P = Delay Time Between Conversions

Note that the dynamic performance specifications (SNR, HD, IMD and FR) for the ML2271 are all specified at 150kHz, which is less than 1/3 of the sampling rate, f_S. This allows adequate margin between the input frequency and the aliased components to allow antialias filtering if needed.

In applications where aliased frequency components are acceptable and filtering of the input signal is not needed, the user can apply an input sinusoid higher than 150kHz to the device. Note, however, that as the input frequency increases above 150kHz, dynamic performance degradation will occur due to the finite bandwidth of the internal sample and hold.

1.5.2 Signal-to-Noise Ratio

Signal-to-noise ratio (SNR) is the measured signal to noise at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling

frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more the levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for ideal 10-bit converter, SNR = 61.96 dB.

1.5.3 Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. Total harmonic distortion (THD) of the ML2271 is defined as

$$20 \log \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 are the rms amplitudes of the individual harmonics.

1.5.4 Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_A and f_B, any active device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of $mf_A + nf_B$, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. The (IMD) intermodulation distortion specification includes the second order terms ($f_A + f_B$) and ($f_A - f_B$) and the third order terms ($2f_A + f_B$), ($2f_A - f_B$), and ($f_A - 2f_B$) only.

1.6 DIGITAL INTERFACE

Depending on the way the external signals are applied to the ML2271, the timing of the conversion and resultant digital interface can be configured in three different modes.

While the operation for each mode is described below, there are some general rules that dictate the general relationships between $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{INT}$, and DB0–DB9. The falling edge of $\overline{WR}$ terminates the acquisition period and initiates a conversion. $\overline{INT}$ is forced low when a conversion is internally completed. $\overline{INT}$ is reset high by the $\overline{RD}$ rising edge. DB0–DB9 is in the high impedance state except when both $\overline{RD}$ and $\overline{INT}$ are low. $\overline{RD}$ low period does not affect the internal conversion but only determines when the digital signals DB0–DB9 are active; thus, $\overline{RD}$ can occur anytime. $\overline{CS}$ is used to select the device and needs to be low only while $\overline{WR}$ is low or when $\overline{RD}$ is low.

1.6.1 Interrupt Mode

Timing for the Interrupt Mode is shown in Figure 2. To do a conversion, $\overline{CS}$ must be low to select the device. $\overline{INT}$ falling edge starts the acquisition period. The falling edge of $\overline{WR}$ ends the acquisition period and the MSB comparison is made. Then, the (Intermediate Significant Bits) ISB and LSB decisions are made with internal timing signals. After the conversion is complete, $\overline{INT}$ goes low indicating end of conversion. When $\overline{RD}$ goes low, DB0–DB9 goes from high impedance to the active state with the digital result of the conversion. $\overline{INT}$ is rest high and DB0–DB9 is reset to high impedance on the rising edge of $\overline{RD}$.

Interrupt Operation is intended to be used in interrupt driven systems or applications where $\overline{INT}$ signals the transfer of data.

1.6.2 Write-Read Mode

Write-Read Operation is the same as Interrupt Operation except that $\overline{RD}$ is brought low before the internal conversion is completed (before $\overline{INT}$ goes low).

Timing for Write-Read Operation is shown in Figure 3. To perform a conversion, $\overline{CS}$ must be low to select the device. $\overline{INT}$ falling edge starts the acquisition period. The falling edge of $\overline{WR}$ ends the acquisition period and the MSB decision is made. Then, the ISB and LSB decisions are made by internal timing signals. In this mode, $\overline{RD}$ is brought low before the internal conversion is completed. When the internal conversion is completed, $\overline{INT}$ will be forced low and data will appear on DB0–DB9 as long as $\overline{RD}$ is still low. $\overline{INT}$ is reset high and DB0–DB9 is reset to high impedance on the rising edge of $\overline{RD}$.

Write-Read Operation is intended for applications where $\overline{RD}$ controls the transfer of data to a microprocessor.

1.6.3 Read Mode

Read Mode Operation is implemented by tying $\overline{RD}$ to $\overline{WR}$ and keeping $\overline{RD}$ and $\overline{WR}$ low long enough so that the conversion time is totally determined by the internal timing signals.

Timing for the Read Mode is shown in Figure 4. To do a conversion, $\overline{CS}$ must be low to select the device. The $\overline{RD}$ and $\overline{WR}$ falling edge starts the conversion. $\overline{RD}$ and $\overline{WR}$ is held low for the entire internal conversion. Thus, the MSB, ISB, and LSB comparisons along with the end of the acquisition period are made by internally generated timing signals. After the conversion is complete, $\overline{INT}$ goes low. Since $\overline{RD}$ is fixed low, DB0–DB9 will go from high impedance to active state as soon as $\overline{INT}$ goes low. $\overline{INT}$ is reset high and DB0–DB9 is reset to high impedance on rising edge of $\overline{WR}$ and $\overline{RD}$.

Read Mode Operation allows a conversion to be done with the device's own internal timing and thus, no eternal timing is needed.

1.6.4 Power-On Reset

When power is first applied, an internal power-on reset and timer circuit inhibits the $\overline{CS}$ input and resets the internal circuitry to prevent the ML2271 from starting in an unknown state. During this period of approximately 5µs, $\overline{INT}$ remains high and the data bus is in the high-impedance state.

2.0 TYPICAL APPLICATIONS

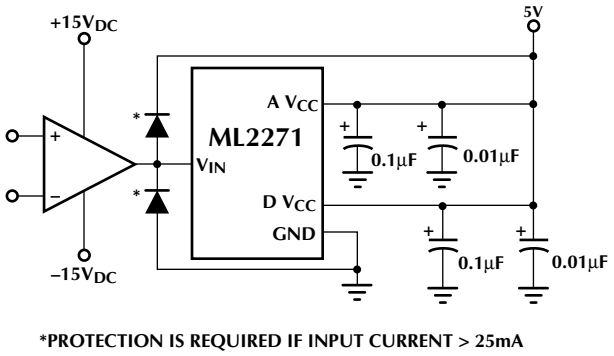


Figure 8. Protecting the Input

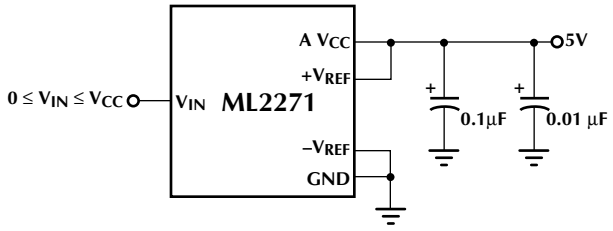


Figure 9. Using V_{CC} as Reference for Ratiometric Operation

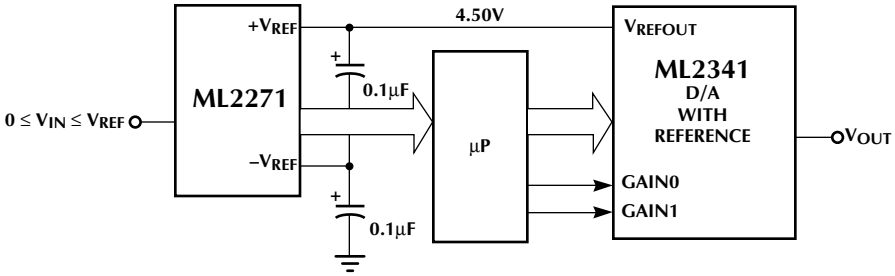


Figure 10. Using External Reference of D/A

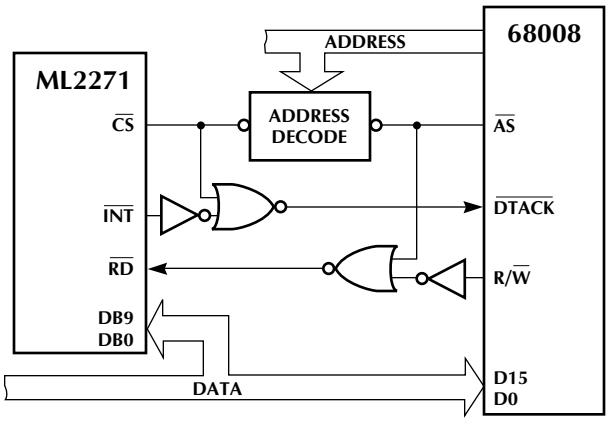


Figure 11. 68000 Type Interface to ML2271

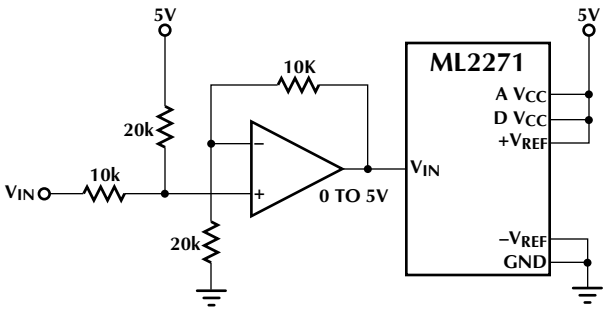


Figure 12. ±2.5V Analog Input Range

2.0 TYPICAL APPLICATIONS (Continued)

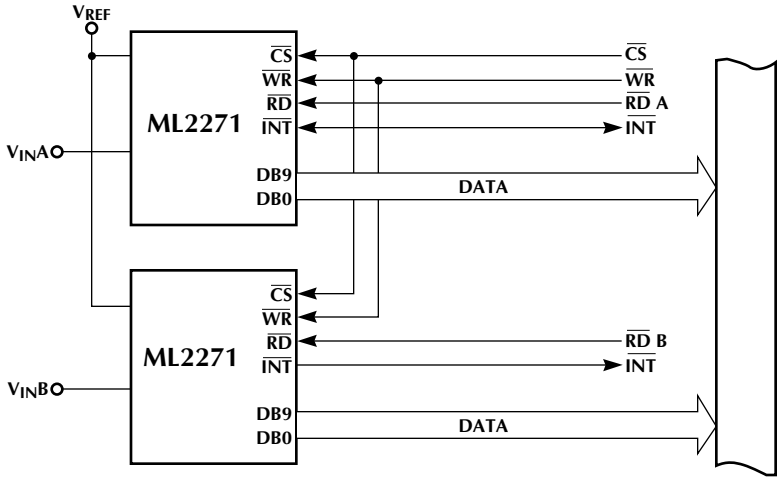


Figure 13. Simultaneous Sampling of Two Variables

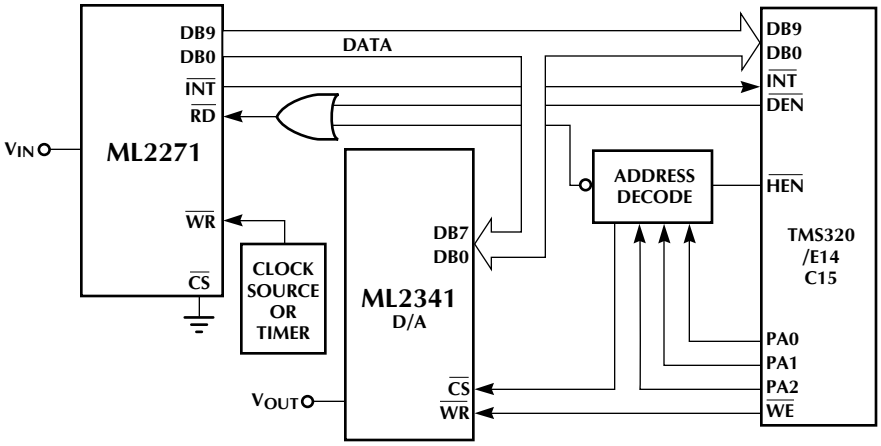


Figure 14. TMS320 Interface with D/A Output

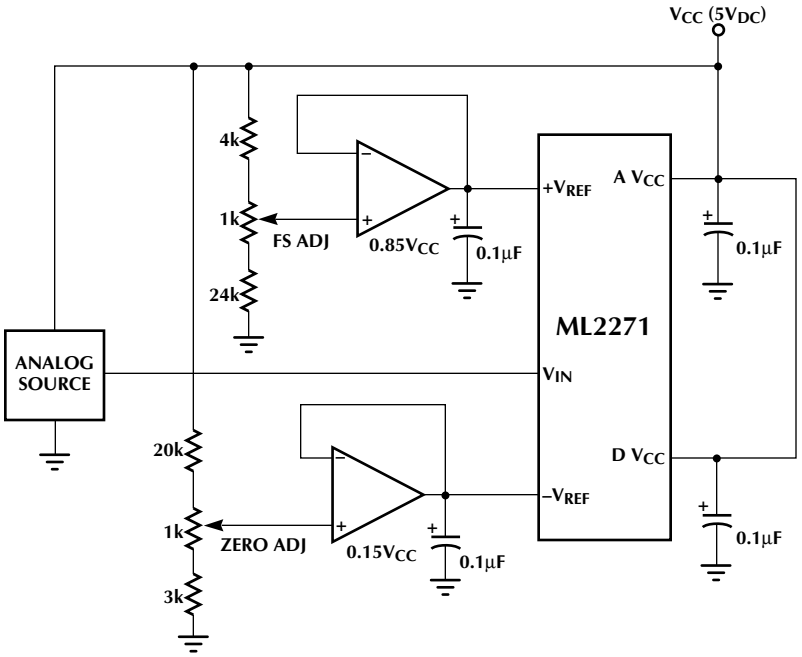
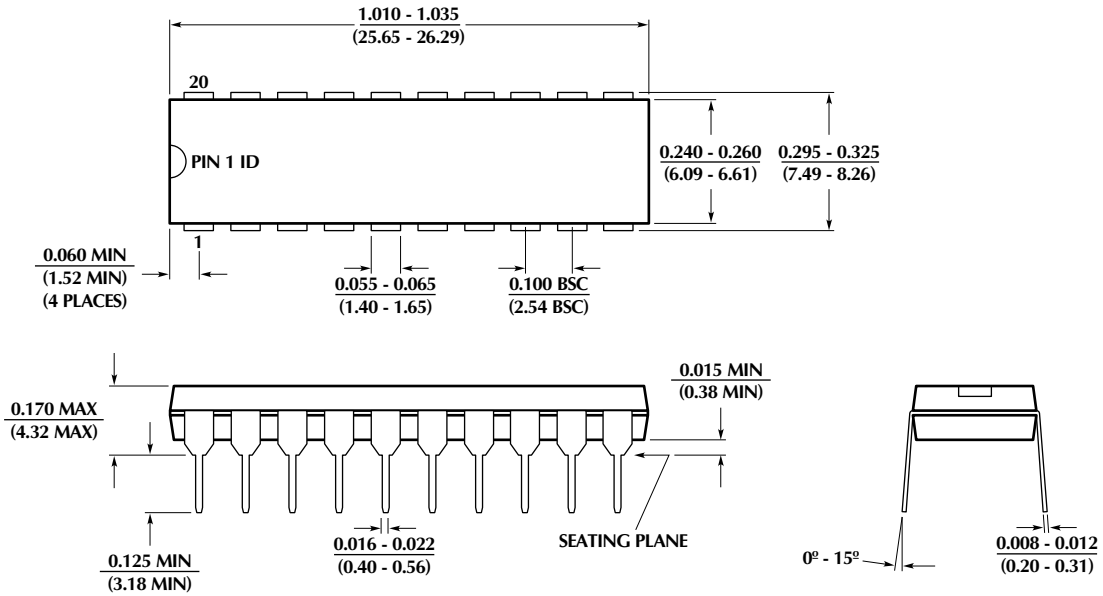


Figure 15. Operating with a Ratiometric Analog Signal of 15% of V_{CC} to 85% of V_{CC}

PHYSICAL DIMENSIONS inches (millimeters)

Package: P20
20-Pin PDIP



ORDERING INFORMATION

PART NUMBER	LINEARITY ERROR	TEMPERATURE RANGE	PACKAGE
ML2271CIP	±1 LSB	–40°C TO +85°C	MOLDED DIP (P20)
ML2271CIS		–40°C TO +85°C	MOLDED SOIC (S20)
ML2271CCP	±1 LSB	0°C TO +70°C	MOLDED DIP (P20)
ML2271CCS		0°C TO +70°C	MOLDED SOIC (S20)

2092 Concourse Drive
San Jose, CA 95131
Tel: 408/433-5200
Fax: 408/432-0295

Micro Linear

To receive a price quote or to request a product sample, call or send e-mail to your local representative.

When sending e-mail, be sure to include the Micro Linear part number and whether you want a price quote or a sample in the subject line.

(i.e. subject: Sample request - ML part#xxxx)

Click here to find your local representative