

74LCX32244

Low Voltage 32-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The LCX32244 contains thirty-two non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 32-bit operation.

The LCX32244 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX32244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
 - 2.3V–3.6V V_{CC} specifications provided
 - 4.5 ns t_{PD} max ($V_{CC} = 3.0V$), 20 μA I_{CC} max
 - Power down high impedance inputs and outputs
 - Supports live insertion/withdrawal (Note 1)
 - ± 24 mA output drive ($V_{CC} = 3.0V$)
 - Uses patented noise/EMI reduction circuitry
 - Latch-up performance exceeds 500 mA
 - ESD performance:
 - Human body model > 2000V
 - Machine model > 200V
 - Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)
- Note 1:** To ensure the high-impedance state during power up or down $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

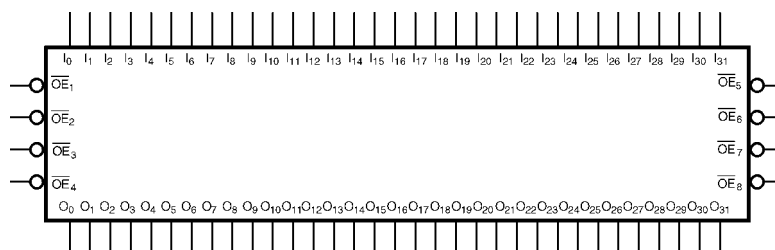
Ordering Code:

Order Number	Package Number	Package Description
74LCX32244G (Note 2)(Note 3)	BGA96A	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

Note 2: Ordering code "G" indicates Trays.

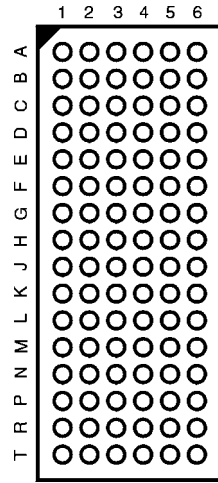
Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



74LCX32244 Low Voltage 32-Bit Buffer/Line Driver with 5V Tolerant Inputs and Outputs

Connection Diagram

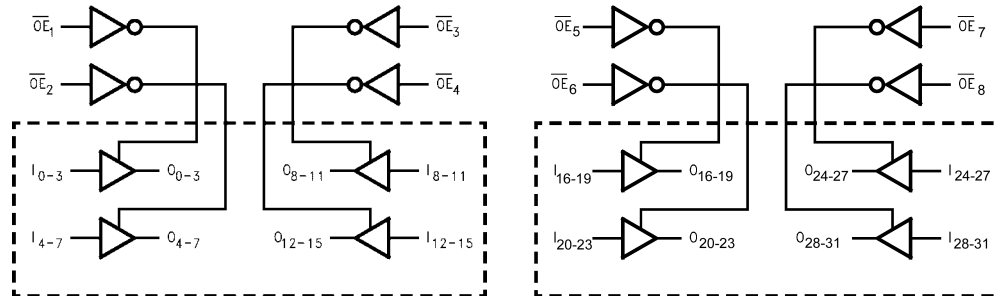


(Top Thru View)

Functional Description

The LCX32244 contains thirty-two non-inverting buffers with 3-STATE standard outputs. The device is nibble (4-bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 32-bit operation. The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input for each nibble. When $\overline{OE}_n$ is LOW, the outputs are in 2-state mode. When $\overline{OE}_n$ is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagrams



Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
I_0-I_{31}	Inputs
O_0-O_{31}	Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_1	O_0	$\overline{OE}_1$	$\overline{OE}_2$	I_0	I_1
B	O_3	O_2	GND	GND	I_2	I_3
C	O_5	O_4	V_{CC}	V_{CC}	I_4	I_5
D	O_7	O_6	GND	GND	I_6	I_7
E	O_9	O_8	GND	GND	I_8	I_9
F	O_{11}	O_{10}	V_{CC}	V_{CC}	I_{10}	I_{11}
G	O_{13}	O_{12}	GND	GND	I_{12}	I_{13}
H	O_{14}	O_{15}	$\overline{OE}_4$	$\overline{OE}_3$	I_{15}	I_{14}
J	O_{17}	O_{16}	$\overline{OE}_5$	$\overline{OE}_6$	I_{16}	I_{17}
K	O_{19}	O_{18}	GND	GND	I_{18}	I_{19}
L	O_{21}	O_{20}	V_{CC}	V_{CC}	I_{20}	I_{21}
M	O_{23}	O_{22}	GND	GND	I_{22}	I_{23}
N	O_{25}	O_{24}	GND	GND	I_{24}	I_{25}
P	O_{27}	O_{26}	V_{CC}	V_{CC}	I_{26}	I_{27}
R	O_{29}	O_{28}	GND	GND	I_{28}	I_{29}
T	O_{30}	O_{31}	$\overline{OE}_8$	$\overline{OE}_7$	I_{31}	I_{30}

Truth Table

Inputs		Outputs
$\overline{OE}_n$	I_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial (HIGH or LOW, inputs may not float)

Z = High Impedance

Absolute Maximum Ratings ^(Note 4)				
Symbol	Parameter	Value	Conditions	Units
V _{CC}	Supply Voltage	−0.5 to +7.0		V
V _I	DC Input Voltage	−0.5 to +7.0		V
V _O	DC Output Voltage	−0.5 to +7.0 −0.5 to V _{CC} + 0.5	Output in 3-STATE Output in HIGH or LOW State (Note 5)	V
I _{IK}	DC Input Diode Current	−50	V _I < GND	mA
I _{OK}	DC Output Diode Current	−50 +50	V _O < GND V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current per Supply Pin	±100		mA
I _{GND}	DC Ground Current per Ground Pin	±100		mA
T _{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 6)					
Symbol	Parameter	Min	Max	Units	
V _{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V _I	Input Voltage	0	5.5	V	
V _O	Output Voltage	HIGH or LOW State	0	V _{CC}	V
		3-STATE	0	5.5	
I _{OH} /I _{OL}	Output Current	V _{CC} = 3.0V – 3.6V V _{CC} = 2.7V – 3.0V V _{CC} = 2.3V – 2.7V		±24 ±12 ±8	mA
T _A	Free-Air Operating Temperature	−40	85	°C	
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V	0	10	ns/V	

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

Note 5: I_O Absolute Maximum Rating must be observed.

Note 6: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics						
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = −40°C to +85°C		Units
				Min	Max	
V _{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V _{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V _{OH}	HIGH Level Output Voltage	I _{OH} = −100 μA	2.3 – 3.6	V _{CC} − 0.2		V
		I _{OH} = −8 mA	2.3	1.8		
		I _{OH} = −12 mA	2.7	2.2		
		I _{OH} = −18 mA	3.0	2.4		
		I _{OH} = −24 mA	3.0	2.2		
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3 – 3.6		0.2	V
		I _{OL} = 8 mA	2.3		0.6	
		I _{OL} = 12 mA	2.7		0.4	
		I _{OL} = 16 mA	3.0		0.4	
		I _{OL} = 24 mA	3.0		0.55	
I _I	Input Leakage Current	0 ≤ V _I ≤ 5.5V	2.3 – 3.6		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 5.5V V _I = V _{IH} or V _{IL}	2.3 – 3.6		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3 – 3.6		20	μA
		3.6V ≤ V _I , V _O ≤ 5.5V (Note 7)	2.3 – 3.6		±20	
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} -0.6V	2.3 – 3.6		500	μA

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

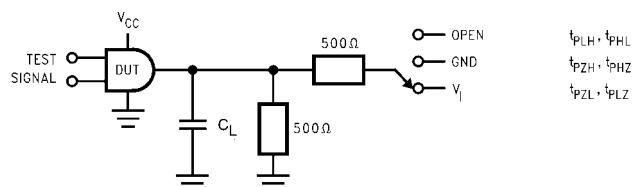
Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500 Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		
		C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
		Min	Max	Min	Max	Min	Max	
t _{PHL}	Propagation Delay	1.0	4.5	1.0	5.2	1.0	5.4	ns
t _{PLH}	Data to Output	1.0	4.5	1.0	5.2	1.0	5.4	
t _{PZL}	Output Enable Time	1.0	5.5	1.0	6.3	1.0	7.2	ns
t _{PZH}		1.0	5.5	1.0	6.3	1.0	7.2	
t _{PLZ}	Output Disable Time	1.0	5.4	1.0	5.7	1.0	6.5	ns
t _{PHZ}		1.0	5.4	1.0	5.7	1.0	6.5	

Dynamic Switching Characteristics

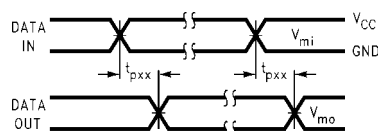
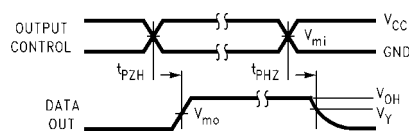
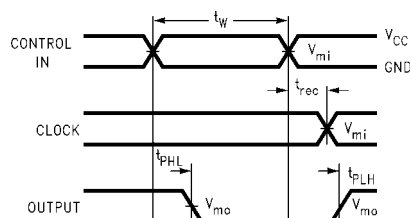
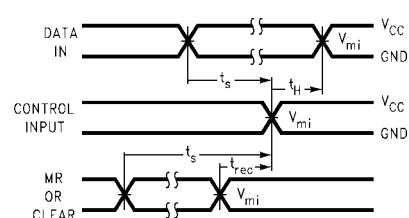
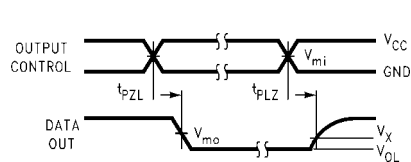
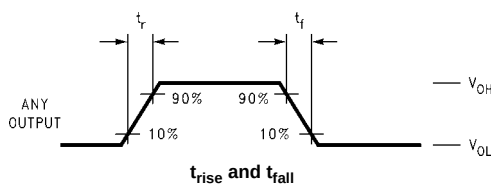
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Units
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	3.3 2.5	0.8 0.6	V
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	3.3 2.5	-0.8 -0.6	V

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10 MHz	20	pF

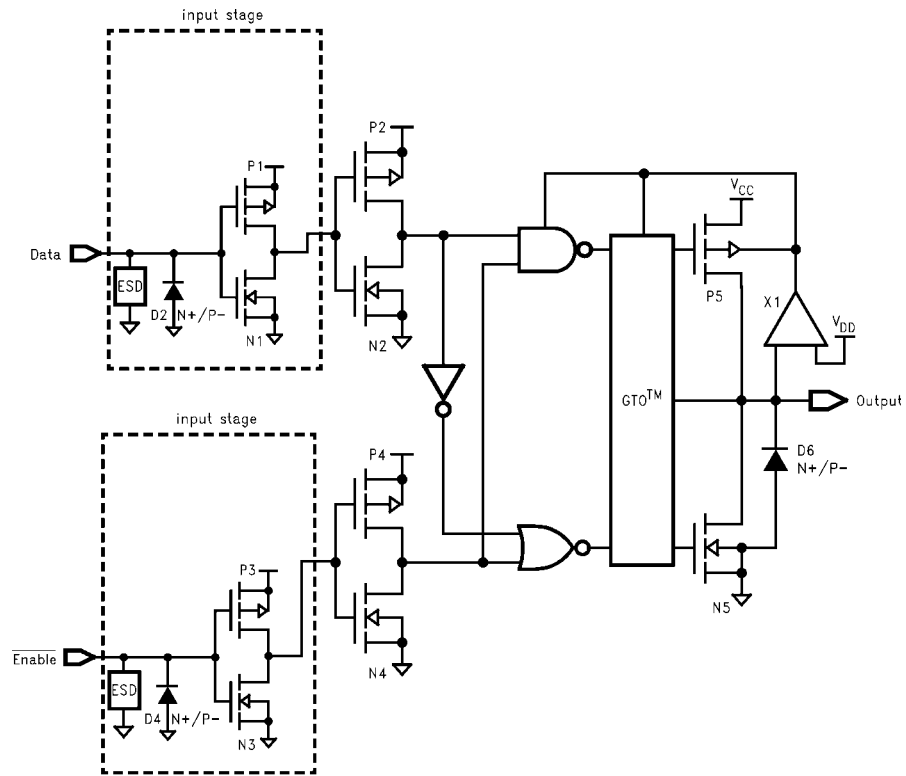
AC LOADING and WAVEFORMS Generic for LCX Family**FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)**

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$, and 2.7V $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH}, t_{PHZ}	GND

**Waveform for Inverting and Non-Inverting Functions****3-STATE Output High Enable and Disable Times for Logic****Propagation Delay, Pulse Width and t_{rec} Waveforms****Setup Time, Hold Time and Recovery Time for Logic****3-STATE Output Low Enable and Disable Times for Logic****FIGURE 2. Waveforms**
(Input Characteristics; $f = 1MHz$, $t_r = t_f = 3ns$)

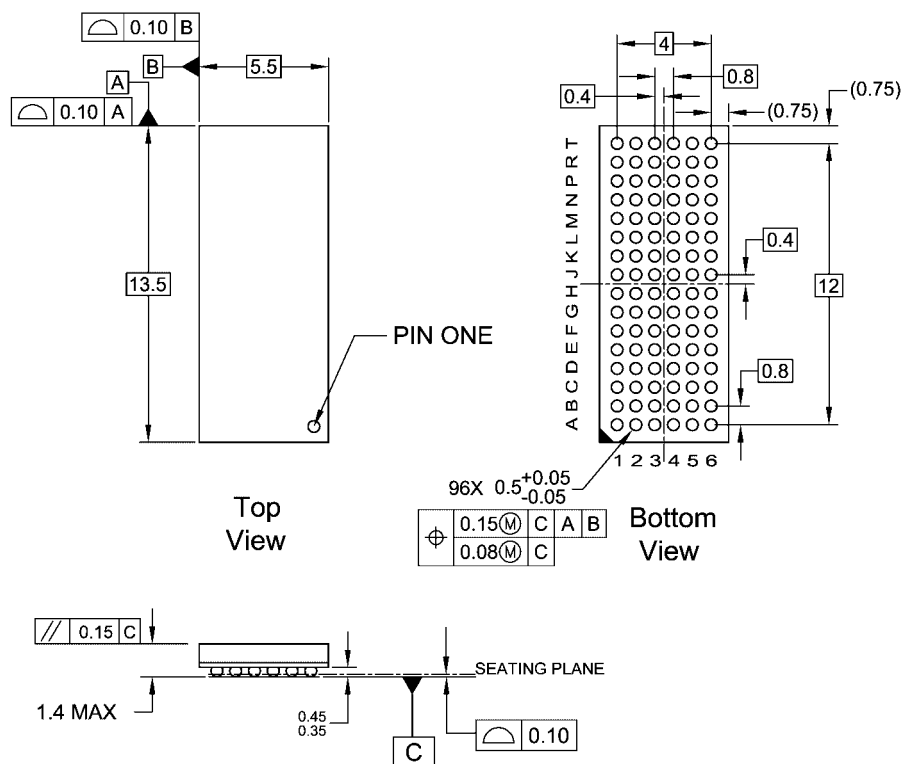
Symbol	V_{CC}		
	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family



Physical Dimensions

inches (millimeters) unless otherwise noted



NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC MO-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA96ArevE

**96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA96A**

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