VND670SP

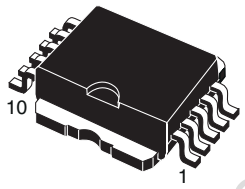
Dual high-side switch with dual Power MOSFET gate driver (bridge configuration)

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VND670SP	30mΩ(1)	15A(1)	40V

1. Per each channel.

- 5V logic level compatible inputs
- Gate drive for two external power MOSFET
- Undervoltage and overvoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Cross-conduction protection
- Current limitation
- Very low standby power consumption
- PWM operation up to 10 KHz
- Protection against loss of ground and loss of V_{CC}
- Reverse battery protection



PowerSO-10

Description

The VND670SP is a monolithic device made using STMicroelectronics VIPower technology M0-3, intended for driving motors in full bridge configuration. The device integrates two 30 mW Power MOSFET in high-side configuration, and provides gate drive for two external Power MOSFET used as low side switches. IN_A and IN_B allow to select clockwise or counter clockwise drive or brake; $DIAG_A/EN_A$, $DIAG_B/EN_B$ allow to disable one half bridge and feedback diagnostic. Built-in thermal shutdown, combined with a current limiter, protects the chip in overtemperature and short circuit conditions. Short to battery protects the external connected low-side Power MOSFET.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSO-10	VND670SP	VND670SP13TR

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1 Block diagram and pin description

Figure 1. Block diagram

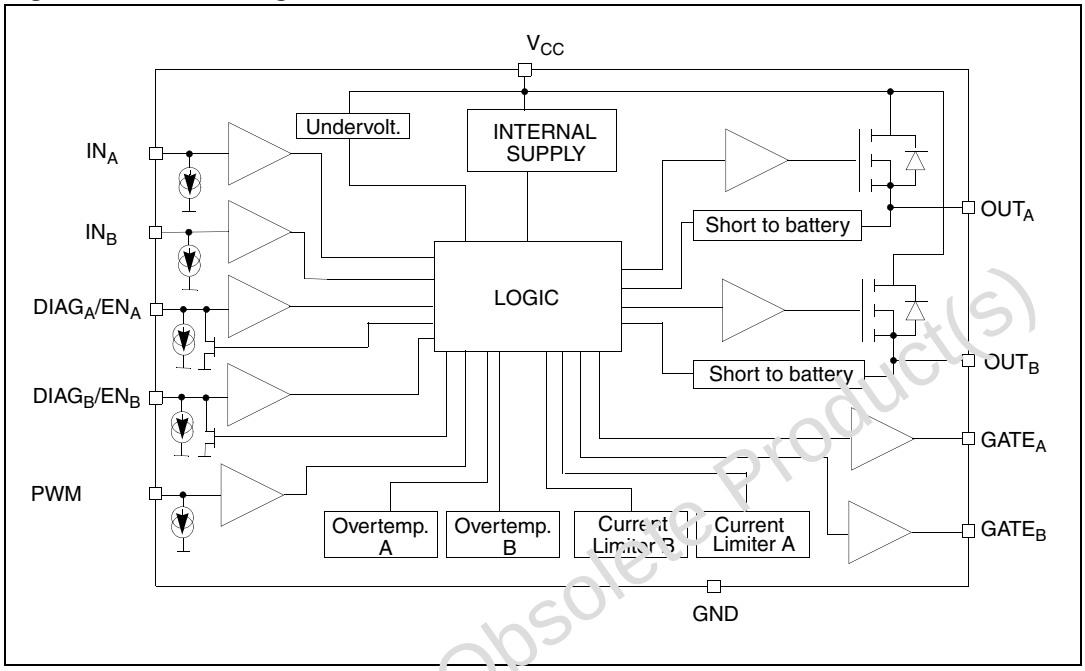


Figure 2. Configuration diagram (top view)

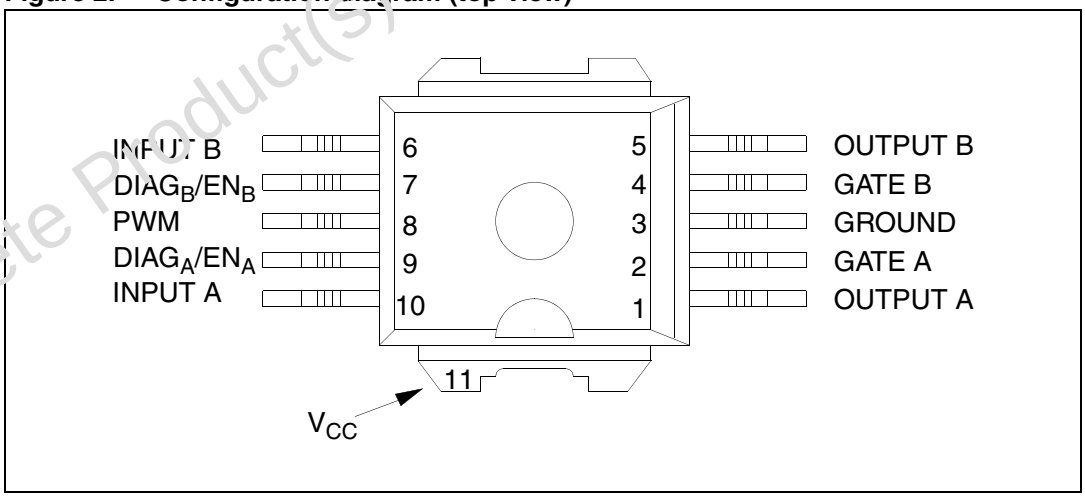
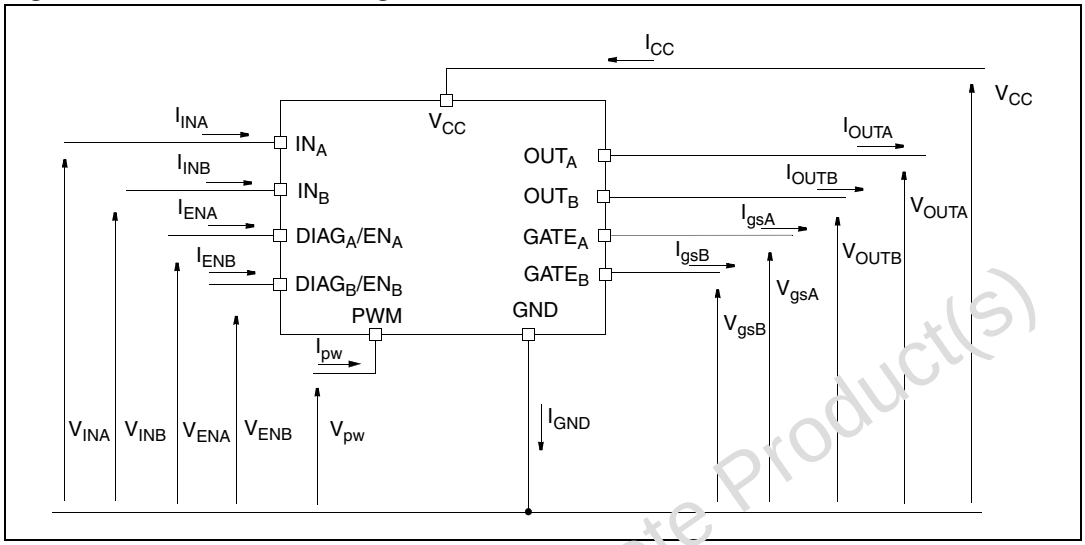


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3..40	V
I_{max1}	Maximum output current (continuous)	15	A
I_{max2}	Maximum output current (250ms pulse duration)	20	A
I_R	Reverse DC output current	- 15	A
I_{IN}	Input current	+/- 10	mA
I_{EN}	Enable pin current	+/- 10	mA
I_{pw}	PWM pin current	+/- 10	mA
I_{gs}	Output gate current	+/- 20	mA
V_{ESD}	Electrostatic discharge (R = 1.5KΩ; C = 100pF)	2000	V
T_j	Junction operating temperature	- 40 to 150	°C
T_{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 4. Thermal data (per island)

Symbol	Parameter	Max. value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.4	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	50(1)	°C/W

1. When mounted using the recommended pad size on FR-4 board (see AN515 Application Note).

2.3 Electrical characteristics

Values specified in this section are for 9V < V_{CC} < 18V; -40°C < T_j < 150°C, unless otherwise stated.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		5.5		36	V
R_{ON}	On-state resistance	I_{LOAD} = 1.2A I_{LOAD} = 1.2A Ti = 25°C		26	50 30	mΩ mΩ
I_s	Supply current	On-state Off-state			15 40	mA µA
V_{gate}	Gate output voltage		5.0		8.5	V
$V_{gs,cl}$	Gate output clamp voltage	I_{gs}= - 1 mA	6.0	6.8	8.0	V

Table 6. Switching (V_{CC} = 13V, R_{LOAD} = 1.1Ω)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{D(on)}$	Turn-on delay time	Input rise time < 1µs (see *Figure 4*)		50	150	µs
$t_{D(off)}$	Turn-off delay time			45	135	µs
t_r	Output voltage rise time			50	150	µs
t_f	Output voltage fall time			40	120	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope			160	500	V/ ms
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope			230	1200	V/ ms
t_{dong}	V_{gs}turn-on delay time	C1=4.7nF Break to ground configuration (see *Figure 5*)		0.5	2	µs
t_{rg}	V_{gs} rise time			2.6	10	µs
t_{doffg}	V_{gs}turn-off delay time			1.0	5.0	µs
t_{fg}	V_{gs} fall time			2.2	10	µs
t_{del}	External MOSFET turn-on dead time	(see *Figure 6*)		600	1800	µs

Table 7. Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{USD}	Undervoltage shutdown				5.5	V
V_{OV}	Overvoltage shutdown		36	43		V
I_{LIM}	Current limitation		30	45		A
T_{TSD}	Thermal shutdown temperature	V_{IN} = 3.25 V	150	170	200	°C
V_{ocl}	Output turn-off clamp voltage	I_{LOAD} = 12A, L = 6mH	V_{CC}-55		V_{CC}-41	V
V_{sat}	External MOSFET saturation voltage detection threshold		2.5	4.2	5.5	V

Table 8. PWM

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{pwl}	PWM low level voltage				1.5	V
I_{pwl}	PWM pin current	V_{pw} = 1.5V	1			µA
V_{pwh}	PWM high level voltage		3.25			V
I_{pwh}	PWM pin current	V_{pw} = 3.25V			10	µA
$V_{pwhhyst}$	PWM hysteresis voltage		0.5			V
V_{pwcl}	PWM clamp voltage	I_{pw} = 1 mA I_{pw} = -1 mA	V_{CC}+0.3 -5.0	V_{CC}+0.7 -3.5	V_{CC}+1.0 -2.0	V V
V_{pwtest}	Test mode PWM pin voltage		-3.5	-2.0	-0.5	V
I_{pwtest}	Test mode PWM pin current	V_{pwtest} = -2.0 V	-2000	-500		µA

Table 9. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				1.5	V
I_{INL}	Input current	V_{IN} = 1.5 V	1			µA
V_{IH}	Input high level voltage		3.25			V
I_{INH}	Input current	V_{IN} = 3.25 V			10	µA
V_{IHYST}	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN}=1mA I_{IN}=-1mA	6.0 -1.0	6.8 -0.7	8.0 -0.3	V V

Table 10. Enable

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ENL}	Enable low level voltage	Normal operation ($DIAG_X/EN_X$ pin acts as an input pin)			1.5	V
I_{ENL}	Enable pin current	V_{EN} = 1.5 V	1			µA
V_{ENH}	Enable high level voltage	Normal operation ($DIAG_X/EN_X$ pin acts as an input pin)	3.25			V
I_{ENH}	Enable pin current	V_{EN} = 3.25 V			10	µA
V_{EHYST}	Enable hysteresis voltage	Normal operation ($DIAG_X/EN_X$ pin acts as an input pin)	0.5			V
V_{ENCL}	Enable clamp voltage	I_{EN} = 1mA I_{EN} = -1mA	6.0 -1.0	6.3 -0.7	8.0 -0.3	V V
V_{DIAG}	Enable output low level voltage	Fault operation ($DIAG_X/EN_X$ pin acts as an input pin) I_{EN} = 1.6 mA			0.4	V

Figure 4. Test conditions for high side switching times measurement

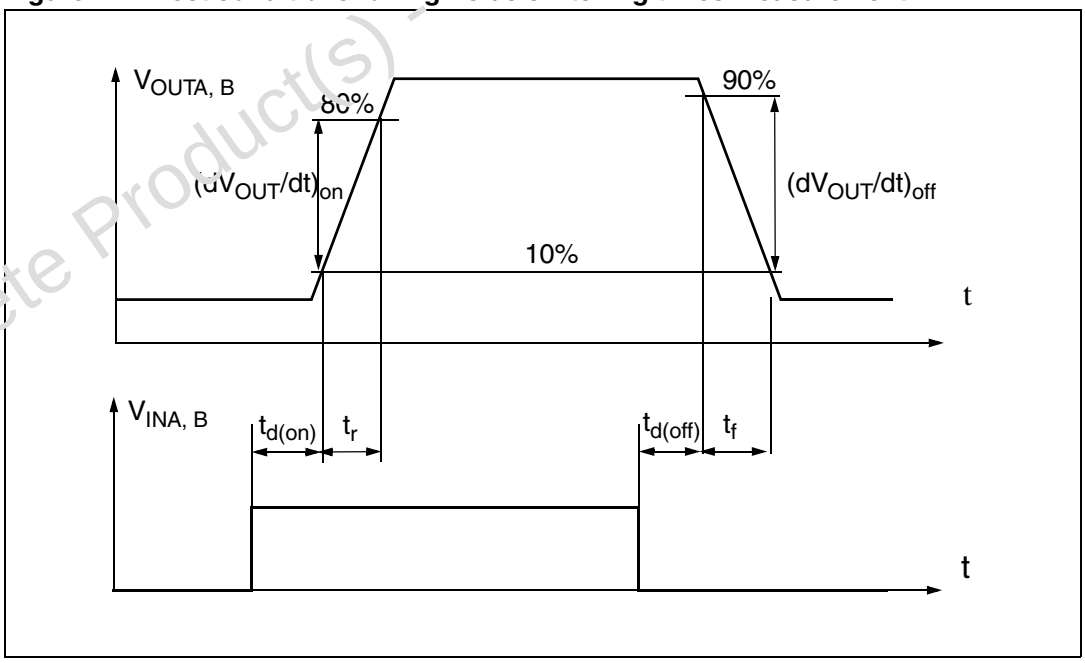


Figure 5. Test conditions for external Power MOSFET switching times measurement

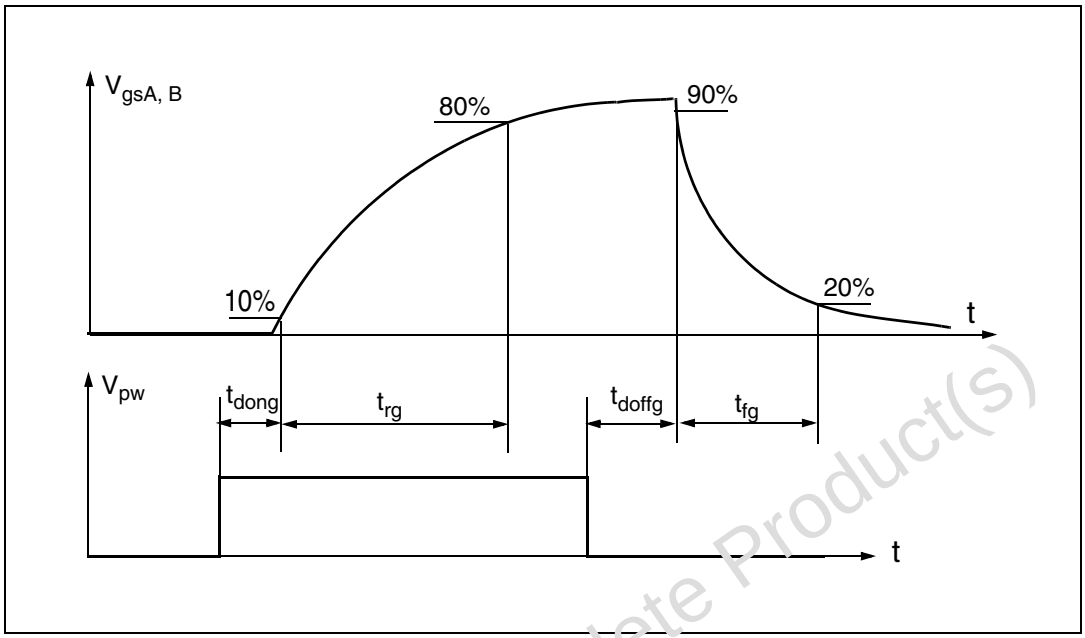
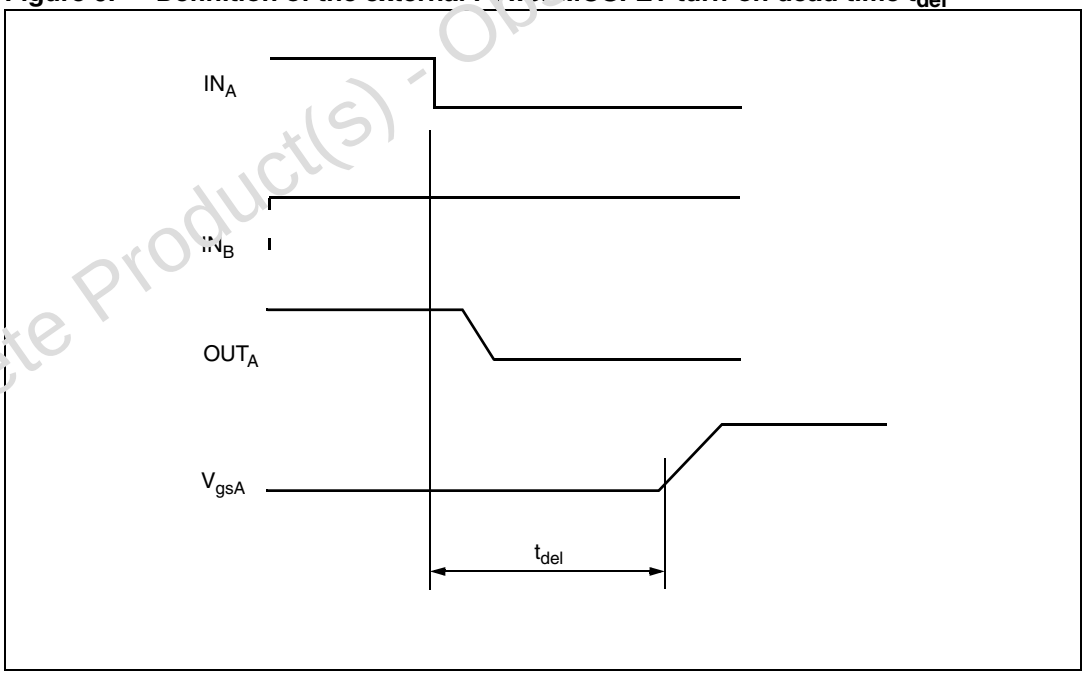
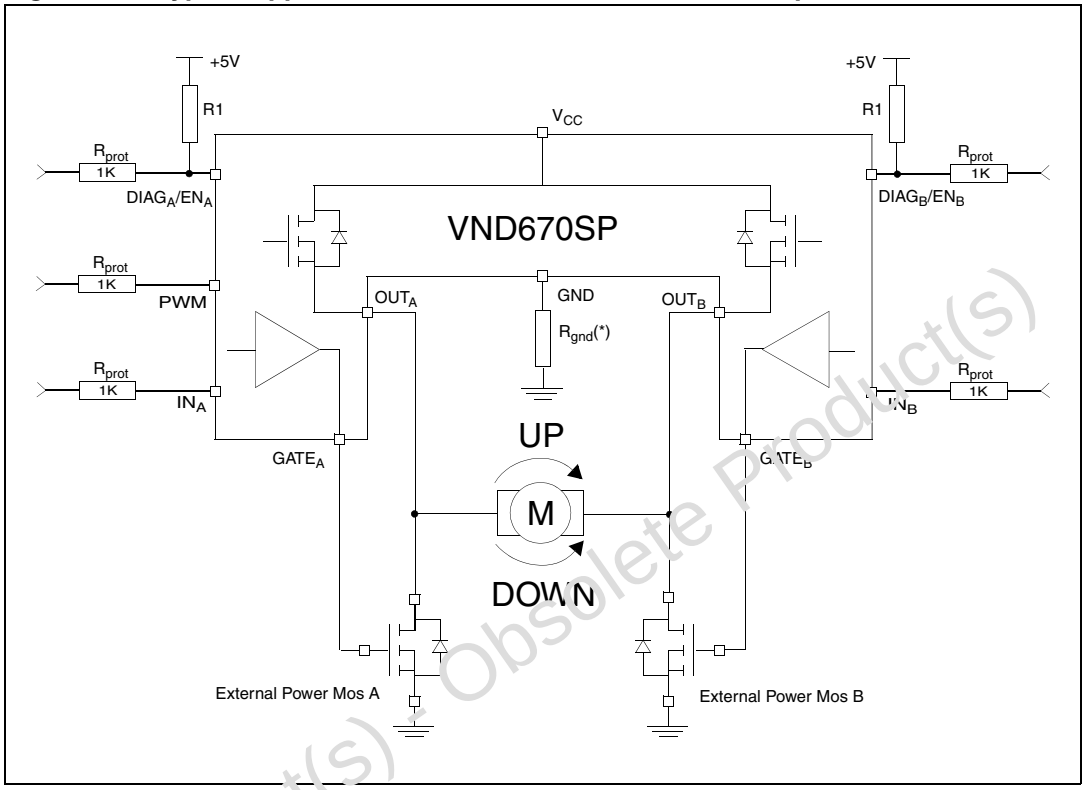


Figure 6. Definition of the external Power MOSFET turn-on dead time t_{del}



3 Application information

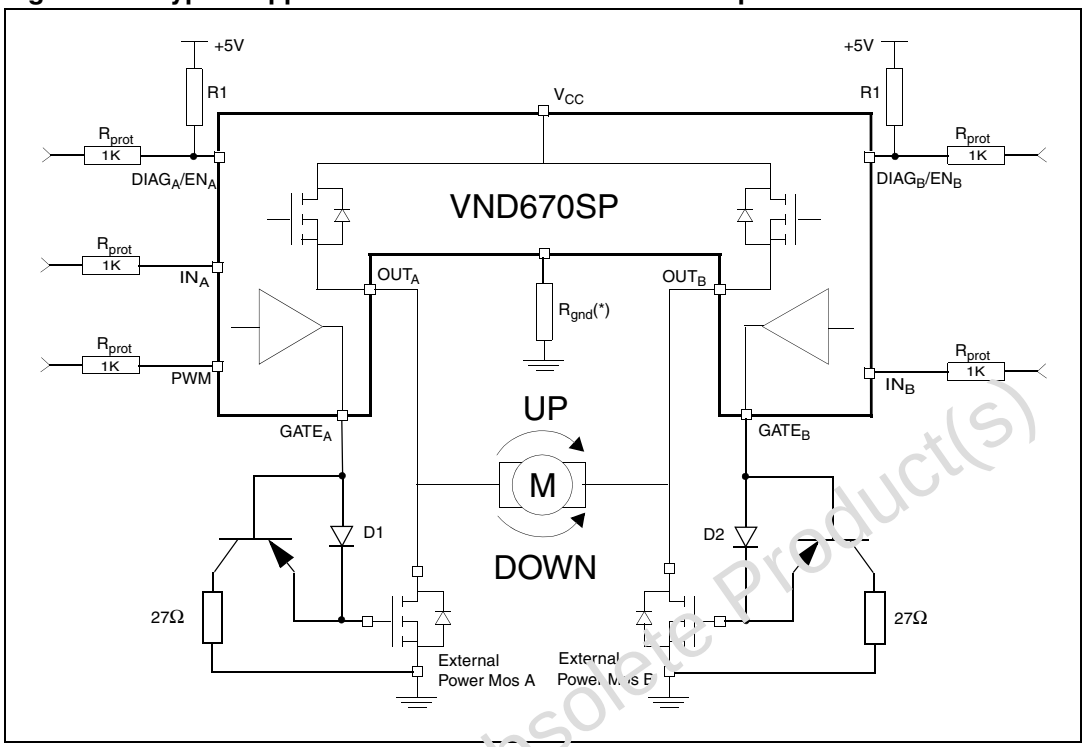
Figure 7. Typical application circuit for DC to 10 KHz PWM operation



Note: 1 Reverse battery protection: series relay in V_{CC} line: R_{gnd}=0 Ohms; series fuse in V_{CC} line with antiparallel diode between ground and V_{CC}: R_{gnd}=10 Ohms.

2 Layout hints: the connection between GND pin of the VN670SP and the Power MOSFET SOURCE connections should be kept short enough to ensure that the dynamic difference between these two points never exceed 1V for the bridge to operate properly.

Figure 8. Typical application circuit for a 20 KHz PWM operation



Note: 1 Reverse battery protection: series relay in V_{CC} line: R_{gnd} = 0 Ohms; series fuse in V_{CC} line with antiparallel diode between ground and V_{CC}: R_{gnd}=10 Ohms.

3.1 Normal operating conditions

Table 11. Truth table in normal operating conditions

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	$GATE_A$	$GATE_B$	Comment
1	1	1	1	H	H	L	L	Brake to V_{CC}
1	0	1	1	H	L	L	H	Clockwise
0	1	1	1	L	H	H	L	Counter cw
0	0	1	1	L	L	H	H	Brake to GND
X	X	0	0	L	L	L	L	Stand by
1	X	1	0	H	L	L	L	HS_A only
0	X	1	0	L	L	H	L	MOS_A only
X	1	0	1	L	H	L	L	HS_B only
X	0	0	1	L	L	L	H	MOS_B only

Note: 1 In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled high.

2 PWM pin usage:

In all cases, a "0" on the PWM pin will turn-off both $GATE_A$ and $GATE_B$ outputs. When PWM rises back to "1", $GATE_A$ or $GATE_B$ turn on again depending on the input pin state.

3.2 Fault conditions

In case of a fault conditions the $DIAG_X/EN_X$ pin is considered as an output pin by the device. The fault conditions are:

- overtemperature on one or both high-sides;
- short to battery condition on the output (saturation detection on the external connected Power MOSFET).

Possible origins of fault conditions may be:

- OUT_A is shorted to ground ---> overtemperature detection on high-side A.
- OUT_A is shorted to V_{CC} ---> external Power MOSFET saturation detection (driven by $GATE_A$).

When a fault condition is detected, the user can know which power element is in fault by monitoring the IN_A, IN_B, $DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins.

In any case, when a fault is detected, the faulty half bridge is latched off. To turn-on the respective output ($GATE_X$ or OUT_X) again, the input signal must rise from low to high level.

Table 12. Truth table in fault conditions (detected on OUT_A)

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	$GATE_A$	$GATE_B$
1	1	0	1	Open	H	L	L
1	0	0	1	Open	Open	L	L
0	1	0	1	Open	H	L	L
0	0	0	1	Open	Open	L	L
X	X	0	0	Open	Open	L	L
1	X	0	0	Open	Open	L	L
0	X	0	0	Open	Open	L	L
X	1	0	1	Open	H	L	L
X	0	0	1	Open	Open	L	L

3.3 Test mode

The PWM pin allows to test the load connection between two half-bridges. In the test mode (V_{pwm}=-2V) the external Power Mos gate drivers are disabled. The IN_A or IN_B inputs allow to turn-on the high-side A or B, respectively, in order to connect one side of the load at V_{CC} voltage. The check of the voltage on the other side of the load allow to verify the continuity of the load connection. In case of load disconnection the $DIAD_X/EN_X$ pin corresponding to the faulty output is pulled down.

Table 13. Electrical transient requirements

ISO T/R 7637/1 Test pulse	Test level				
	I	II	III	IV	Delays and impedance
1	- 25V(1)	- 50V(1)	- 75V(1)	- 100V(1)	2ms, 10Ω
2	+ 25V(1)	+ 50V(1)	+ 75V(1)	+ 100V(1)	0.2ms, 10Ω
3a	- 25V(1)	- 50V(1)	- 100V(1)	- 150V(1)	0.1µs, 50Ω
3b	+ 25V(1)	+ 50V(1)	+ 75V(1)	+ 100V(1)	0.1µs, 50Ω
4	- 4V(1)	- 5V(1)	- 6V(1)	- 7V(1)	100ms, 0.01Ω
5	+ 26.5V(1)	+ 46.5V(2)	+ 66.5V(2)	+ 86.5V(2)	400ms, 2Ω

1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 9. Waveforms (1)

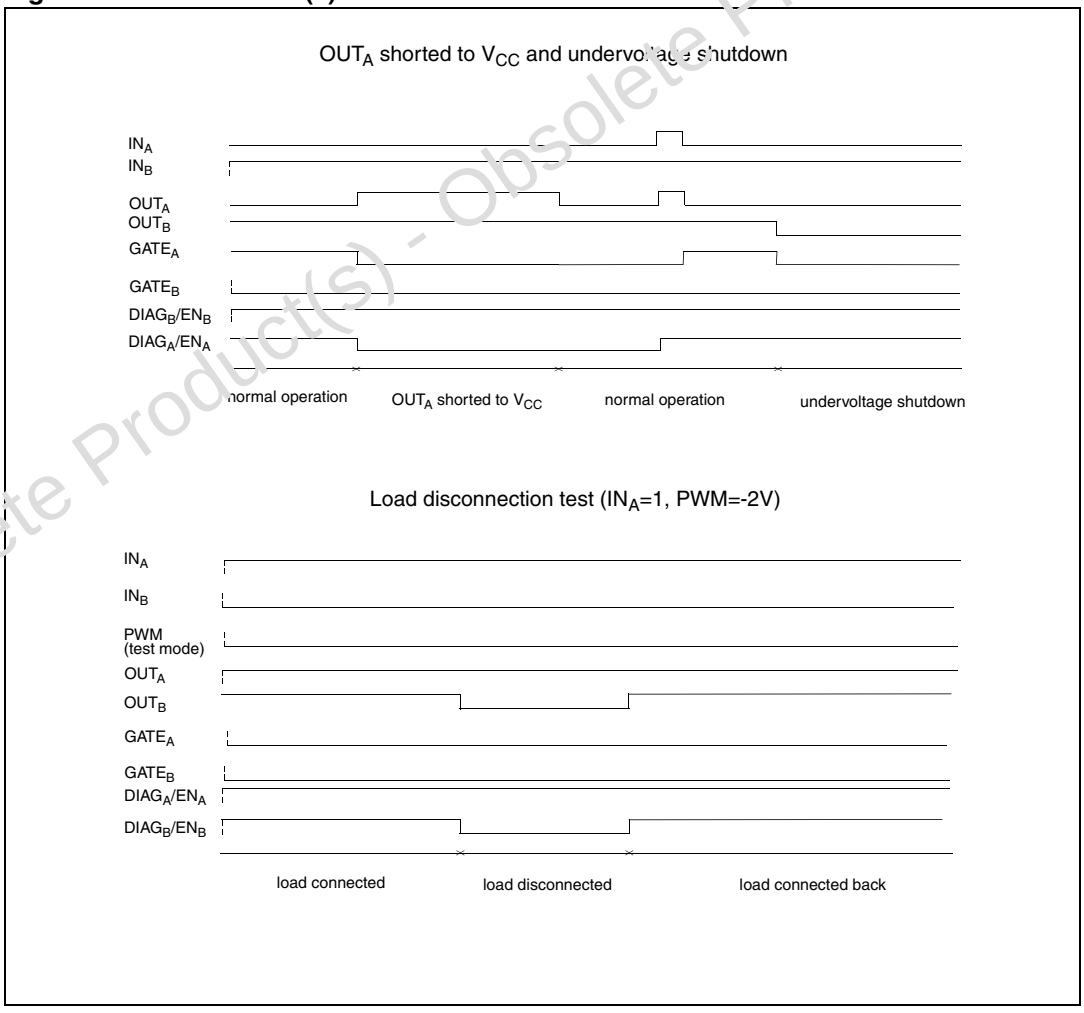
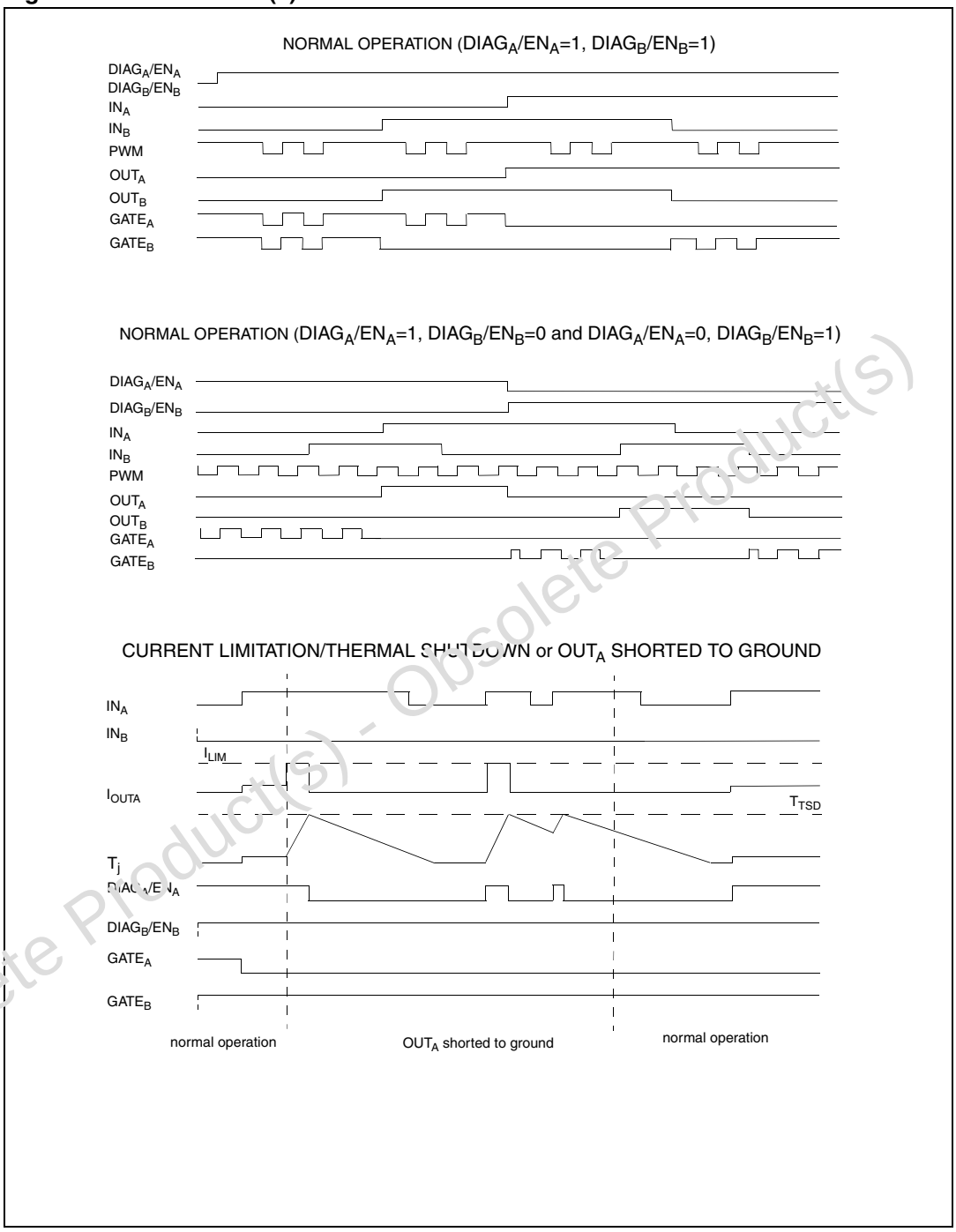


Figure 10. Waveforms (2)



4 Package and packing information

4.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.2 PowerSO-10 mechanical data

Figure 11. PowerSO-10 package dimensions

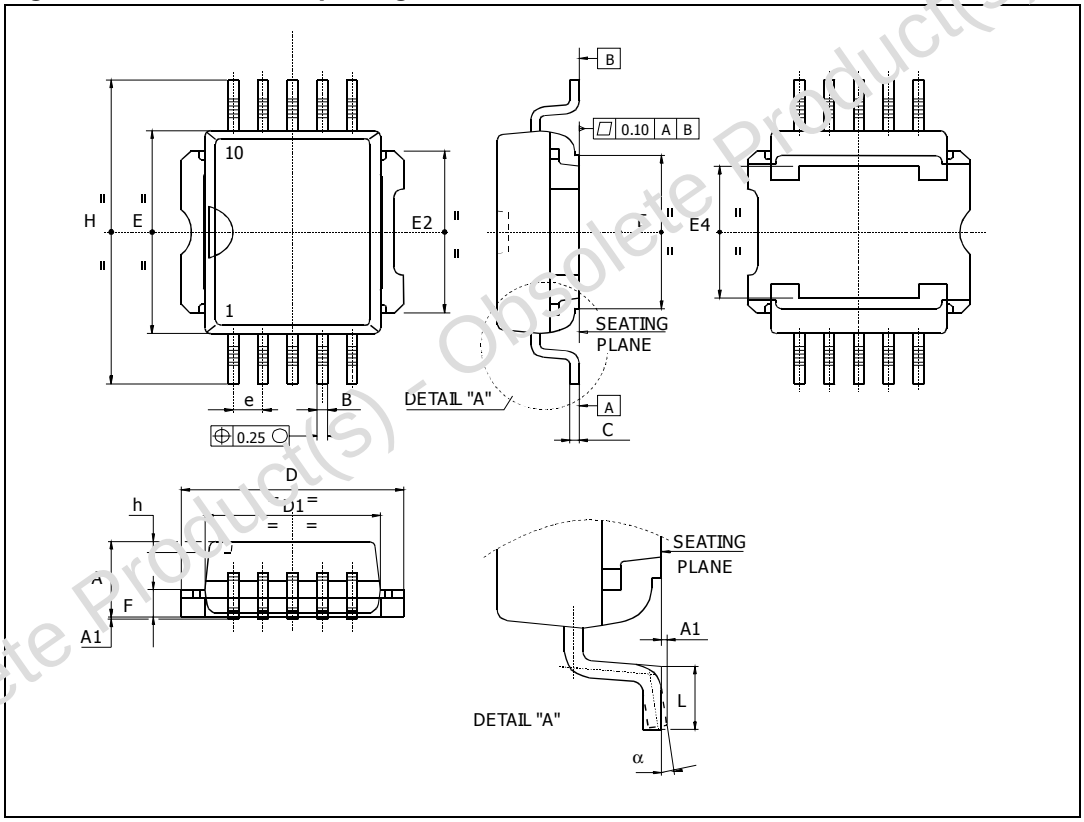


Table 14. PowerSO-10 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	3.35		3.65
A(1)	3.4		3.6
A1	0		0.10
B	0.40		0.60
B(1)	0.37		0.53
C	0.35		0.55
C(1)	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2(1)	7.30		7.50
E4	5.90		6.10
E4(1)	5.90		6.30
e		1.27	
F	1.25		1.35
F(1)	1.20		1.40
H	13.80		14.40
H(1)	13.85		14.35
h		0.50	
L	1.20		1.80
L(1)	0.80		1.10
α	0°		8°
α(1)	2°		8°

1. Muar only POA P013P.

4.3 PowerSO-10 packing information

Figure 12. PowerSO-10 suggested pad layout

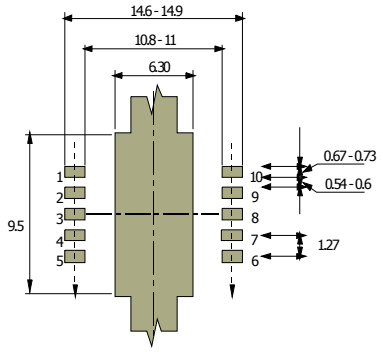
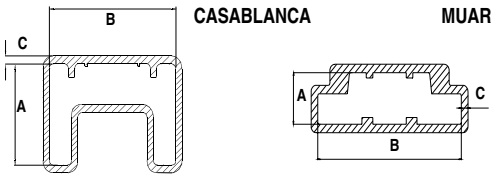


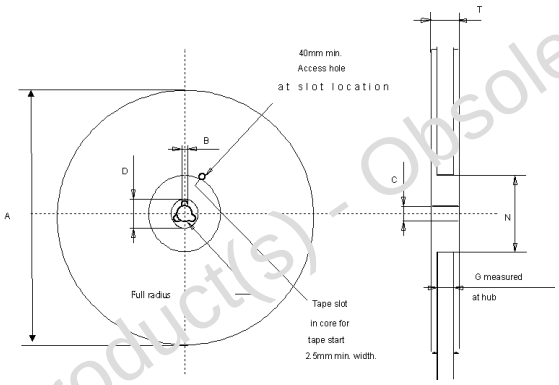
Figure 13. PowerSO-10 tube shipment (no suffix)



All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

Figure 14. PowerSO-10 tape and reel shipment (suffix "TR")



Reel dimensions

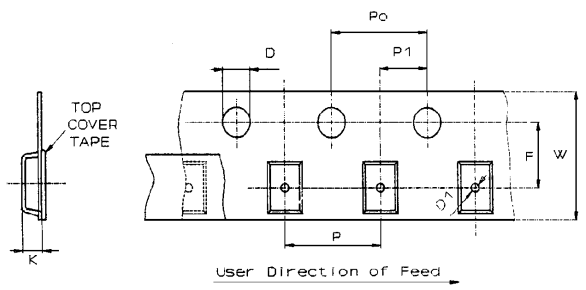
Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

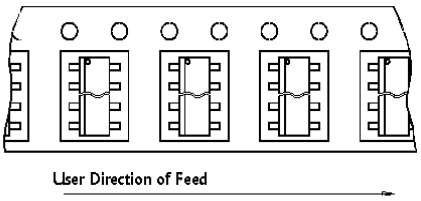
Tape dimensions

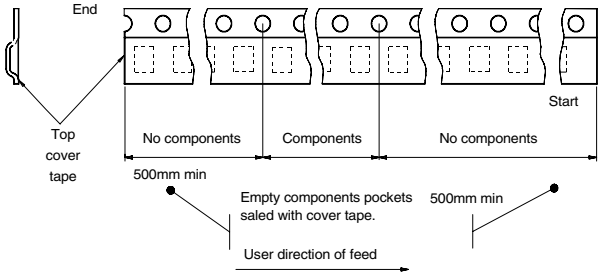
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.







5 Revision history

Table 15. Document revision history

Date	Revision	Changes
03-May-2006	1	Initial release.
11-Dec-2008	2	Document reformatted and restructured. Added contents, list of tables and figures. Added *ECOPACK® packages* information.

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