HIGH-VOLTAGE MONOLITHIC IC

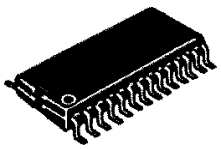
ECN3053F

ECN3053 is a single chip driver IC which has 6 MOS-Gated devices for its output.
It is suitable for controlling 3-phase DC brushless motors and 3-phase induction motors.

Functions

- Lower arm Over current (OC) Protection
- Under voltage Protection
- Fault Output function

Package

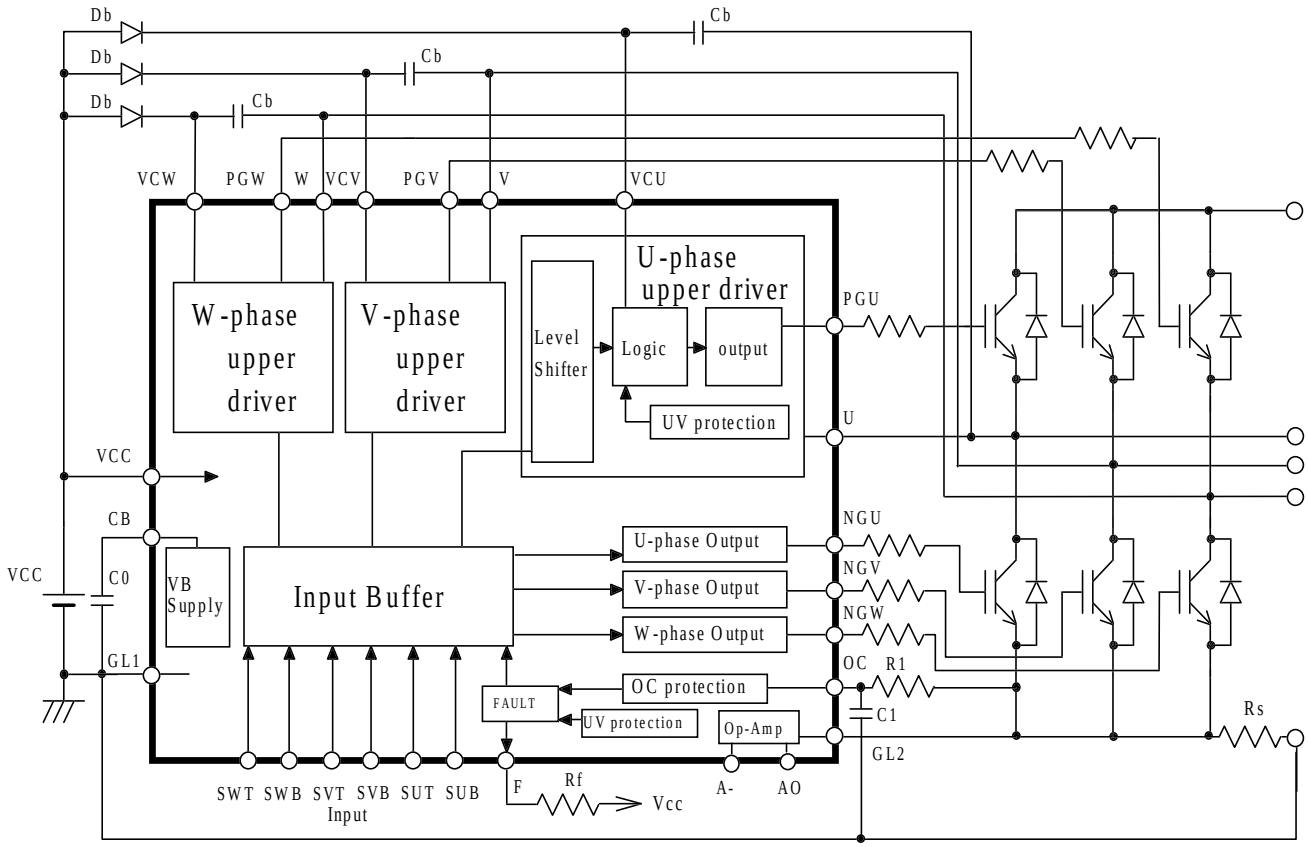


SOP-28

Features

- It can be controlled by PWM with 6 inputs from an external microprocessor.
- 6 logic inputs are compatible with 5V CMOS and LSTTL outputs.

Block Diagram



ECN3053F

1. General

This specification shall be applied to the following semiconductor integrated circuits.

1) Type : ECN3053F
2) Application : 3-phase Brushless Motor, 3-phase Induction Motor
3) Structure : Monolithic IC
4) Package : SOP28

2. Maximum Allowable Ratings (Ta=25°C)

No.	ITEMS	SYMBOLS	UNIT	VALUES	CONDITIONS
1	Output Device Breakdown voltage	Vbv	V	620	Between Vcu,v,w & GL1
2	GL2 terminal voltage	Vgl2	V	-5~Vcc	Vcc=18Vmax at GL2=-5V
3	U,V,W terminal Voltage	Vu,v,w	V	-5~600	
4	Supply voltage	Vcc	V	20	
5	Input voltage	Vin	V	-0.5~Vcc+0.5	
6	Operating Junction Temperature	Tjop	°C	-20~125	
7	Storage Temperature	Tstg	°C	-40~150	

Note 1 : Thermal resistance Rja

PACKAGE	SOP28	Unit
Single	121	°C/W
Mounted	84	°C/W
PCB size,Density *	120x21x1.6 (30%)	mm

* This figure varies depending on the mounting condition.

ECN3053F

3. Electrical Characteristics

Unless otherwise noted, Ta=25 C, Vu,v,w to GL1=374V,Vcc=15V.(suffix T=top, B=bottom arm)

No	ITEMS		SYMBOLS	UNIT	MIN.	TYP.	MAX.	CONDITIONS
1	Stand-by current		Is1	mA	-	6.5	10	Vin=H or L , Between Vcc-GL1
			Is2	µA	-	15	30	Between Vcu-U,Vcv-V,Vcw-W 15V, Vin=H or L
2	Input Voltage (Output is L)		VIH	V	3.5	-	-	Input=H or L
	Input Voltage (Output is H)		VIL	V	-	-	1.5	
3	Output Source Current		Io+	A	0.2	0.25	-	Vcu-PGU,Vcv-PGV, Vcw-PGW =15V, Vcc-NGU,V,W =15V PW<10µs
4	Output Sink Current		Io-	A	0.4	0.5	-	PGU-U,PGV-V, PGW-W =15V, NGU,V,W -GL2=15V PW<10µs
5	High level Output Voltage		VOH	mV	-	-	100	Vcu,v,w-PGU,V, W & Vcc-NGU,V,W Vin=0, Io=0
6	Low level Output Voltage		VOL	mV	-	-	100	PGU,V, W-U,V,W & NGU,V,W -GL2 Vin=5V,Io=0
7	Leakage Current at HV terminal		IL	µA	-	-	50	Vcu,v,w=U,V,W=600V
8	Input Current		IIL	µA	-200	-	-	Vin=0V Internal Pull up R=200kΩ
9	Input Current		IIH	µA	-120	-	-	Vin=5V Internal Pull up R=200kΩ
10	Vcc Under voltage	Negative Going	Vuvb	V	9.5	10.5	11.6	
		Reset Hysterisis	Vrhb	V	0.1	0.4	0.9	
11	Vcu,v,w Under Voltage	Negative Going	Vuvt	V	8.9	10.5	12.1	
		Reset Hysterisis	Vrht	V	0.1	0.4	0.9	
12	OC Input Positive Going threshold		Voc	V	0.44	0.49	0.54	
13	Fault Output On Resistance		Ronf	Ω	-	300	400	F-GL1=0.5V
14	Turn On Delay Time		ton	µs	-	0.8	1.5	CL=1000pF RL=0
15	Turn Off Delay Time		toff	µs	-	0.5	1.2	CL=1000pF RL=0
16	OC Output to Output Shutdown Delay		toc	µs	-	0.7	1.7	CL=1000pF RL=0
17	OC to Fault Delay		tflt	µs	-	0.6	1.6	CL=1000pF RL=0
18	Fault Reset Delay Time		tflrs	µs	6.5	10	20	CL=1000pF RL=0
19	Fault Output terminal Voltage		Vflt	V	-0.5	-	Vcc+0.5	
20	Fault Output Sink Current		Iflt	mA	4	-	-	V(F&GL)=2V
21	VB Output Voltage		VB	V	6.8	7.5	8.2	
22	VB Output Current		IB	mA	25	-	-	Delta Vload=0.1V
23	Op-Amp Input Offset Voltage		Vos	mV	-	-	30	GL2=A-=0.2V
24	Op-Amp High Level Output Voltage		VOHa	V	5.0	7.5	-	A-=0V GL2=1V
25	Op-Amp Low Level Output Voltage		VOLa	mV	-	-	20	A-=1V GL2=0V
26	Op-Amp Output Source Current		Isrca	mA	1.0	-	-	A-=0V GL2=1V AO=4V
27	Op-Amp Output Sink Current		Isnka	mA	1.0	-	-	A-=1V GL2=0V AO=2V

Note 1: Vuvb, Vrhb, Vuvt and Vrht are defined and shown in Fig. 1.

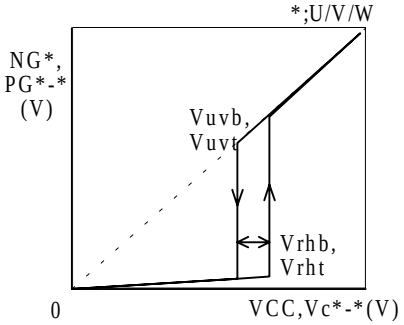


Fig 1. Negative going and reset voltage and hysterisis for the top and bottom arm under voltage circuit

ECN3053F

4. Truth Table

INPUT		OC Input	U phase		V phase		W phase	
			Top arm	Bot.arm	Top arm	Bot.arm	Top arm	Bot.arm
SUT	L	L	ON	-	-	-	-	-
	H		OFF	-	-	-	-	-
SUB	L		-	ON	-	-	-	-
	H		-	OFF	-	-	-	-
SVT	L		-	-	ON	-	-	-
	H		-	-	OFF	-	-	-
SVB	L		-	-	-	ON	-	-
	H		-	-	-	OFF	-	-
SWT	L		-	-	-	-	ON	-
	H		-	-	-	-	OFF	-
SWB	L		-	-	-	-	-	ON
	H		-	-	-	-	-	OFF
-	-	H	OFF	OFF	OFF	OFF	OFF	OFF
SUT,SUB	L	-	OFF	OFF	-	-	-	-
SVT,SVB	L	-	-	-	OFF	OFF	-	-
SWT,SWB	L	-	-	-	-	-	OFF	OFF

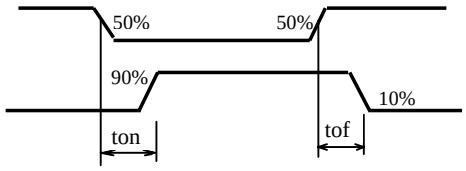
Note 1: Fault output level is referenced Low when over current or under voltage for Vcc is detected.

Note 2: Over current protection works when the voltage drop of the external sensing resistor exceeds the threshold voltage Voc(typical 0.49V). In this case all six outputs are turned off and Fault output level becomes low.
Reset after detection is done by feeding high signal to all six inputs or re-supplying Vcc voltage.

Note 3: The output signal for Fault is reset by feeding high signal to all six inputs.

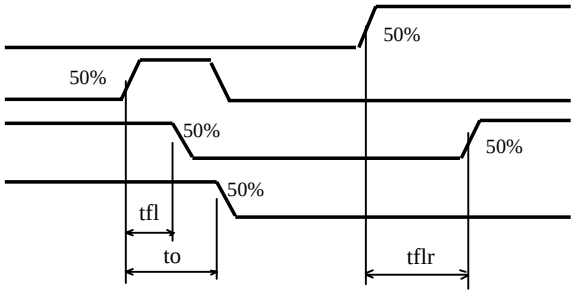
5. Definition of switching delay

Input
(SUB,T, SVB,T, SWB,T)
Output
(PGU,V,W, NGU,V,W)



Input
OC

F
Output
(PGU,V,W NGU,V,W)



ECN3053F

6. Recommended Operating Conditions

No.	ITEMS	SYMBOLS	UNIT	VALUES TOL.	CONDITIONS
1	Power Supply Voltage	Vcc	V	13.5~16.5	
2	PWM Frequency	fpwm	kHz	1~20	
3	VB Smoothing Capacitor	Co	μF	> 0.22	Stress voltage:VB
4	Boot Strap Capacitor	Cb	μF	3.3	Stress voltage:Vcc
5	Boot Strap Diodes	Db	Hitachi DFG1C6 DFM1F6 or equivalent		600V/1.0A ≦ 0.1μs
6	Sensing Resistor	Rs	Ω	Note 1	
7	OC Filtering Resistor	R1	Ω	Note 2	
8	OC Filtering Capacitor	C1	μF	Note 2	
9	Load resistor for F terminal	Rf	kΩ	≧ 5.6	

Note 1. Over-current detection level is determined by the following equation

Ioc=Voc/Rs

Note.2 This IC has filters of 0.4us for noise reduction.

But appropriate R1, C1 should be added when noise can not be removed.

7. Pin Assignment

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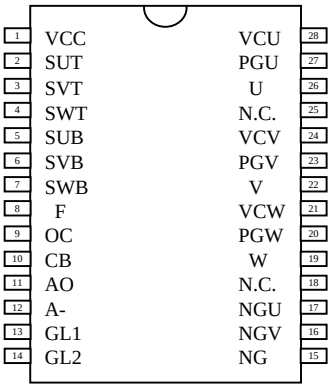

8. Outline Drawing

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