



#### Features

- **In-System Reprogrammable™ (ISR™) CMOS CPLDs**
  - JTAG interface for reconfigurability
  - Design changes do not cause pinout changes
  - Design changes do not cause timing changes
- **High density**
  - 32 to 512 macrocells
  - 32 to 264 I/O pins
  - Five dedicated inputs including four clock pins
- **Simple timing model**
  - No fanout delays
  - No expander delays
  - No dedicated vs. I/O pin delays
  - No additional delay through PIM
  - No penalty for using full 16 product terms
  - No delay for steering or sharing product terms
- **3.3V and 5V versions**
- **PCI-compatible<sup>[1]</sup>**
- **Programmable bus-hold capabilities on all I/Os**
- **Intelligent product term allocator provides:**
  - 0 to 16 product terms to any macrocell
  - Product term steering on an individual basis
  - Product term sharing among local macrocells
- **Flexible clocking**
  - Four synchronous clocks per device
  - Product term clocking
  - Clock polarity control per logic block
- **Consistent package/pinout offering across all densities**
  - Simplifies design migration
  - Same pinout for 3.3V and 5.0V devices
- **Packages**
  - 44 to 400 leads in PLCC, CLCC, PQFP, TQFP, CQFP, BGA, and Fine-Pitch BGA packages

#### Note:

1. Due to the 5V-tolerant nature of 3.3V device I/Os, the I/Os are not clamped to  $V_{CC}$ ,  $PCI V_{IH} = 2V$ .

#### General Description

The Ultra37000™ family of CMOS CPLDs provides a range of high-density programmable logic solutions with unparalleled system performance. The Ultra37000 family is designed to bring the flexibility, ease of use, and performance of the 22V10 to high-density CPLDs. The architecture is based on a number of logic blocks that are connected by a Programmable Interconnect Matrix (PIM). Each logic block features its own product term array, product term allocator, and 16 macrocells. The PIM distributes signals from the logic block outputs and all input pins to the logic block inputs.

All of the Ultra37000 devices are electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The ISR feature provides the ability to reconfigure the devices without having design changes cause pinout or timing changes. The Cypress ISR function is implemented through a JTAG-compliant serial interface. Data is shifted in and out through the TDI and TDO pins, respectively. Because of the superior routability and simple timing model of the Ultra37000 devices, ISR allows users to change existing logic designs while simultaneously fixing pinout assignments and maintaining system performance.

The entire family features JTAG for ISR and boundary scan, and is compatible with the PCI Local Bus specification, meeting the electrical and timing requirements. The Ultra37000 family features user programmable bus-hold capabilities on all I/Os.

#### Ultra37000 5.0V Devices

The Ultra37000 devices operate with a 5V supply and can support 5V or 3.3V I/O levels.  $V_{CCO}$  connections provide the capability of interfacing to either a 5V or 3.3V bus. By connecting the  $V_{CCO}$  pins to 5V the user insures 5V TTL levels on the outputs. If  $V_{CCO}$  is connected to 3.3V the output levels meet 3.3V JEDEC standard CMOS levels and are 5V tolerant. These devices require 5V ISR programming.

#### Ultra37000V 3.3V Devices

Devices operating with a 3.3V supply require 3.3V on all  $V_{CCO}$  pins, reducing the device's power consumption. These devices support 3.3V JEDEC standard CMOS output levels, and are 5V-tolerant. These devices allow 3.3V ISR programming.



## Selection Guide

### 5.0V Selection Guide

#### General Information

| Device  | Macrocells | Dedicated Inputs | I/O Pins    | Speed (t <sub>PD</sub> ) | Speed (f <sub>MAX</sub> ) |
|---------|------------|------------------|-------------|--------------------------|---------------------------|
| CY37032 | 32         | 5                | 32          | 6                        | 200                       |
| CY37064 | 64         | 5                | 32/64       | 6                        | 200                       |
| CY37128 | 128        | 5                | 64/128      | 6.5                      | 167                       |
| CY37192 | 192        | 5                | 120         | 7.5                      | 154                       |
| CY37256 | 256        | 5                | 128/160/192 | 7.5                      | 154                       |
| CY37384 | 384        | 5                | 160/192     | 10                       | 118                       |
| CY37512 | 512        | 5                | 160/192/264 | 10                       | 118                       |

#### Speed Bins

| Device  | 200 | 167 | 154 | 143 | 125 | 100 | 83 | 66 |
|---------|-----|-----|-----|-----|-----|-----|----|----|
| CY37032 | X   |     | X   |     | X   |     |    |    |
| CY37064 | X   |     | X   |     | X   |     |    |    |
| CY37128 |     | X   |     |     | X   | X   |    |    |
| CY37192 |     |     | X   |     | X   |     | X  |    |
| CY37256 |     |     | X   |     | X   |     | X  |    |
| CY37384 |     |     |     |     | X   |     | X  |    |
| CY37512 |     |     |     |     | X   | X   | X  |    |

#### Device-Package Offering and I/O Count

| Device  | 44-Lead TQFP | 44-Lead PLCC | 44-Lead CLCC | 84-Lead PLCC | 84-Lead CLCC | 100-Lead TQFP | 160-Lead TQFP | 160-Lead CQFP | 208-Lead PQFP | 208-Lead CQFP | 256-Lead BGA | 352-Lead BGA |
|---------|--------------|--------------|--------------|--------------|--------------|---------------|---------------|---------------|---------------|---------------|--------------|--------------|
| CY37032 | 37           | 37           |              |              |              |               |               |               |               |               |              |              |
| CY37064 | 37           | 37           | 37           | 69           |              | 69            |               |               |               |               |              |              |
| CY37128 |              |              |              | 69           | 69           | 69            | 133           |               |               |               |              |              |
| CY37192 |              |              |              |              |              |               | 125           |               |               |               |              |              |
| CY37256 |              |              |              |              |              |               | 133           | 133           | 165           |               | 197          |              |
| CY37384 |              |              |              |              |              |               |               |               | 165           |               | 197          |              |
| CY37512 |              |              |              |              |              |               |               |               | 165           | 165           | 197          | 269          |

### 3.3V Selection Guide

#### General Information

| Device   | Macrocells | Dedicated Inputs | I/O Pins    | Speed (t <sub>PD</sub> ) | Speed (f <sub>MAX</sub> ) |
|----------|------------|------------------|-------------|--------------------------|---------------------------|
| CY37032V | 32         | 5                | 32          | 8.5                      | 143                       |
| CY37064V | 64         | 5                | 32/64       | 8.5                      | 143                       |
| CY37128V | 128        | 5                | 64/80/128   | 10                       | 125                       |
| CY37192V | 192        | 5                | 120         | 12                       | 100                       |
| CY37256V | 256        | 5                | 128/160/192 | 12                       | 100                       |
| CY37384V | 384        | 5                | 160/192     | 15                       | 83                        |
| CY37512V | 512        | 5                | 160/192/264 | 15                       | 83                        |

## Speed Bins

| Device   | 200 | 167 | 154 | 143 | 125 | 100 | 83 | 66 |
|----------|-----|-----|-----|-----|-----|-----|----|----|
| CY37032V |     |     |     | X   |     | X   |    |    |
| CY37064V |     |     |     | X   |     | X   |    |    |
| CY37128V |     |     |     |     | X   |     | X  |    |
| CY37192V |     |     |     |     |     | X   |    | X  |
| CY37256V |     |     |     |     |     | X   |    | X  |
| CY37384V |     |     |     |     |     |     | X  | X  |
| CY37512V |     |     |     |     |     |     | X  | X  |

## Device-Package Offering & I/O Count

| Device   | 44-Lead<br>TQFP | 44-Lead<br>CLCC | 48-Lead<br>FBGA | 84-Lead<br>CLCC | 100-Lead<br>TQFP | 100-Lead<br>FBGA | 160-Lead<br>TQFP | 160-Lead<br>CQFP | 208-Lead<br>PQFP | 208-Lead<br>CQFP | 256-Lead<br>BGA | 256-Lead<br>FBGA | 352-Lead<br>BGA | 400-Lead<br>FBGA |
|----------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|------------------|------------------|------------------|------------------|-----------------|------------------|-----------------|------------------|
| CY37032V | 37              |                 | 37              |                 |                  |                  |                  |                  |                  |                  |                 |                  |                 |                  |
| CY37064V | 37              | 37              | 37              |                 | 69               | 69               |                  |                  |                  |                  |                 |                  |                 |                  |
| CY37128V |                 |                 |                 | 69              | 69               | 85               | 133              |                  |                  |                  |                 |                  |                 |                  |
| CY37192V |                 |                 |                 |                 |                  |                  | 125              |                  |                  |                  |                 |                  |                 |                  |
| CY37256V |                 |                 |                 |                 |                  |                  | 133              | 133              | 165              |                  | 197             | 197              |                 |                  |
| CY37384V |                 |                 |                 |                 |                  |                  |                  |                  | 165              |                  | 197             |                  |                 |                  |
| CY37512V |                 |                 |                 |                 |                  |                  |                  |                  | 165              | 165              | 197             |                  | 269             | 269              |

## Architecture Overview of Ultra37000 Family

### Programmable Interconnect Matrix

The PIM consists of a completely global routing matrix for signals from I/O pins and feedbacks from the logic blocks. The PIM provides extremely robust interconnection to avoid fitting and density limitations.

The inputs to the PIM consist of all I/O and dedicated input pins and all macrocell feedbacks from within the logic blocks. The number of PIM inputs increases with pin count and the number of logic blocks. The outputs from the PIM are signals routed to the appropriate logic blocks. Each logic block receives 36 inputs from the PIM and their complements, allowing for 32-bit operations to be implemented in a single pass through the device. The wide number of inputs to the logic block also improves the routing capacity of the Ultra37000 family.

An important feature of the PIM is its simple timing. The propagation delay through the PIM is accounted for in the timing specifications for each device. There is no additional delay for traveling through the PIM. In fact, all inputs travel through the PIM. As a result, there are no route-dependent timing parameters on the Ultra37000 devices. The worst-case PIM delays are incorporated in all appropriate Ultra37000 specifications.

Routing signals through the PIM is completely invisible to the user. All routing is accomplished by software—no hand routing is necessary. *Warp*<sup>®</sup> and third-party development packages automatically route designs for the Ultra37000 family in a matter of minutes. Finally, the rich routing resources of the Ultra37000 family accommodate last minute logic changes while maintaining fixed pin assignments.

### Logic Block

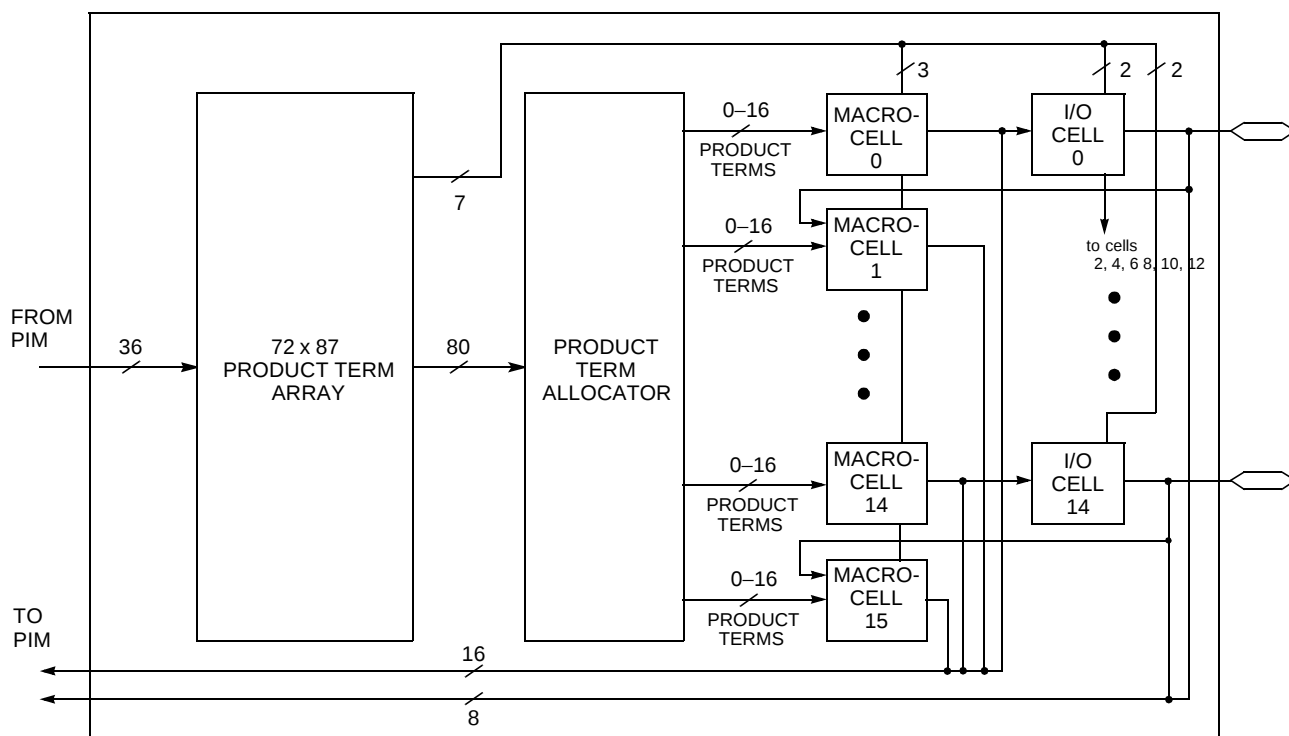
The logic block is the basic building block of the Ultra37000 architecture. It consists of a product term array, an intelligent product-term allocator, 16 macrocells, and a number of I/O cells. The number of I/O cells varies depending on the device used. Refer to *Figure 1* for the block diagram.

### Product Term Array

Each logic block features a 72 x 87 programmable product term array. This array accepts 36 inputs from the PIM, which originate from macrocell feedbacks and device pins. Active LOW and active HIGH versions of each of these inputs are generated to create the full 72-input field. The 87 product terms in the array can be created from any of the 72 inputs.

Of the 87 product terms, 80 are for general-purpose use for the 16 macrocells in the logic block. Four of the remaining seven product terms in the logic block are output enable (OE) product terms. Each of the OE product terms controls up to eight of the 16 macrocells and is selectable on an individual macrocell basis. In other words, each I/O cell can select between one of two OE product terms to control the output buffer. The first two of these four OE product terms are available to the upper half of the I/O macrocells in a logic block. The other two OE product terms are available to the lower half of the I/O macrocells in a logic block.

The next two product terms in each logic block are dedicated asynchronous set and asynchronous reset product terms. The final product term is the product term clock. The set, reset, OE and product term clock have polarity control to realize OR functions in a single pass through the array.



**Figure 1. Logic Block with 50% Buried Macrocells**

#### *Low-Power Option*

Each logic block can operate in high-speed mode for critical path performance, or in low-power mode for power conservation. The logic block mode is set by the user on a logic block by logic block basis.

#### **Product Term Allocator**

Through the product term allocator, software automatically distributes product terms among the 16 macrocells in the logic block as needed. A total of 80 product terms are available from the local product term array. The product term allocator provides two important capabilities without affecting performance: product term steering and product term sharing.

#### *Product Term Steering*

Product term steering is the process of assigning product terms to macrocells as needed. For example, if one macrocell requires ten product terms while another needs just three, the product term allocator will “steer” ten product terms to one macrocell and three to the other. On Ultra37000 devices, product terms are steered on an individual basis. Any number between 0 and 16 product terms can be steered to any macrocell. Note that 0 product terms is useful in cases where a particular macrocell is unused or used as an input register.

#### *Product Term Sharing*

Product term sharing is the process of using the same product term among multiple macrocells. For example, if more than one output has one or more product terms in its equation that are common to other outputs, those product terms are only programmed once. The Ultra37000 product term allocator allows sharing across groups of four output macrocells in a

variable fashion. The software automatically takes advantage of this capability—the user does not have to intervene.

Note that neither product term sharing nor product term steering have any effect on the speed of the product. All worst-case steering and sharing configurations have been incorporated in the timing specifications for the Ultra37000 devices.

#### **Ultra37000 Macrocell**

Within each logic block there are 16 macrocells. Macrocells can either be I/O Macrocells, which include an I/O Cell which is associated with an I/O pin, or buried Macrocells, which do not connect to an I/O. The combination of I/O Macrocells and buried Macrocells varies from device to device.

#### *Buried Macrocell*

Figure 2 displays the architecture of buried macrocells. The buried macrocell features a register that can be configured as combinatorial, a D flip-flop, a T flip-flop, or a level-triggered latch.

The register can be asynchronously set or asynchronously reset at the logic block level with the separate set and reset product terms. Each of these product terms features programmable polarity. This allows the registers to be set or reset based on an AND expression or an OR expression.

Clocking of the register is very flexible. Four global synchronous clocks and a product term clock are available to clock the register. Furthermore, each clock features programmable polarity so that registers can be triggered on falling as well as rising edges (see the Clocking section). Clock polarity is chosen at the logic block level.

The buried macrocell also supports input register capability. The buried macrocell can be configured to act as an input register (D-type or latch) whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

### *I/O Macrocell*

Figure 2 illustrates the architecture of the I/O macrocell. The I/O macrocell supports the same functions as the buried macrocell with the addition of I/O capability. At the output of the macrocell, a polarity control mux is available to select active LOW or active HIGH signals. This has the added advantage of allowing significant logic reduction to occur in many applications.

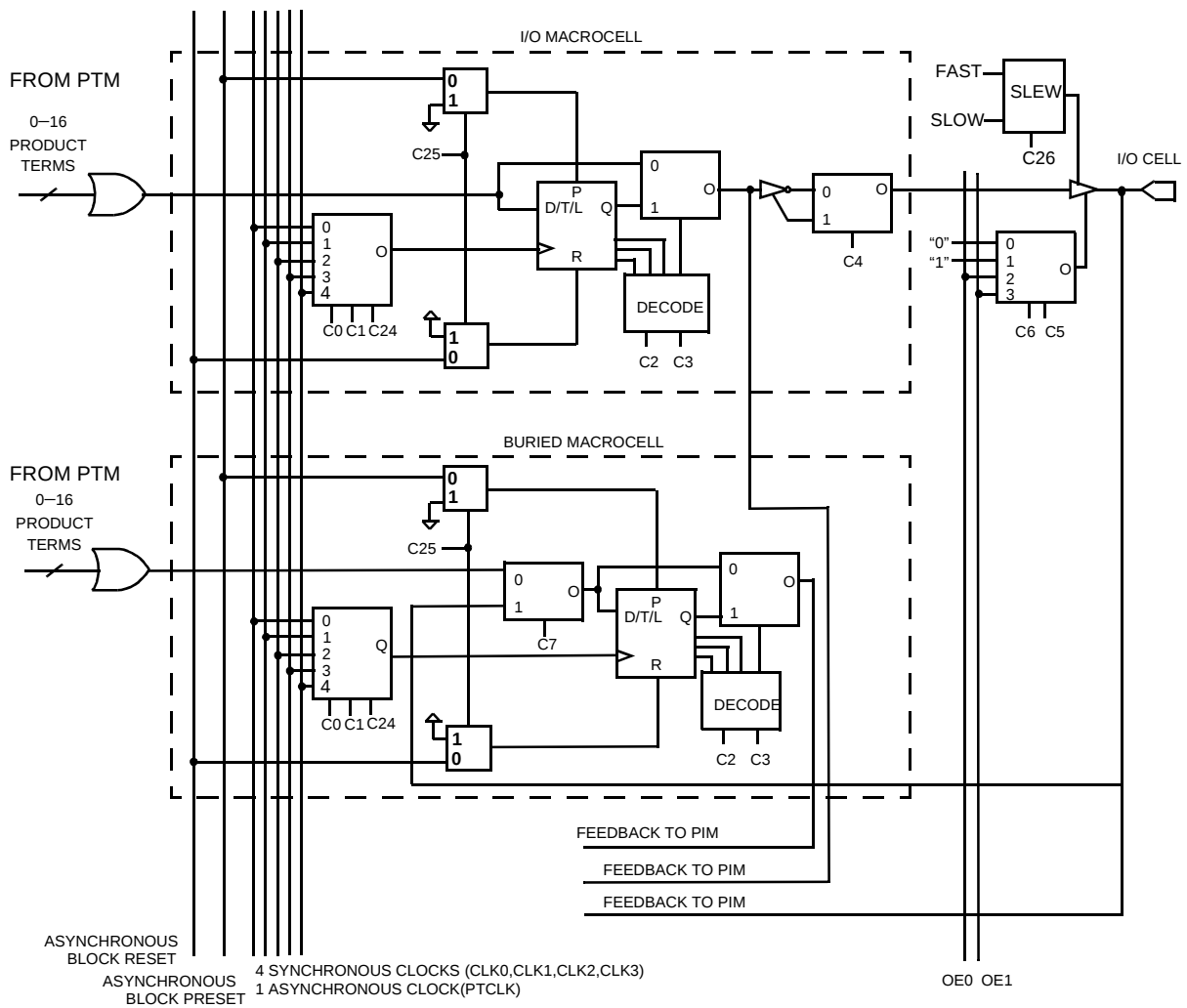
The Ultra37000 macrocell features a feedback path to the PIM separate from the I/O pin input path. This means that if the macrocell is buried (fed back internally only), the associated I/O pin can still be used as an input.

### *Bus Hold Capabilities on all I/Os*

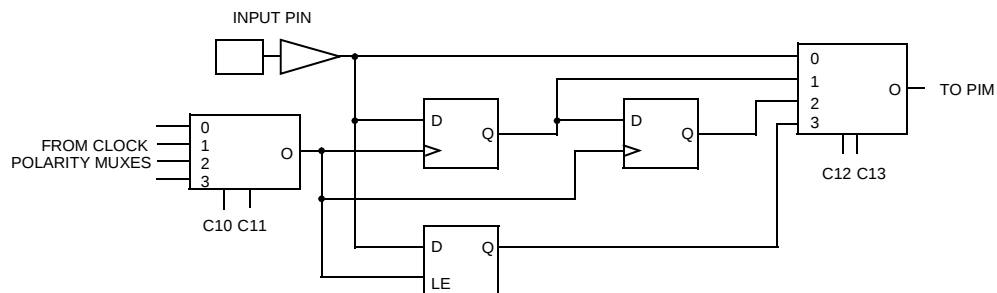
Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold maintains the last state of a pin when the pin is placed in a high-impedance state, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to  $V_{CC}$  or GND. For more information, see the application note "Understanding Bus-Hold — A Feature of Cypress CPLDs."

### *Programmable Slew Rate Control*

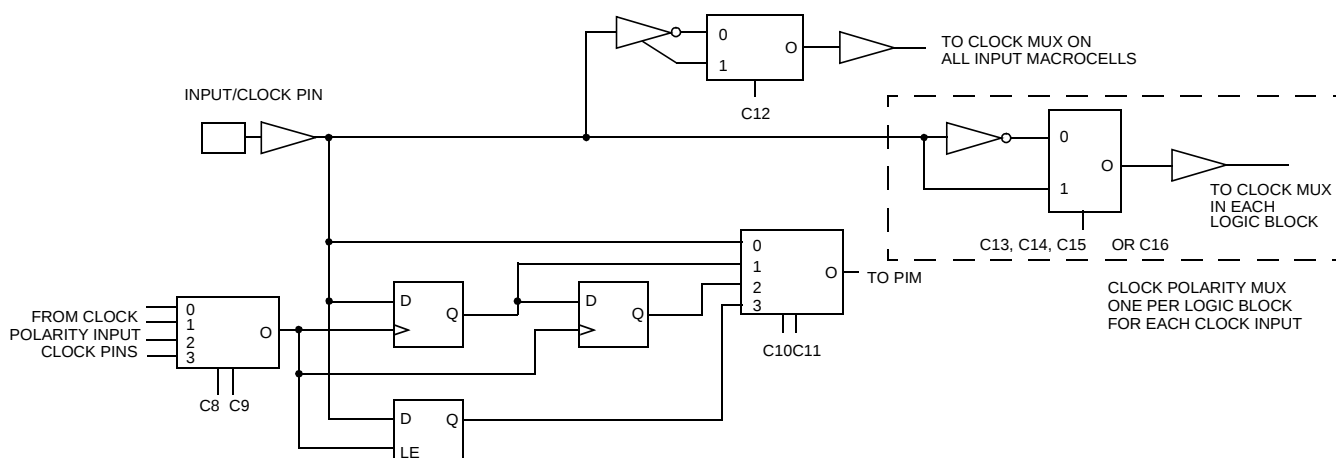
Each output has a programmable configuration bit, which sets the output slew rate to fast or slow. For designs concerned with meeting FCC emissions standards the slow edge provides for lower system noise. For designs requiring very high performance the fast edge rate provides maximum system performance.



**Figure 2. I/O and Buried Macrocells**



**Figure 3. Input Macrocell**



**Figure 4. Input/Clock Macrocell**

## Clocking

Each I/O and buried macrocell has access to four synchronous clocks (CLK0, CLK1, CLK2 and CLK3) as well as an asynchronous product term clock PTCLK. Each input macrocell has access to all four synchronous clocks.

### Dedicated Inputs/Clocks

Five pins on each member of the Ultra37000 family are designated as input-only. There are two types of dedicated inputs on Ultra37000 devices: input pins and input/clock pins. *Figure 3* illustrates the architecture for input pins. Four input options are available for the user: combinatorial, registered, double-registered, or latched. If a registered or latched option is selected, any one of the input clocks can be selected for control.

Figure 4 illustrates the architecture for the input/clock pins. Like the input pins, input/clock pins can be combinatorial, registered, double-registered, or latched. In addition, these pins feed the clocking structures throughout the device. The clock path at the input has user-configurable polarity.

### Product Term Clocking

In addition to the four synchronous clocks, the Ultra37000 family also has a product term clock for asynchronous clocking. Each logic block has an independent product term clock which is available to all 16 macrocells. Each product term clock also supports user configurable polarity selection.

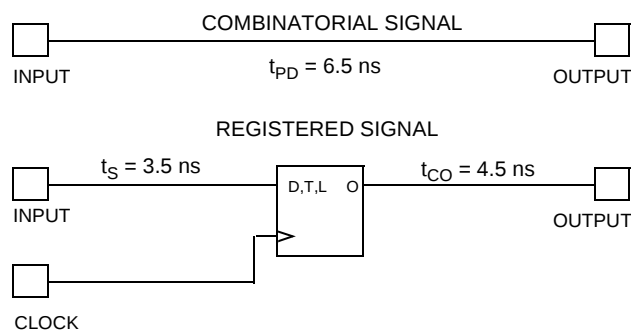
## Timing Model

One of the most important features of the Ultra37000 family is the simplicity of its timing. All delays are worst case and system performance is unaffected by the features used. *Figure 5* illustrates the true timing model for the 167-MHz devices in high speed mode. For combinatorial paths, any input to any output incurs a 6.5-ns worst-case delay regardless of the amount of logic used. For synchronous systems, the input set-up time to the output macrocells for any input is 3.5 ns and the clock to output time is also 4.0 ns. These measurements are for any output and synchronous clock, regardless of the logic used.

The Ultra37000 features:

- No fanout delays
- No expander delays
- No dedicated vs. I/O pin delays
- No additional delay through PIM
- No penalty for using 0–16 product terms
- No added delay for steering product terms
- No added delay for sharing product terms
- No routing delays
- No output bypass delays

The simple timing model of the Ultra37000 family eliminates unexpected performance penalties.



### Figure 5. Timing Model for CY37128

## JTAG and PCI Standards

## PCI Compliance

5V operation of the Ultra37000 is fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The 3.3V products meet all PCI requirements except for the output 3.3V clamp, which is in direct conflict with 5V tolerance. The Ultra37000 family's simple and predictable timing model ensures compliance with the PCI AC specifications independent of the design.

## IEEE 1149.1-compliant JTAG

The Ultra37000 family has an IEEE 1149.1 JTAG interface for both Boundary Scan and ISR.

### Boundary Scan

The Ultra37000 family supports Bypass, Sample/Preload, Extest, Idcode, and Usercode boundary scan instructions. The JTAG interface is shown in Figure 6.

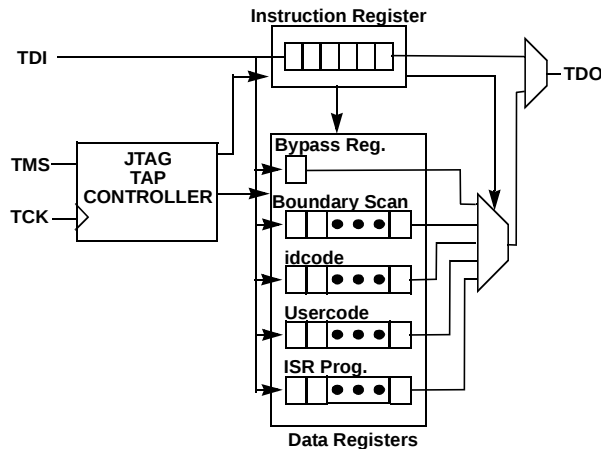


Figure 6. JTAG Interface

### In-System Reprogramming (ISR)

In-System Reprogramming is the combination of the capability to program or reprogram a device on-board, and the ability to support design changes without changing the system timing or device pinout. This combination means design changes during debug or field upgrades do not cause board respins. The Ultra37000 family implements ISR by providing a JTAG compliant interface for on-board programming, robust routing resources for pinout flexibility, and a simple timing model for consistent system performance.

## Development Software Support

### Warp

Warp is a state-of-the-art compiler and complete CPLD design tool. For design entry, Warp provides an IEEE-STD-1076/1164 VHDL text editor, an IEEE-STD-1364 Verilog text editor, and a graphical finite state machine editor. It provides optimized synthesis and fitting by replacing basic circuits with ones pre-optimized for the target device, by implementing logic in unused memory and by perfect communication between fitting and synthesis. To facilitate design and debugging, Warp provides graphical timing simulation and analysis.

### Warp Professional™

Warp Professional contains several additional features. It provides an extra method of design entry with its graphical block diagram editor. It allows up to 5 ms timing simulation instead of only 2 ms. It allows comparison of waveforms before and after design changes.

### Warp Enterprise™

Warp Enterprise provides even more features. It provides unlimited timing simulation and source-level behavioral simulation as well as a debugger. It has the ability to generate graphical HDL blocks from HDL text. It can even generate testbenches.

Warp is available for PC and UNIX platforms. Some features are not available in the UNIX version. For further information see the Warp for PC, Warp for UNIX, Warp Professional and Warp Enterprise data sheets on Cypress's web site ([www.cypress.com](http://www.cypress.com)).

### Third-Party Software

Although Warp is a complete CPLD development tool on its own, it interfaces with nearly every third party EDA tool. All major third-party software vendors provide support for the Ultra37000 family of devices. Refer to the third-party software data sheet or contact your local sales office for a list of currently supported third-party vendors.

### Programming

There are four programming options available for Ultra37000 devices. The first method is to use a PC with the 37000 UltraISR programming cable and software. With this method, the ISR pins of the Ultra37000 devices are routed to a connector at the edge of the printed circuit board. The 37000 UltraISR programming cable is then connected between the parallel port of the PC and this connector. A simple configuration file instructs the ISR software of the programming operations to be performed on each of the Ultra37000 devices in the system. The ISR software then automatically completes all of the necessary data manipulations required to accomplish the programming, reading, verifying, and other ISR functions. For more information on the Cypress ISR Interface, see the ISR Programming Kit data sheet (CY3700i).

The second method for programming Ultra37000 devices is on automatic test equipment (ATE). This is accomplished through a file created by the ISR software. Check the Cypress website for the latest ISR software download information.

The third programming option for Ultra37000 devices is to utilize the embedded controller or processor that already exists in the system. The Ultra37000 ISR software assists in this method by converting the device JEDEC maps into the ISR serial stream that contains the ISR instruction information and the addresses and data of locations to be programmed. The embedded controller then simply directs this ISR stream to the chain of Ultra37000 devices to complete the desired reconfiguring or diagnostic operations. Contact your local sales office for information on availability of this option.

The fourth method for programming Ultra37000 devices is to use the same programmer that is currently being used to program FLASH370i devices.

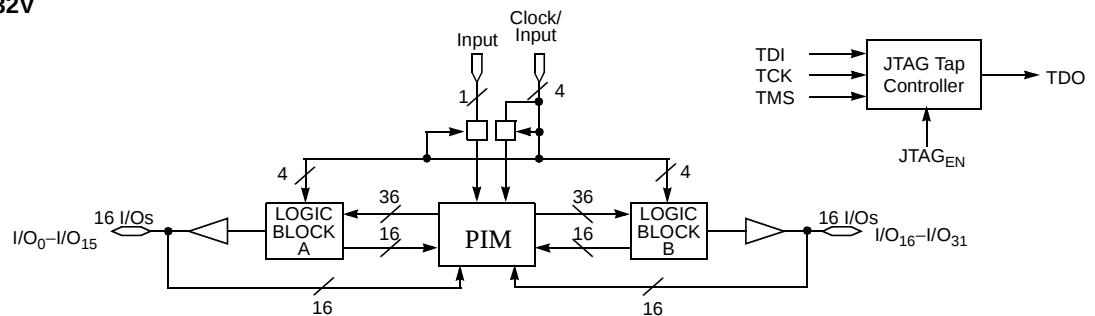
For all pinout, electrical, and timing requirements, refer to device data sheets. For ISR cable and software specifications, refer to the UltraISR kit data sheet (CY3700i).

### Third-Party Programmers

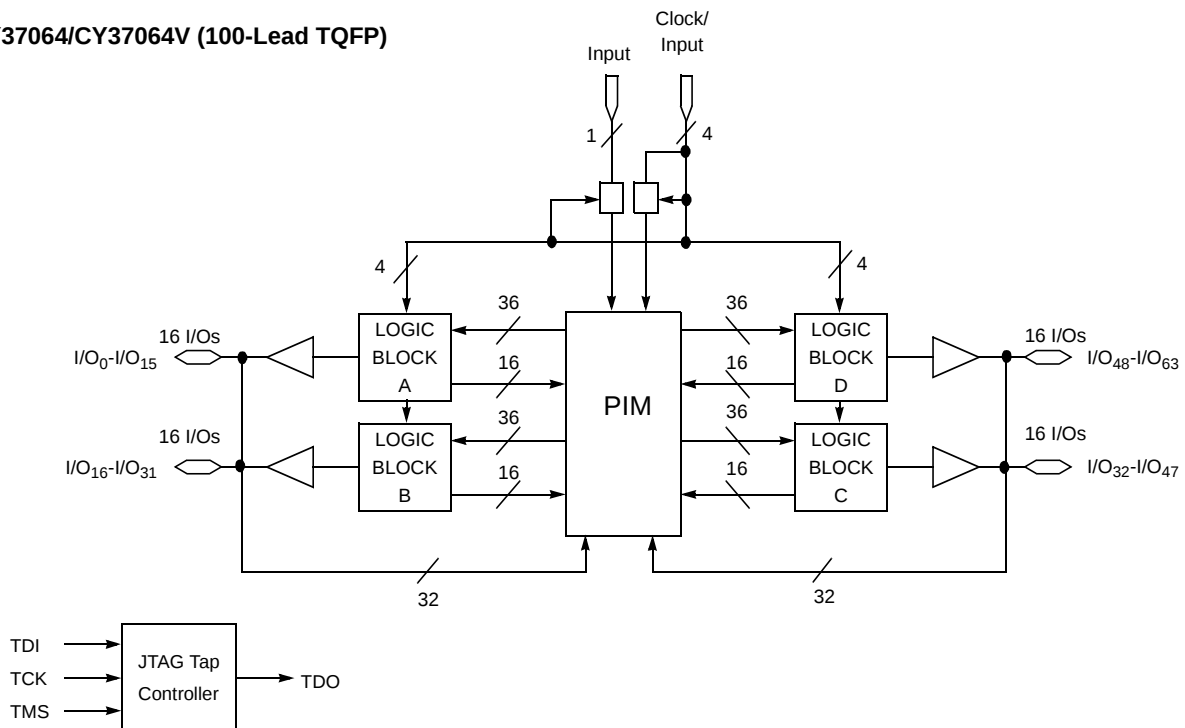
As with development software, Cypress support is available on a wide variety of third-party programmers. All major third-party programmers (including BP Micro, Data I/O, and SMS) support the Ultra37000 family.

## Logic Block Diagrams

### CY37032/CY37032V

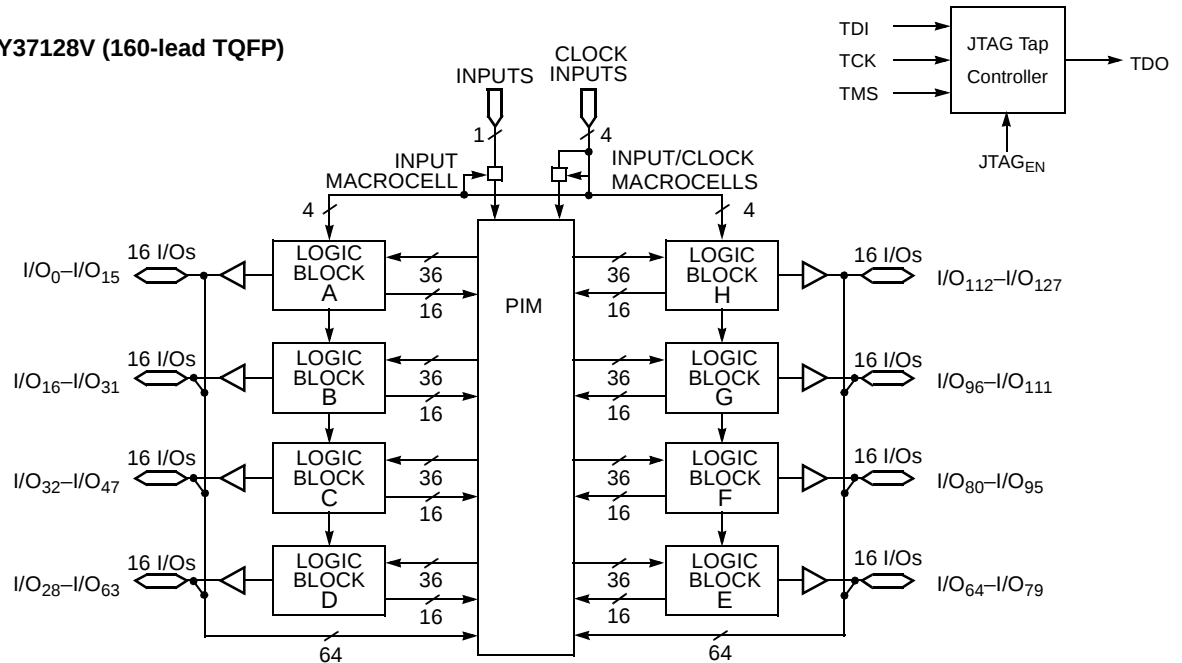


### CY37064/CY37064V (100-Lead TQFP)

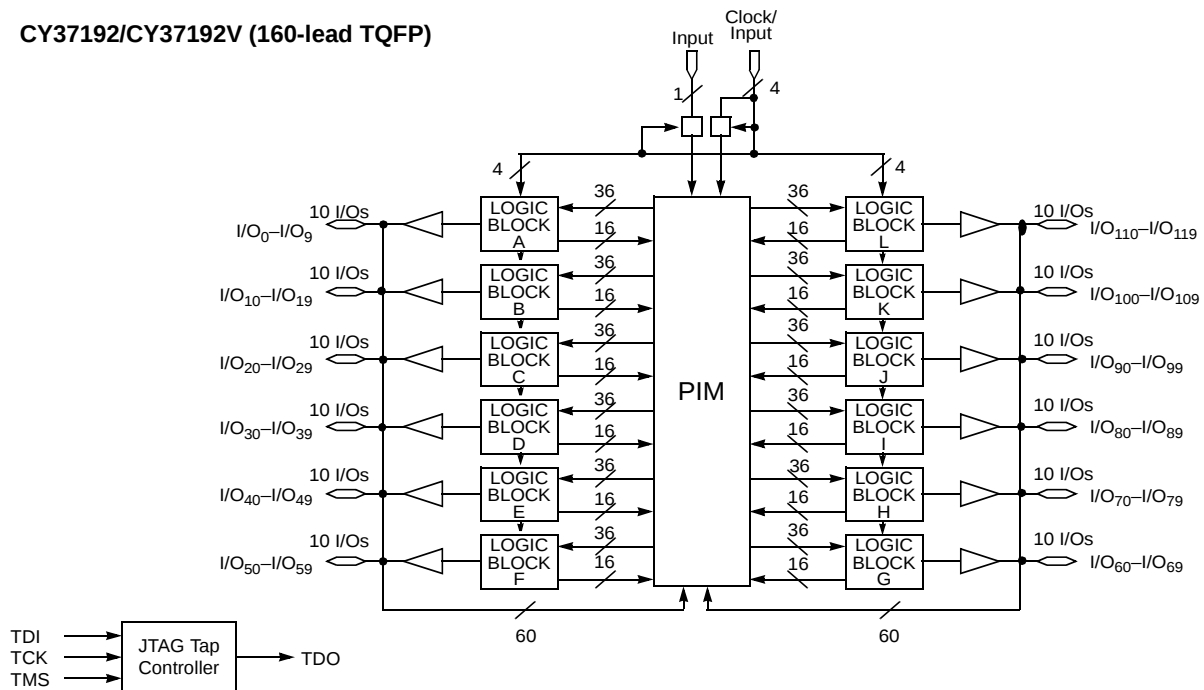


## Logic Block Diagrams (continued)

**CY37128/CY37128V (160-lead TQFP)**

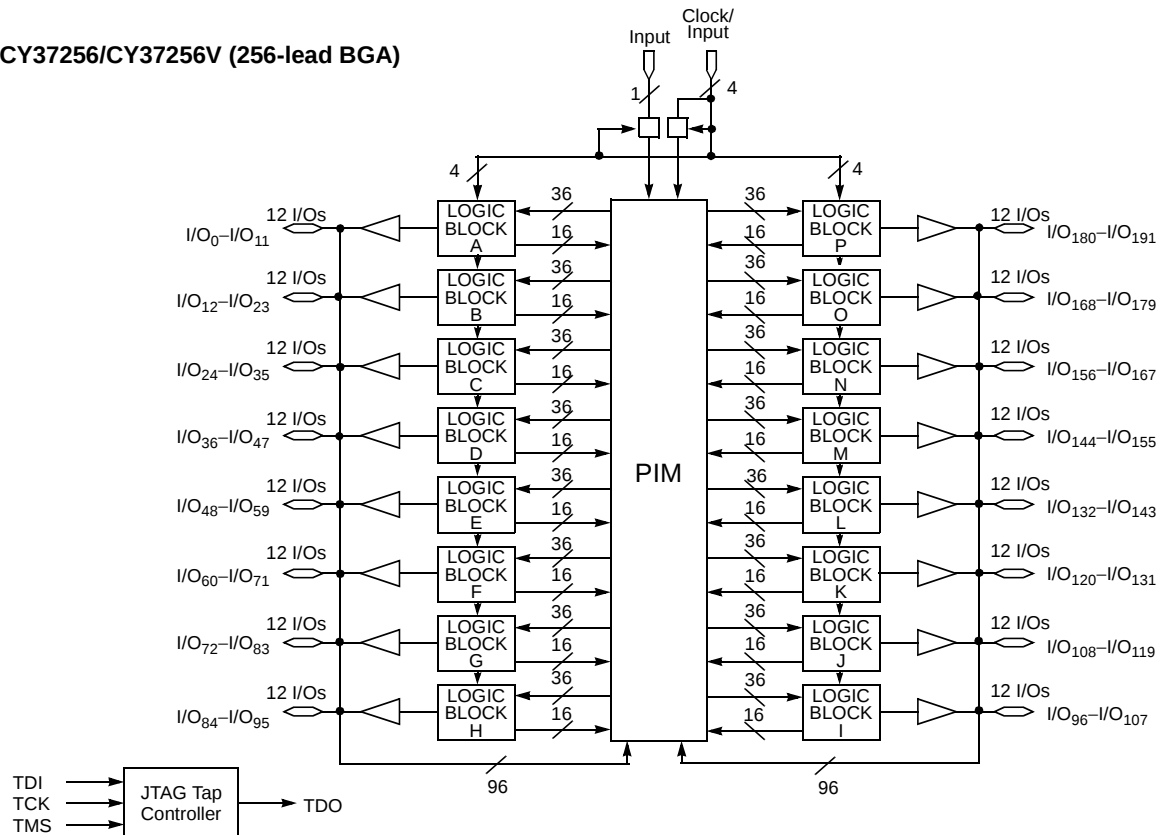


**CY37192/CY37192V (160-lead TQFP)**



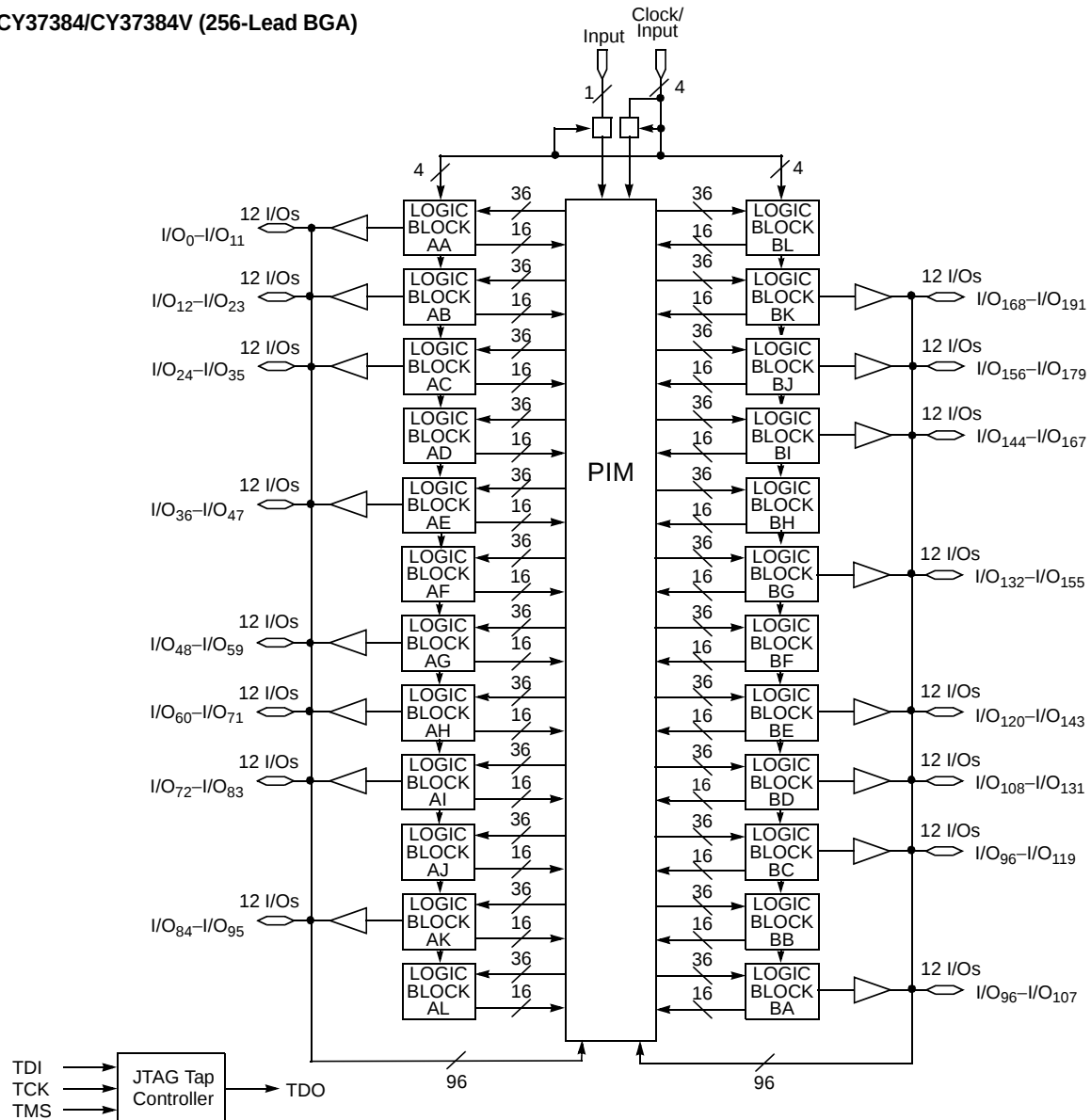
## Logic Block Diagrams (continued)

**CY37256/CY37256V (256-lead BGA)**



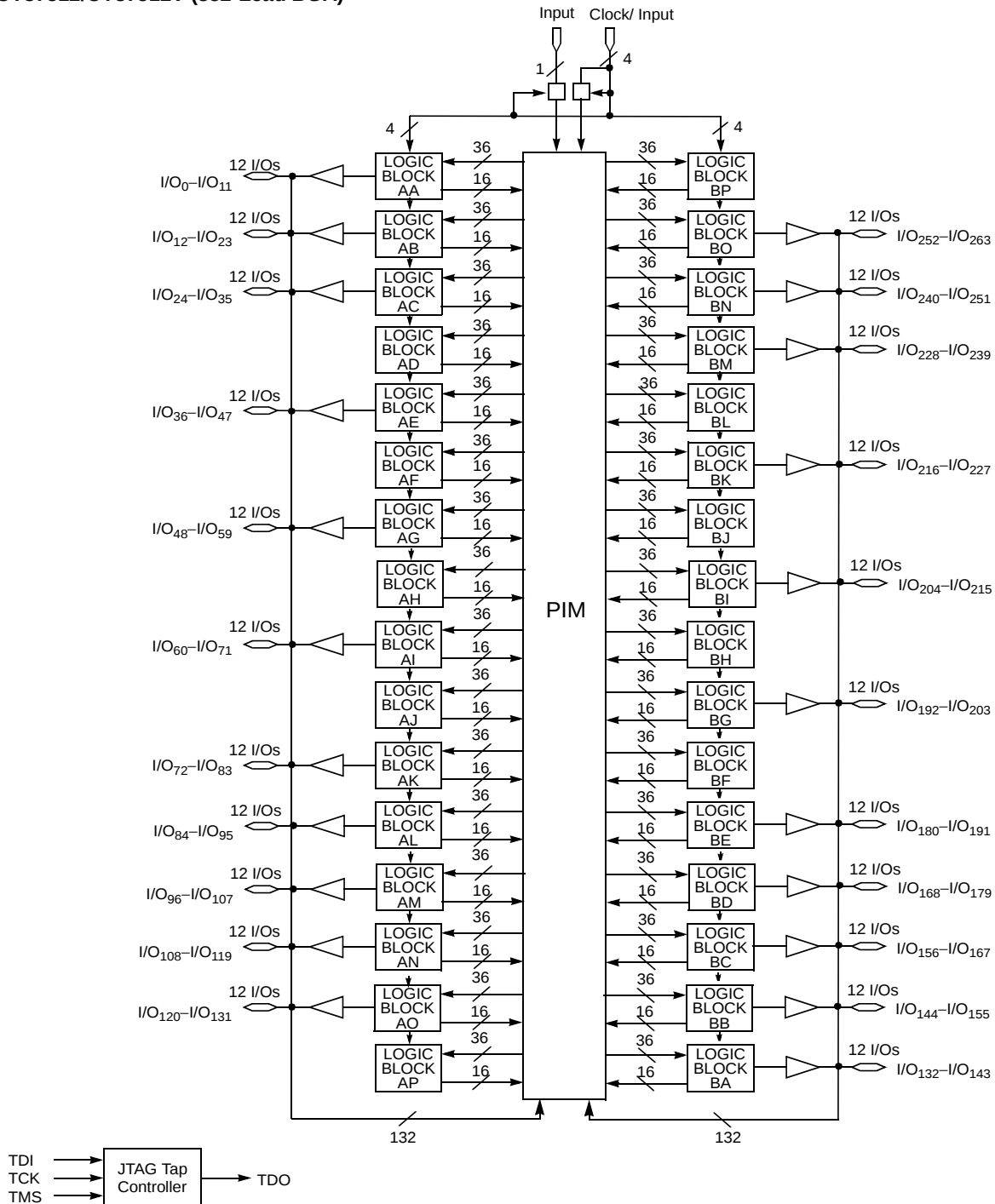
## Logic Block Diagrams (continued)

CY37384/CY37384V (256-Lead BGA)



## Logic Block Diagrams (continued)

CY37512/CY37512V (352-Lead BGA)





## 5.0V Device Characteristics

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High-Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -0.5V to +7.0V

DC Program Voltage ..... 4.5 to 5.5V

Current into Outputs ..... 16 mA

Static Discharge Voltage ..... > 2001V  
(per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

### Operating Range<sup>[2]</sup>

| Range                   | Ambient Temperature <sup>[2]</sup> | Junction Temperature | Output Condition | V <sub>CC</sub> | V <sub>CCO</sub> |
|-------------------------|------------------------------------|----------------------|------------------|-----------------|------------------|
| Commercial              | 0°C to +70°C                       | 0°C to +90°C         | 5V               | 5V ± 0.25V      | 5V ± 0.25V       |
|                         |                                    |                      | 3.3V             | 5V ± 0.25V      | 3.3V ± 0.3V      |
| Industrial              | -40°C to +85°C                     | -40°C to +105°C      | 5V               | 5V ± 0.5V       | 5V ± 0.5V        |
|                         |                                    |                      | 3.3V             | 5V ± 0.5V       | 3.3V ± 0.3V      |
| Military <sup>[3]</sup> | -55°C to +125°C                    | -55°C to +130°C      | 5V               | 5V ± 0.5V       | 5V ± 0.5V        |
|                         |                                    |                      | 3.3V             | 5V ± 0.5V       | 3.3V ± 0.3V      |

### 5.0V Device Electrical Characteristics Over the Operating Range

| Parameter         | Description                                             | Test Conditions                                                              | Min.                                                 | Typ. | Max.               | Unit |
|-------------------|---------------------------------------------------------|------------------------------------------------------------------------------|------------------------------------------------------|------|--------------------|------|
| V <sub>OH</sub>   | Output HIGH Voltage                                     | V <sub>CC</sub> = Min.                                                       | I <sub>OH</sub> = -3.2 mA (Com'I/Ind) <sup>[4]</sup> | 2.4  |                    | V    |
|                   |                                                         |                                                                              | I <sub>OH</sub> = -2.0 mA (Mil) <sup>[4]</sup>       | 2.4  |                    | V    |
| V <sub>OHZ</sub>  | Output HIGH Voltage with Output Disabled <sup>[5]</sup> | V <sub>CC</sub> = Max.                                                       | I <sub>OH</sub> = 0 μA (Com'I) <sup>[6]</sup>        |      | 4.2                | V    |
|                   |                                                         |                                                                              | I <sub>OH</sub> = 0 μA (Ind/Mil) <sup>[6]</sup>      |      | 4.5                | V    |
|                   |                                                         |                                                                              | I <sub>OH</sub> = -100 μA (Com'I) <sup>[6]</sup>     |      | 3.6                | V    |
|                   |                                                         |                                                                              | I <sub>OH</sub> = -150 μA (Ind/Mil) <sup>[6]</sup>   |      | 3.6                | V    |
| V <sub>OL</sub>   | Output LOW Voltage                                      | V <sub>CC</sub> = Min.                                                       | I <sub>OL</sub> = 16 mA (Com'I/Ind) <sup>[4]</sup>   |      | 0.5                | V    |
|                   |                                                         |                                                                              | I <sub>OL</sub> = 12 mA (Mil) <sup>[4]</sup>         |      | 0.5                | V    |
| V <sub>IH</sub>   | Input HIGH Voltage                                      | Guaranteed Input Logical HIGH Voltage for all Inputs <sup>[7]</sup>          | 2.0                                                  |      | V <sub>CCmax</sub> | V    |
| V <sub>IL</sub>   | Input LOW Voltage                                       | Guaranteed Input Logical LOW Voltage for all Inputs <sup>[7]</sup>           | -0.5                                                 |      | 0.8                | V    |
| I <sub>IX</sub>   | Input Load Current                                      | V <sub>I</sub> = GND OR V <sub>CC</sub> , Bus-Hold Disabled                  | -10                                                  |      | 10                 | μA   |
| I <sub>OZ</sub>   | Output Leakage Current                                  | V <sub>O</sub> = GND or V <sub>CC</sub> , Output Disabled, Bus-Hold Disabled | -50                                                  |      | 50                 | μA   |
| I <sub>OS</sub>   | Output Short Circuit Current <sup>[8, 5]</sup>          | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V                              | -30                                                  |      | -160               | mA   |
| I <sub>BHL</sub>  | Input Bus-Hold LOW Sustaining Current                   | V <sub>CC</sub> = Min., V <sub>IL</sub> = 0.8V                               | +75                                                  |      |                    | μA   |
| I <sub>BHH</sub>  | Input Bus-Hold HIGH Sustaining Current                  | V <sub>CC</sub> = Min., V <sub>IH</sub> = 2.0V                               | -75                                                  |      |                    | μA   |
| I <sub>BHLO</sub> | Input Bus-Hold LOW Overdrive Current                    | V <sub>CC</sub> = Max.                                                       |                                                      |      | +500               | μA   |
| I <sub>BHHO</sub> | Input Bus-Hold HIGH Overdrive Current                   | V <sub>CC</sub> = Max.                                                       |                                                      |      | -500               | μA   |

#### Notes:

- Normal Programming Conditions apply across Ambient Temperature Range for specified programming methods. For more information on programming the Ultra37000 Family devices, please refer to the Application Note titled "An Introduction to In System Reprogramming with the Ultra37000."
- T<sub>A</sub> is the "Instant On" case temperature.
- I<sub>OH</sub> = -2 mA, I<sub>OL</sub> = 2 mA for TDO.
- Tested initially and after any design or process changes that may affect these parameters.
- When the I/O is output disabled, the bus-hold circuit can weakly pull the I/O to above 3.6V if no leakage current is allowed. Note that all I/Os are output disabled during ISR programming. Refer to the application note "Understanding Bus-Hold" for additional information.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V<sub>OUT</sub> = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

## Inductance<sup>[5]</sup>

| Parameter | Description            | Test Conditions                       | 44-Lead TQFP | 44-Lead PLCC | 44-Lead CLCC | 84-Lead PLCC | 84-Lead CLCC | 100-Lead TQFP | 160-Lead TQFP | 208-Lead PQFP | Unit |
|-----------|------------------------|---------------------------------------|--------------|--------------|--------------|--------------|--------------|---------------|---------------|---------------|------|
| L         | Maximum Pin Inductance | $V_{IN} = 5.0V$ at $f = 1\text{ MHz}$ | 2            | 5            | 2            | 8            | 5            | 8             | 9             | 11            | nH   |

## Capacitance<sup>[5]</sup>

| Parameter | Description                       | Test Conditions                                             | Max. | Unit |
|-----------|-----------------------------------|-------------------------------------------------------------|------|------|
| $C_{I/O}$ | Input/Output Capacitance          | $V_{IN} = 5.0V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$ | 10   | pF   |
| $C_{CLK}$ | Clock Signal Capacitance          | $V_{IN} = 5.0V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$ | 12   | pF   |
| $C_{DP}$  | Dual Function Pins <sup>[9]</sup> | $V_{IN} = 5.0V$ at $f = 1\text{ MHz}$ at $T_A = 25^\circ C$ | 16   | pF   |

## Endurance Characteristics<sup>[5]</sup>

| Parameter | Description                  | Test Conditions                              | Min.  | Typ.   | Unit   |
|-----------|------------------------------|----------------------------------------------|-------|--------|--------|
| N         | Minimum Reprogramming Cycles | Normal Programming Conditions <sup>[2]</sup> | 1,000 | 10,000 | Cycles |

## 3.3V Device Characteristics

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....  $-65^\circ C$  to  $+150^\circ C$

Ambient Temperature with

Power Applied .....  $-55^\circ C$  to  $+125^\circ C$

Supply Voltage to Ground Potential .....  $-0.5V$  to  $+4.6V$

DC Voltage Applied to Outputs

in High-Z State .....  $-0.5V$  to  $+7.0V$

DC Input Voltage .....  $-0.5V$  to  $+7.0V$

DC Program Voltage .....  $3.0$  to  $3.6V$

Current into Outputs .....  $8\text{ mA}$

Static Discharge Voltage .....  $>2001V$   
(per MIL-STD-883, Method 3015)

Latch-up Current .....  $>200\text{ mA}$

## Operating Range<sup>[2]</sup>

| Range                   | Ambient Temperature <sup>[2]</sup> | Junction Temperature            | $V_{CC}$ <sup>[10]</sup> |
|-------------------------|------------------------------------|---------------------------------|--------------------------|
| Commercial              | $0^\circ C$ to $+70^\circ C$       | $0^\circ C$ to $+90^\circ C$    | $3.3V \pm 0.3V$          |
| Industrial              | $-40^\circ C$ to $+85^\circ C$     | $-40^\circ C$ to $+105^\circ C$ | $3.3V \pm 0.3V$          |
| Military <sup>[3]</sup> | $-55^\circ C$ to $+125^\circ C$    | $-55^\circ C$ to $+130^\circ C$ | $3.3V \pm 0.3V$          |

## 3.3V Device Electrical Characteristics Over the Operating Range

| Parameter | Description                                    | Test Conditions                                                                                        | Min.   | Max.   | Unit    |
|-----------|------------------------------------------------|--------------------------------------------------------------------------------------------------------|--------|--------|---------|
| $V_{OH}$  | Output HIGH Voltage                            | $V_{CC} = \text{Min.}$<br>$I_{OH} = -4\text{ mA (Com'l)}^{[4]}$<br>$I_{OH} = -3\text{ mA (Mil)}^{[4]}$ | 2.4    |        | V       |
| $V_{OL}$  | Output LOW Voltage                             | $V_{CC} = \text{Min.}$<br>$I_{OL} = 8\text{ mA (Com'l)}^{[4]}$<br>$I_{OL} = 6\text{ mA (Mil)}^{[4]}$   |        | 0.5    | V       |
| $V_{IH}$  | Input HIGH Voltage                             | Guaranteed Input Logical HIGH Voltage for all Inputs <sup>[7]</sup>                                    | 2.0    | 5.5    | V       |
| $V_{IL}$  | Input LOW Voltage                              | Guaranteed Input Logical LOW Voltage for all Inputs <sup>[7]</sup>                                     | $-0.5$ | 0.8    | V       |
| $I_{IX}$  | Input Load Current                             | $V_I = \text{GND OR } V_{CC}$ , Bus-Hold Disabled                                                      | $-10$  | 10     | $\mu A$ |
| $I_{OZ}$  | Output Leakage Current                         | $V_O = \text{GND or } V_{CC}$ , Output Disabled, Bus-Hold Disabled                                     | $-50$  | 50     | $\mu A$ |
| $I_{OS}$  | Output Short Circuit Current <sup>[8, 5]</sup> | $V_{CC} = \text{Max.}$ , $V_{OUT} = 0.5V$                                                              | $-30$  | $-160$ | mA      |
| $I_{BHL}$ | Input Bus-Hold LOW Sustaining Current          | $V_{CC} = \text{Min.}$ , $V_{IL} = 0.8V$                                                               | +75    |        | $\mu A$ |

### Notes:

9. Dual pins are I/O with JTAG pins.

10. For CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC; Operating Range:  $V_{CC}$  is  $3.3V \pm 0.16V$ .

## 3.3V Device Electrical Characteristics Over the Operating Range (continued)

| Parameter  | Description                            | Test Conditions                       | Min. | Max. | Unit    |
|------------|----------------------------------------|---------------------------------------|------|------|---------|
| $I_{BHH}$  | Input Bus-Hold HIGH Sustaining Current | $V_{CC} = \text{Min.}, V_{IH} = 2.0V$ | -75  |      | $\mu A$ |
| $I_{BHLO}$ | Input Bus-Hold LOW Overdrive Current   | $V_{CC} = \text{Max.}$                |      | +500 | $\mu A$ |
| $I_{BHHO}$ | Input Bus-Hold HIGH Overdrive Current  | $V_{CC} = \text{Max.}$                |      | -500 | $\mu A$ |

## Inductance<sup>[5]</sup>

| Parameter | Description            | Test Conditions                        | 44-Lead TQFP | 44-Lead PLCC | 44-Lead CLCC | 84-Lead PLCC | 84-Lead CLCC | 100-Lead TQFP | 160-Lead TQFP | 208-Lead PQFP | Unit |
|-----------|------------------------|----------------------------------------|--------------|--------------|--------------|--------------|--------------|---------------|---------------|---------------|------|
| L         | Maximum Pin Inductance | $V_{IN} = 3.3V$ at $f = 1 \text{ MHz}$ | 2            | 5            | 2            | 8            | 5            | 8             | 9             | 11            | nH   |

## Capacitance<sup>[5]</sup>

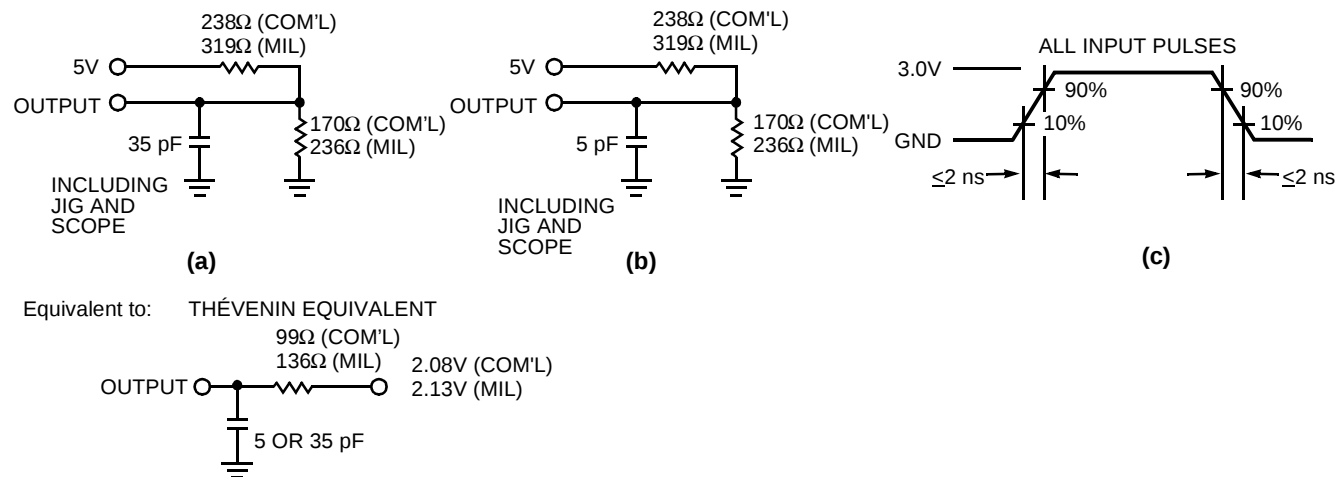
| Parameter | Description                         | Test Conditions                                              | Max. | Unit |
|-----------|-------------------------------------|--------------------------------------------------------------|------|------|
| $C_{I/O}$ | Input/Output Capacitance            | $V_{IN} = 3.3V$ at $f = 1 \text{ MHz}$ at $T_A = 25^\circ C$ | 8    | pF   |
| $C_{CLK}$ | Clock Signal Capacitance            | $V_{IN} = 3.3V$ at $f = 1 \text{ MHz}$ at $T_A = 25^\circ C$ | 12   | pF   |
| $C_{DP}$  | Dual Functional Pins <sup>[9]</sup> | $V_{IN} = 3.3V$ at $f = 1 \text{ MHz}$ at $T_A = 25^\circ C$ | 16   | pF   |

## Endurance Characteristics<sup>[5]</sup>

| Parameter | Description                  | Test Conditions                              | Min.  | Typ.   | Unit   |
|-----------|------------------------------|----------------------------------------------|-------|--------|--------|
| N         | Minimum Reprogramming Cycles | Normal Programming Conditions <sup>[2]</sup> | 1,000 | 10,000 | Cycles |

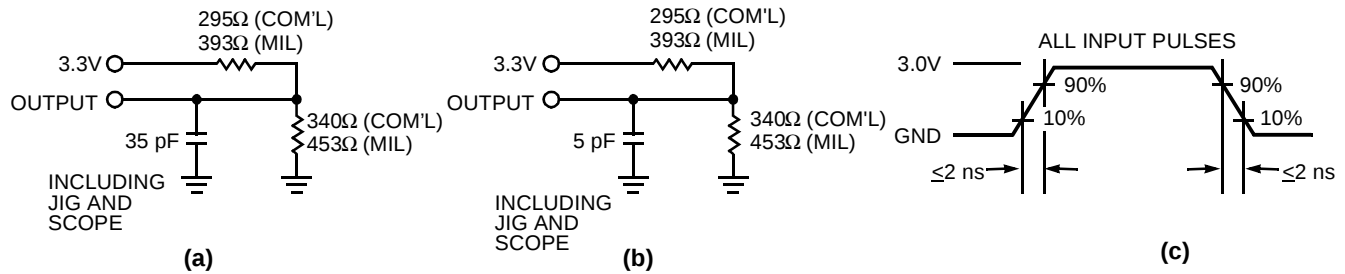
## AC Characteristics

### 5.0V AC Test Loads and Waveforms

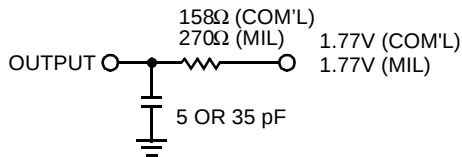


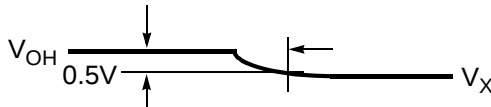
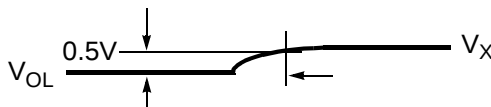
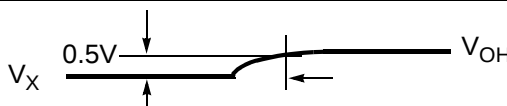
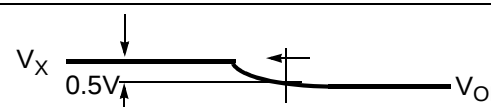
## AC Characteristics

### 3.3V AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



| Parameter <sup>[11]</sup> | V <sub>X</sub>   | Output Waveform—Measurement Level                                                    |
|---------------------------|------------------|--------------------------------------------------------------------------------------|
| t <sub>ER(-)</sub>        | 1.5V             |    |
| t <sub>ER(+)</sub>        | 2.6V             |   |
| t <sub>EA(+)</sub>        | 1.5V             |  |
| t <sub>EA(-)</sub>        | V <sub>the</sub> |  |

(d) Test Waveforms

### Switching Characteristics Over the Operating Range<sup>[12]</sup>

| Parameter                                 | Description                                                  | Unit |
|-------------------------------------------|--------------------------------------------------------------|------|
| <b>Combinatorial Mode Parameters</b>      |                                                              |      |
| t <sub>PD</sub> <sup>[13, 14, 15]</sup>   | Input to Combinatorial Output                                | ns   |
| t <sub>PDL</sub> <sup>[13, 14, 15]</sup>  | Input to Output Through Transparent Input or Output Latch    | ns   |
| t <sub>PDLL</sub> <sup>[13, 14, 15]</sup> | Input to Output Through Transparent Input and Output Latches | ns   |
| t <sub>EA</sub> <sup>[13, 14, 15]</sup>   | Input to Output Enable                                       | ns   |
| t <sub>ER</sub> <sup>[11, 13]</sup>       | Input to Output Disable                                      | ns   |
| <b>Input Register Parameters</b>          |                                                              |      |
| t <sub>WL</sub>                           | Clock or Latch Enable Input LOW Time <sup>[8]</sup>          | ns   |

#### Notes:

- t<sub>ER</sub> measured with 5-pF AC Test Load and t<sub>EA</sub> measured with 35-pF AC Test Load.
- All AC parameters are measured with two outputs switching and 35-pF AC Test Load.
- Logic Blocks operating in Low-Power Mode, add t<sub>LP</sub> to this spec.
- Outputs using Slow Output Slew Rate, add t<sub>SLEW</sub> to this spec.
- When V<sub>CCO</sub> = 3.3V, add t<sub>3,3IO</sub> to this spec.



## Switching Characteristics Over the Operating Range<sup>[12]</sup> (continued)

| Parameter                               | Description                                                                                                                                                                                                                                                                | Unit |
|-----------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| $t_{WH}$                                | Clock or Latch Enable Input HIGH Time <sup>[8]</sup>                                                                                                                                                                                                                       | ns   |
| $t_{IS}$                                | Input Register or Latch Set-up Time                                                                                                                                                                                                                                        | ns   |
| $t_{IH}$                                | Input Register or Latch Hold Time                                                                                                                                                                                                                                          | ns   |
| $t_{ICO}$ <sup>[13, 14, 15]</sup>       | Input Register Clock or Latch Enable to Combinatorial Output                                                                                                                                                                                                               | ns   |
| $t_{ICOL}$ <sup>[13, 14, 15]</sup>      | Input Register Clock or Latch Enable to Output Through Transparent Output Latch                                                                                                                                                                                            | ns   |
| <b>Synchronous Clocking Parameters</b>  |                                                                                                                                                                                                                                                                            |      |
| $t_{CO}$ <sup>[14, 15]</sup>            | Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable to Output                                                                                                                                                | ns   |
| $t_S$ <sup>[13]</sup>                   | Set-Up Time from Input to Sync. Clk (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable                                                                                                                                        | ns   |
| $t_H$                                   | Register or Latch Data Hold Time                                                                                                                                                                                                                                           | ns   |
| $t_{CO2}$ <sup>[13, 14, 15]</sup>       | Output Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable to Combinatorial Output Delay (Through Logic Array)                                                                                               | ns   |
| $t_{SCS}$ <sup>[13]</sup>               | Output Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable to Output Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable (Through Logic Array) | ns   |
| $t_{SL}$ <sup>[13]</sup>                | Set-Up Time from Input Through Transparent Latch to Output Register Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable                                                                                      | ns   |
| $t_{HL}$                                | Hold Time for Input Through Transparent Latch from Output Register Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) or Latch Enable                                                                                       | ns   |
| <b>Product Term Clocking Parameters</b> |                                                                                                                                                                                                                                                                            |      |
| $t_{COPT}$ <sup>[13, 14, 15]</sup>      | Product Term Clock or Latch Enable (PTCLK) to Output                                                                                                                                                                                                                       | ns   |
| $t_{SPT}$                               | Set-Up Time from Input to Product Term Clock or Latch Enable (PTCLK)                                                                                                                                                                                                       | ns   |
| $t_{HPT}$                               | Register or Latch Data Hold Time                                                                                                                                                                                                                                           | ns   |
| $t_{ISPT}$ <sup>[13]</sup>              | Set-Up Time for Buried Register used as an Input Register from Input to Product Term Clock or Latch Enable (PTCLK)                                                                                                                                                         | ns   |
| $t_{IHPT}$                              | Buried Register Used as an Input Register or Latch Data Hold Time                                                                                                                                                                                                          | ns   |
| $t_{CO2PT}$ <sup>[13, 14, 15]</sup>     | Product Term Clock or Latch Enable (PTCLK) to Output Delay (Through Logic Array)                                                                                                                                                                                           | ns   |
| <b>Pipelined Mode Parameters</b>        |                                                                                                                                                                                                                                                                            |      |
| $t_{ICS}$ <sup>[13]</sup>               | Input Register Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> ) to Output Register Synchronous Clock (CLK <sub>0</sub> , CLK <sub>1</sub> , CLK <sub>2</sub> , or CLK <sub>3</sub> )                                      | ns   |
| <b>Operating Frequency Parameters</b>   |                                                                                                                                                                                                                                                                            |      |
| $f_{MAX1}$                              | Maximum Frequency with Internal Feedback (Lesser of $1/t_{SCS}$ , $1/(t_S + t_H)$ , or $1/t_{CO}$ ) <sup>[5]</sup>                                                                                                                                                         | MHz  |
| $f_{MAX2}$                              | Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$ , $1/(t_S + t_H)$ , or $1/t_{CO}$ ) <sup>[5]</sup>                                                                                                                          | MHz  |
| $f_{MAX3}$                              | Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ or $1/(t_{WL} + t_{WH})$ ) <sup>[5]</sup>                                                                                                                                                           | MHz  |
| $f_{MAX4}$                              | Maximum Frequency in Pipelined Mode (Lesser of $1/(t_{CO} + t_{IS})$ , $1/t_{ICS}$ , $1/(t_{WL} + t_{WH})$ , $1/(t_{IS} + t_{IH})$ , or $1/t_{SCS}$ ) <sup>[5]</sup>                                                                                                       | MHz  |
| <b>Reset/Preset Parameters</b>          |                                                                                                                                                                                                                                                                            |      |
| $t_{RW}$                                | Asynchronous Reset Width <sup>[5]</sup>                                                                                                                                                                                                                                    | ns   |
| $t_{RR}$ <sup>[13]</sup>                | Asynchronous Reset Recovery Time <sup>[5]</sup>                                                                                                                                                                                                                            | ns   |
| $t_{RO}$ <sup>[13, 14, 15]</sup>        | Asynchronous Reset to Output                                                                                                                                                                                                                                               | ns   |
| $t_{PW}$                                | Asynchronous Preset Width <sup>[5]</sup>                                                                                                                                                                                                                                   | ns   |
| $t_{PR}$ <sup>[13]</sup>                | Asynchronous Preset Recovery Time <sup>[5]</sup>                                                                                                                                                                                                                           | ns   |
| $t_{PO}$ <sup>[13, 14, 15]</sup>        | Asynchronous Preset to Output                                                                                                                                                                                                                                              | ns   |
| <b>User Option Parameters</b>           |                                                                                                                                                                                                                                                                            |      |
| $t_{LP}$                                | Low Power Adder                                                                                                                                                                                                                                                            | ns   |
| $t_{SLEW}$                              | Slow Output Slew Rate Adder                                                                                                                                                                                                                                                | ns   |
| $t_{3.3IO}$                             | 3.3V I/O Mode Timing Adder <sup>[5]</sup>                                                                                                                                                                                                                                  | ns   |



## Switching Characteristics Over the Operating Range<sup>[12]</sup> (continued)

| Parameter                     | Description                                          | Unit |
|-------------------------------|------------------------------------------------------|------|
| <b>JTAG Timing Parameters</b> |                                                      |      |
| $t_{S\ JTAG}$                 | Set-up Time from TDI and TMS to TCK <sup>[5]</sup>   | ns   |
| $t_{H\ JTAG}$                 | Hold Time on TDI and TMS <sup>[5]</sup>              | ns   |
| $t_{CO\ JTAG}$                | Falling Edge of TCK to TDO <sup>[5]</sup>            | ns   |
| $f_{JTAG}$                    | Maximum JTAG Tap Controller Frequency <sup>[5]</sup> | ns   |

## Switching Characteristics Over the Operating Range<sup>[12]</sup>

| Parameter                                  | 200 MHz |      | 167 MHz |      | 154 MHz |      | 143 MHz |      | 125 MHz             |                     | 100 MHz           |                     | 83 MHz            |                   | 66 MHz |      | Unit |
|--------------------------------------------|---------|------|---------|------|---------|------|---------|------|---------------------|---------------------|-------------------|---------------------|-------------------|-------------------|--------|------|------|
|                                            | Min.    | Max. | Min.    | Max. | Min.    | Max. | Min.    | Max. | Min.                | Max.                | Min.              | Max.                | Min.              | Max.              | Min.   | Max. |      |
| Combinatorial Mode Parameters              |         |      |         |      |         |      |         |      |                     |                     |                   |                     |                   |                   |        |      |      |
| t <sub>PD</sub> <sup>[13, 14, 15]</sup>    |         | 6    |         | 6.5  |         | 7.5  |         | 8.5  |                     | 10                  |                   | 12                  |                   | 15                |        | 20   | ns   |
| t <sub>PDL</sub> <sup>[13, 14, 15]</sup>   |         | 11   |         | 12.5 |         | 14.5 |         | 16   |                     | 16.5                |                   | 17                  |                   | 19                |        | 22   | ns   |
| t <sub>PDLL</sub> <sup>[13, 14, 15]</sup>  |         | 12   |         | 13.5 |         | 15.5 |         | 17   |                     | 17.5                |                   | 18                  |                   | 20                |        | 24   | ns   |
| t <sub>EA</sub> <sup>[13, 14, 15]</sup>    |         | 8    |         | 8.5  |         | 11   |         | 13   |                     | 14                  |                   | 16                  |                   | 19                |        | 24   | ns   |
| t <sub>ER</sub> <sup>[11, 13]</sup>        |         | 8    |         | 8.5  |         | 11   |         | 13   |                     | 14                  |                   | 16                  |                   | 19                |        | 24   | ns   |
| Input Register Parameters                  |         |      |         |      |         |      |         |      |                     |                     |                   |                     |                   |                   |        |      |      |
| t <sub>WL</sub>                            | 2.5     |      | 2.5     |      | 2.5     |      | 2.5     |      | 3                   |                     | 3                 |                     | 4                 |                   | 5      |      | ns   |
| t <sub>WH</sub>                            | 2.5     |      | 2.5     |      | 2.5     |      | 2.5     |      | 3                   |                     | 3                 |                     | 4                 |                   | 5      |      | ns   |
| t <sub>IS</sub>                            | 2       |      | 2       |      | 2       |      | 2       |      | 2                   |                     | 2.5               |                     | 3                 |                   | 4      |      | ns   |
| t <sub>IH</sub>                            | 2       |      | 2       |      | 2       |      | 2       |      | 2                   |                     | 2.5               |                     | 3                 |                   | 4      |      | ns   |
| t <sub>ICO</sub> <sup>[13, 14, 15]</sup>   |         | 11   |         | 11   |         | 11   |         | 12.5 |                     | 12.5                |                   | 16                  |                   | 19                |        | 24   | ns   |
| t <sub>ICOL</sub> <sup>[13, 14, 15]</sup>  |         | 12   |         | 12   |         | 12   |         | 14   |                     | 16                  |                   | 18                  |                   | 21                |        | 26   | ns   |
| Synchronous Clocking Parameters            |         |      |         |      |         |      |         |      |                     |                     |                   |                     |                   |                   |        |      |      |
| t <sub>CO</sub> <sup>[14, 15]</sup>        |         | 4    |         | 4    |         | 4.5  |         | 6    |                     | 6.5 <sup>[16]</sup> |                   | 6.5 <sup>[17]</sup> |                   | 8 <sup>[18]</sup> |        | 10   | ns   |
| t <sub>S</sub> <sup>[13]</sup>             | 4       |      | 4       |      | 5       |      | 5       |      | 5.5 <sup>[16]</sup> |                     | 6 <sup>[17]</sup> |                     | 8 <sup>[18]</sup> |                   | 10     |      | ns   |
| t <sub>H</sub>                             | 0       |      | 0       |      | 0       |      | 0       |      | 0                   |                     | 0                 |                     | 0                 |                   | 0      |      | ns   |
| t <sub>CO2</sub> <sup>[13, 14, 15]</sup>   |         | 9.5  |         | 10   |         | 11   |         | 12   |                     | 14                  |                   | 16                  |                   | 19                |        | 24   | ns   |
| t <sub>SCS</sub> <sup>[13]</sup>           | 5       |      | 6       |      | 6.5     |      | 7       |      | 8 <sup>[16]</sup>   |                     | 10                |                     | 12                |                   | 15     |      | ns   |
| t <sub>SL</sub> <sup>[13]</sup>            | 7.5     |      | 7.5     |      | 8.5     |      | 9       |      | 10                  |                     | 12                |                     | 15                |                   | 15     |      | ns   |
| t <sub>HL</sub>                            | 0       |      | 0       |      | 0       |      | 0       |      | 0                   |                     | 0                 |                     | 0                 |                   | 0      |      | ns   |
| Product Term Clocking Parameters           |         |      |         |      |         |      |         |      |                     |                     |                   |                     |                   |                   |        |      |      |
| t <sub>COPT</sub> <sup>[13, 14, 15]</sup>  |         | 7    |         | 10   |         | 10   |         | 13   |                     | 13                  |                   | 13                  |                   | 15                |        | 20   | ns   |
| t <sub>SPT</sub>                           | 2.5     |      | 2.5     |      | 2.5     |      | 3       |      | 5                   |                     | 5.5               |                     | 6                 |                   | 7      |      | ns   |
| t <sub>HPT</sub>                           | 2.5     |      | 2.5     |      | 2.5     |      | 3       |      | 5                   |                     | 5.5               |                     | 6                 |                   | 7      |      | ns   |
| t <sub>ISPT</sub> <sup>[13]</sup>          | 0       |      | 0       |      | 0       |      | 0       |      | 0                   |                     | 0                 |                     | 0                 |                   | 0      |      | ns   |
| t <sub>IHPT</sub>                          | 6       |      | 6.5     |      | 6.5     |      | 7.5     |      | 9                   |                     | 11                |                     | 14                |                   | 19     |      | ns   |
| t <sub>CO2PT</sub> <sup>[13, 14, 15]</sup> |         | 12   |         | 14   |         | 15   |         | 19   |                     | 19                  |                   | 21                  |                   | 24                |        | 30   | ns   |
| Pipelined Mode Parameters                  |         |      |         |      |         |      |         |      |                     |                     |                   |                     |                   |                   |        |      |      |
| t <sub>ICS</sub> <sup>[13]</sup>           | 5       |      | 6       |      | 6       |      | 7       |      | 8 <sup>[16]</sup>   |                     | 10                |                     | 12                |                   | 15     |      | ns   |

### Notes:

- The following values correspond to the CY37512 and CY37384 devices:  $t_{CO} = 5$  ns,  $t_S = 6.5$  ns,  $t_{SCS} = 8.5$  ns,  $t_{ICS} = 8.5$  ns,  $f_{MAX1} = 118$  MHz.
- The following values correspond to the CY37192V and CY37256V devices:  $t_{CO} = 6$  ns,  $t_S = 7$  ns,  $f_{MAX2} = 143$  MHz,  $f_{MAX3} = 77$  MHz, and  $f_{MAX4} = 100$  MHz; and for the CY37512 devices:  $t_S = 7$  ns.
- The following values correspond to the CY37512V and CY37384V devices:  $t_{CO} = 6.5$  ns,  $t_S = 9.5$  ns, and  $f_{MAX2} = 105$  MHz.

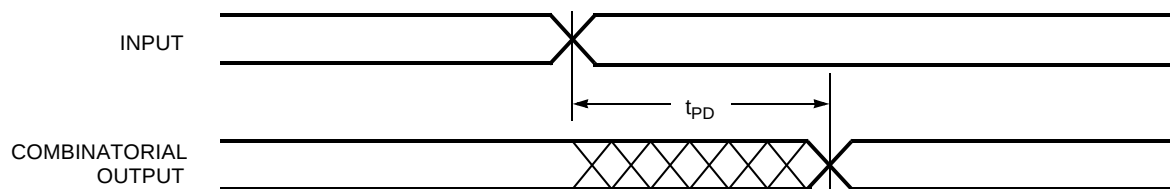


## Switching Characteristics Over the Operating Range<sup>[12]</sup> (continued)

| Parameter                               | 200 MHz |      | 167 MHz |      | 154 MHz |      | 143 MHz |      | 125 MHz             |      | 100 MHz             |      | 83 MHz              |      | 66 MHz |      | Unit |
|-----------------------------------------|---------|------|---------|------|---------|------|---------|------|---------------------|------|---------------------|------|---------------------|------|--------|------|------|
|                                         | Min.    | Max. | Min.    | Max. | Min.    | Max. | Min.    | Max. | Min.                | Max. | Min.                | Max. | Min.                | Max. | Min.   | Max. |      |
| Operating Frequency Parameters          |         |      |         |      |         |      |         |      |                     |      |                     |      |                     |      |        |      |      |
| f <sub>MAX1</sub>                       | 200     |      | 167     |      | 154     |      | 143     |      | 125 <sup>[16]</sup> |      | 100                 |      | 83                  |      | 66     |      | MHz  |
| f <sub>MAX2</sub>                       | 200     |      | 200     |      | 200     |      | 167     |      | 154                 |      | 153 <sup>[17]</sup> |      | 125 <sup>[18]</sup> |      | 100    |      | MHz  |
| f <sub>MAX3</sub>                       | 125     |      | 125     |      | 105     |      | 91      |      | 83                  |      | 80 <sup>[17]</sup>  |      | 62.5                |      | 50     |      | MHz  |
| f <sub>MAX4</sub>                       | 167     |      | 167     |      | 154     |      | 125     |      | 118                 |      | 100                 |      | 83                  |      | 66     |      | MHz  |
| Reset/Preset Parameters                 |         |      |         |      |         |      |         |      |                     |      |                     |      |                     |      |        |      |      |
| t <sub>RW</sub>                         | 8       |      | 8       |      | 8       |      | 8       |      | 10                  |      | 12                  |      | 15                  |      | 20     |      | ns   |
| t <sub>RR</sub> <sup>[13]</sup>         | 10      |      | 10      |      | 10      |      | 10      |      | 12                  |      | 14                  |      | 17                  |      | 22     |      | ns   |
| t <sub>RO</sub> <sup>[13, 14, 15]</sup> |         | 12   |         | 13   |         | 13   |         | 14   |                     | 15   |                     | 18   |                     | 21   |        | 26   | ns   |
| t <sub>PW</sub>                         | 8       |      | 8       |      | 8       |      | 8       |      | 10                  |      | 12                  |      | 15                  |      | 20     |      | ns   |
| t <sub>PR</sub> <sup>[13]</sup>         | 10      |      | 10      |      | 10      |      | 10      |      | 12                  |      | 14                  |      | 17                  |      | 22     |      | ns   |
| t <sub>PO</sub> <sup>[13, 14, 15]</sup> |         | 12   |         | 13   |         | 13   |         | 14   |                     | 15   |                     | 18   |                     | 21   |        | 26   | ns   |
| User Option Parameters                  |         |      |         |      |         |      |         |      |                     |      |                     |      |                     |      |        |      |      |
| t <sub>LP</sub>                         |         | 2.5  |         | 2.5  |         | 2.5  |         | 2.5  |                     | 2.5  |                     | 2.5  |                     | 2.5  |        | 2.5  | ns   |
| t <sub>SLEW</sub>                       |         | 3    |         | 3    |         | 3    |         | 3    |                     | 3    |                     | 3    |                     | 3    |        | 3    | ns   |
| t <sub>3.3IO</sub> <sup>[19]</sup>      |         | 0.3  |         | 0.3  |         | 0.3  |         | 0.3  |                     | 0.3  |                     | 0.3  |                     | 0.3  |        | 0.3  | ns   |
| JTAG Timing Parameters                  |         |      |         |      |         |      |         |      |                     |      |                     |      |                     |      |        |      |      |
| t <sub>S JTAG</sub>                     | 0       |      | 0       |      | 0       |      | 0       |      | 0                   |      | 0                   |      | 0                   |      | 0      |      | ns   |
| t <sub>H JTAG</sub>                     | 20      |      | 20      |      | 20      |      | 20      |      | 20                  |      | 20                  |      | 20                  |      | 20     |      | ns   |
| t <sub>CO JTAG</sub>                    |         | 20   |         | 20   |         | 20   |         | 20   |                     | 20   |                     | 20   |                     | 20   |        | 20   | ns   |
| f <sub>JTAG</sub>                       |         | 20   |         | 20   |         | 20   |         | 20   |                     | 20   |                     | 20   |                     | 20   |        | 20   | MHz  |

## Switching Waveforms

### Combinatorial Output

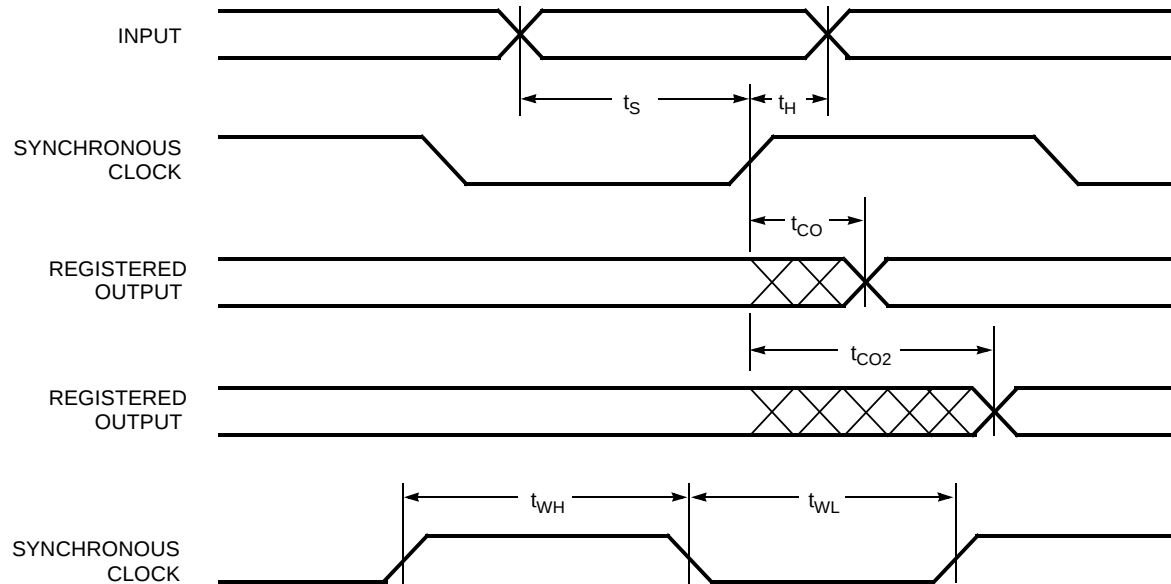


#### Note:

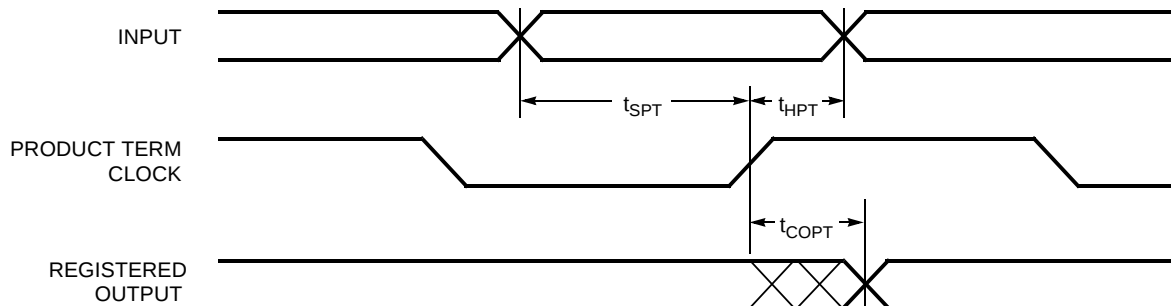
19. Only applicable to the 5V devices.

## Switching Waveforms (continued)

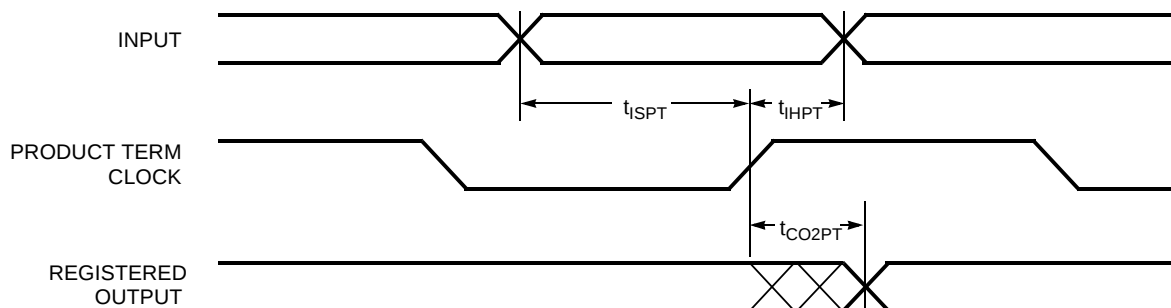
### Registered Output with Synchronous Clocking

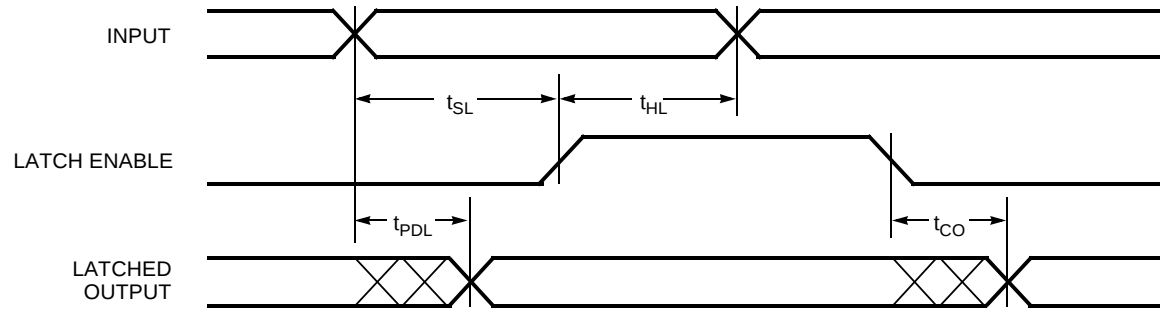
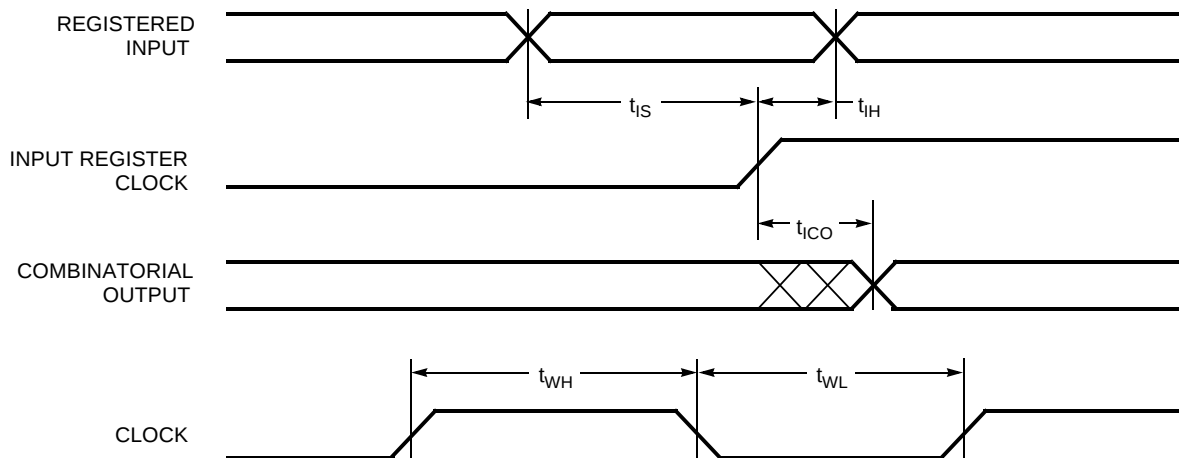
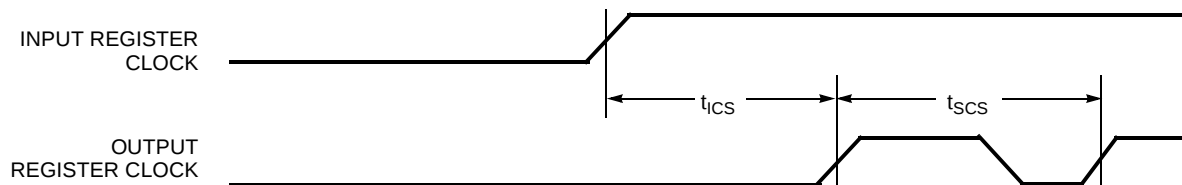


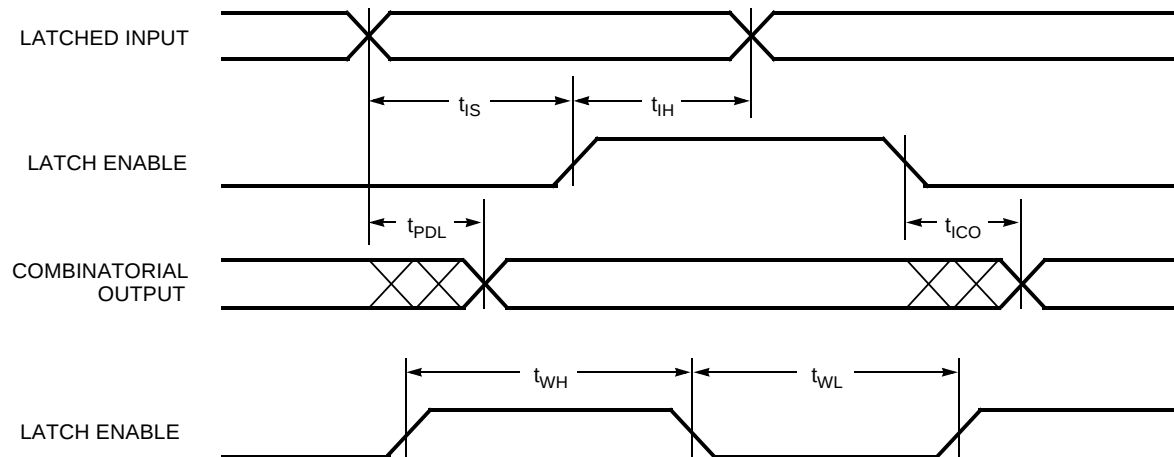
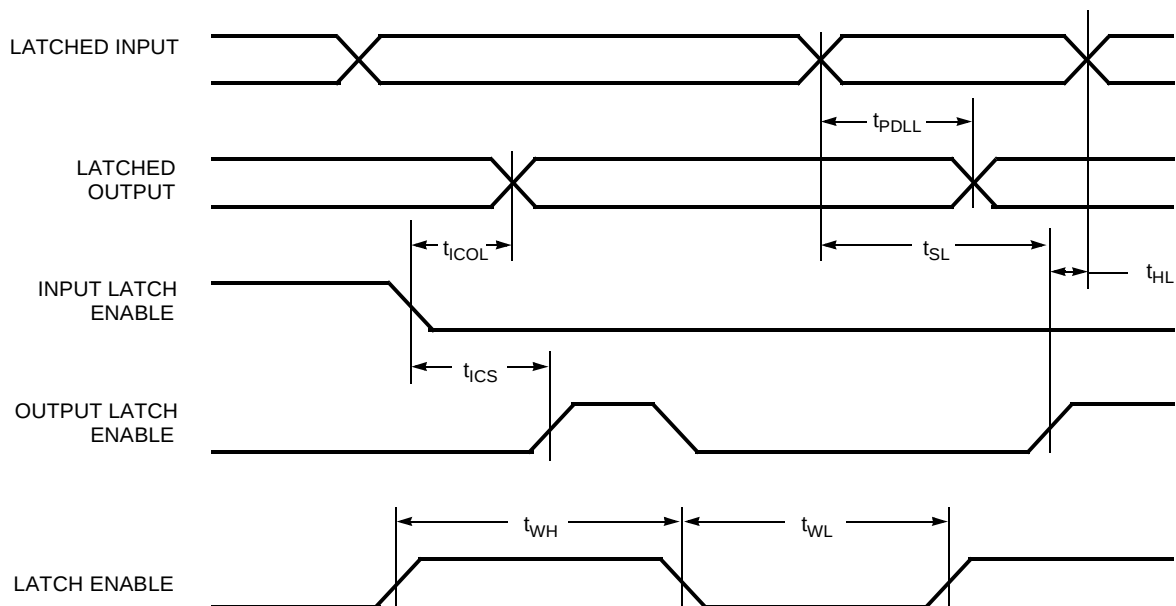
### Registered Output with Product Term Clocking Input Going Through the Array

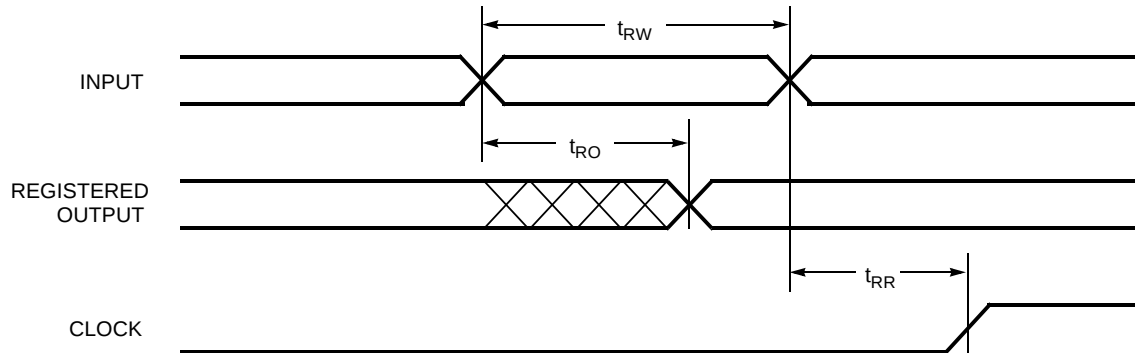
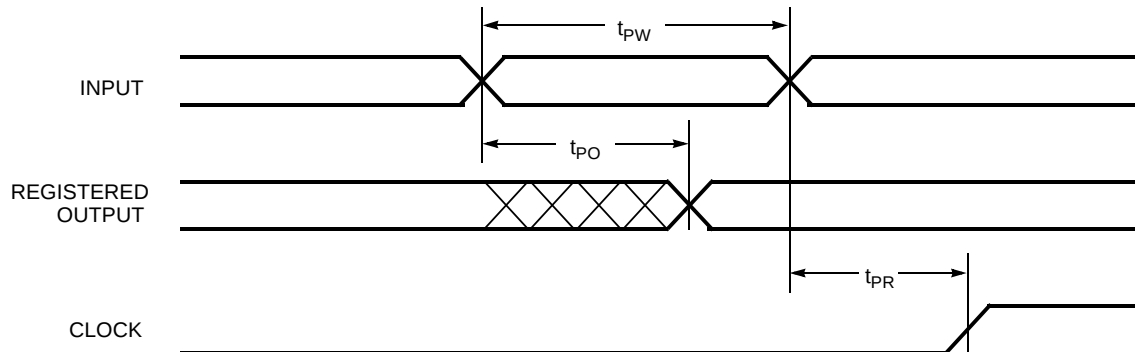
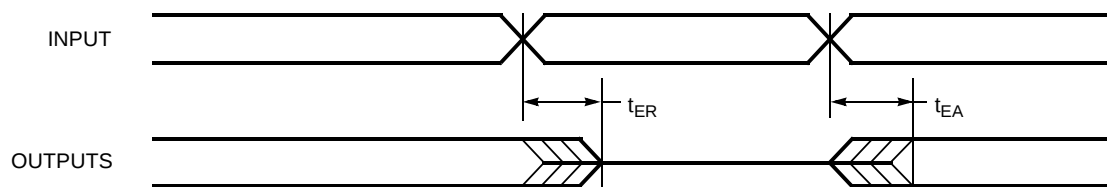


### Registered Output with Product Term Clocking Input Coming From Adjacent Buried Register



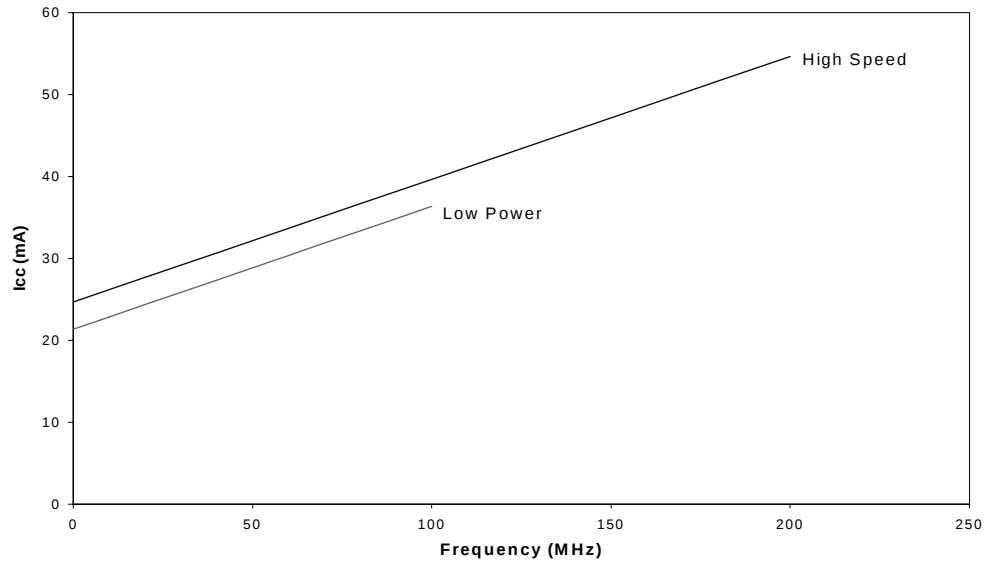
**Switching Waveforms (continued)**
**Latched Output**

**Registered Input**

**Clock to Clock**


**Switching Waveforms (continued)**
**Latched Input**

**Latched Input and Output**


**Switching Waveforms (continued)**
**Asynchronous Reset**

**Asynchronous Preset**

**Output Enable/Disable**


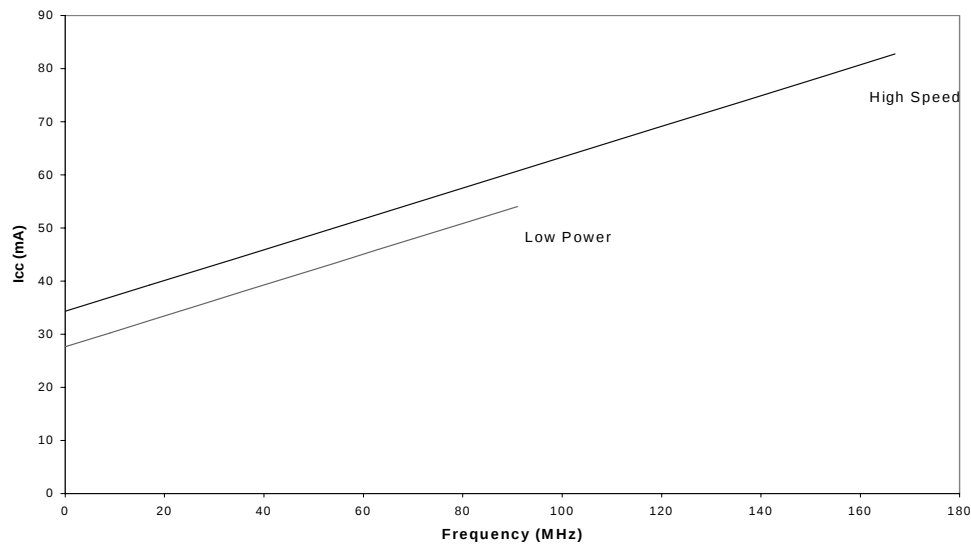
## Power Consumption

### Typical 5.0V Power Consumption CY37032



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
V<sub>CC</sub> = 5.0V, T<sub>A</sub> = Room Temperature

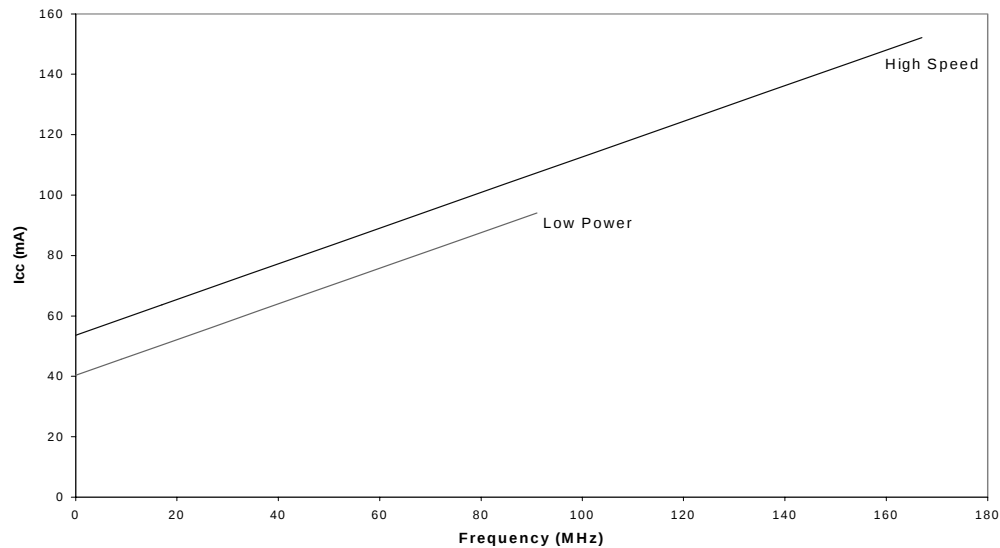
### CY37064



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
V<sub>CC</sub> = 5.0V, T<sub>A</sub> = Room Temperature

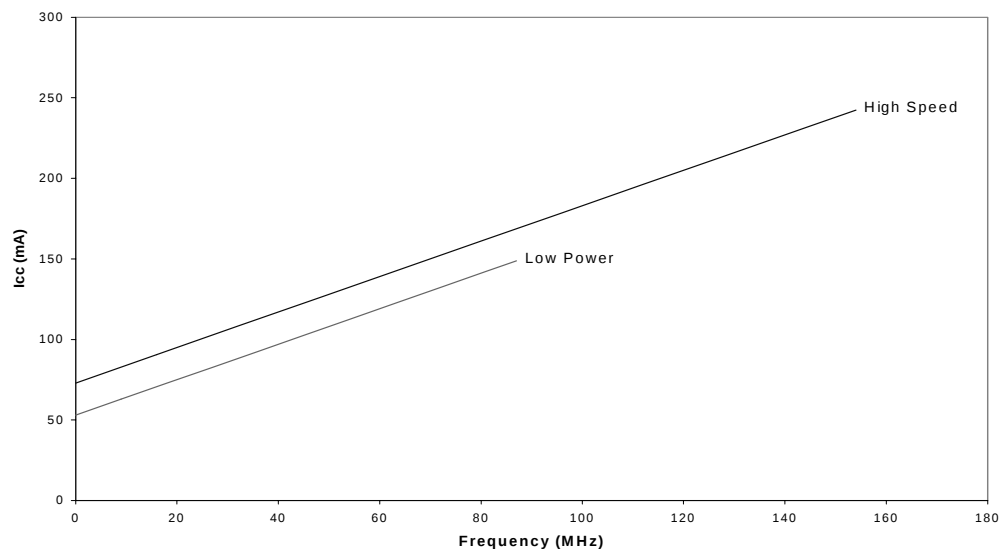
## Typical 5.0V Power Consumption (continued)

### CY37128



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
 $V_{CC} = 5.0V$ ,  $T_A = \text{Room Temperature}$

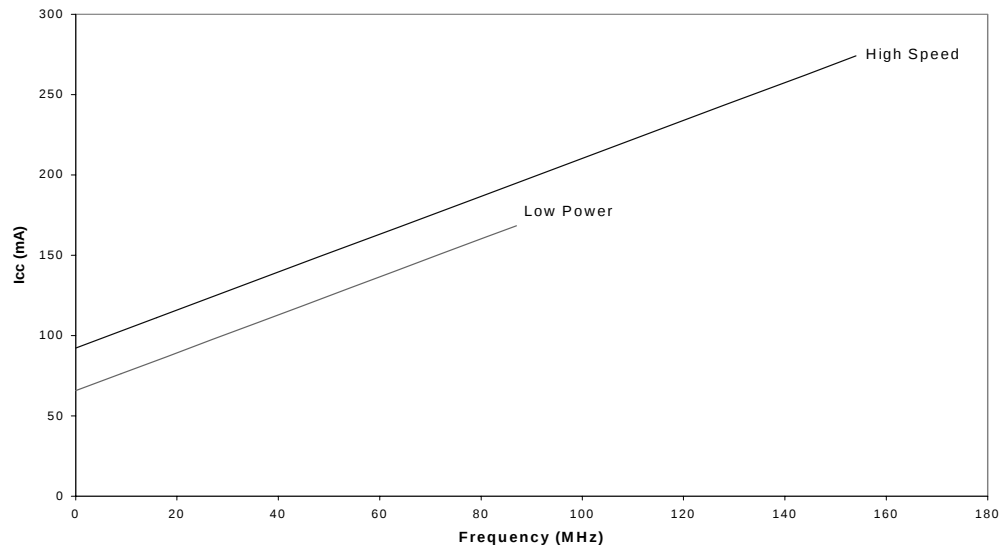
### CY37192



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
 $V_{CC} = 5.0V$ ,  $T_A = \text{Room Temperature}$

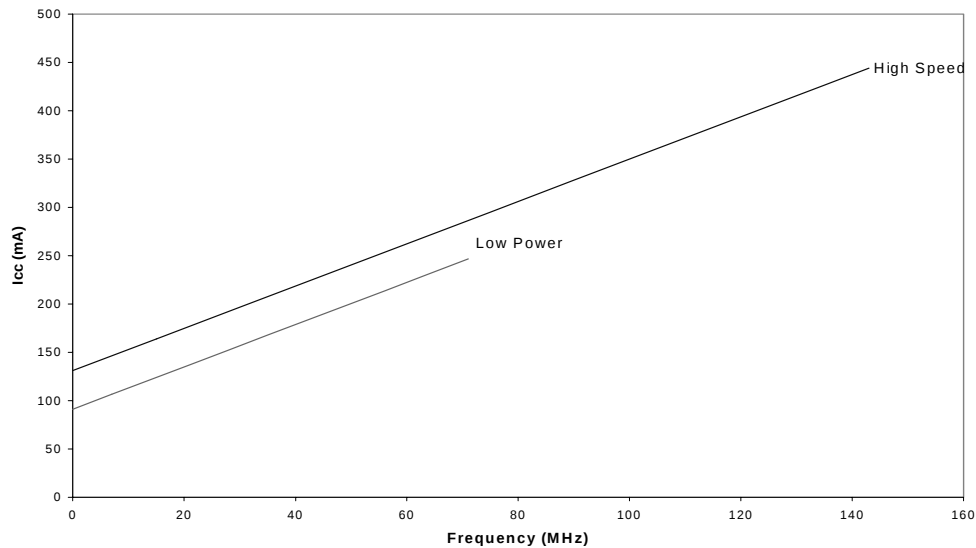
## Typical 5.0V Power Consumption (continued)

### CY37256



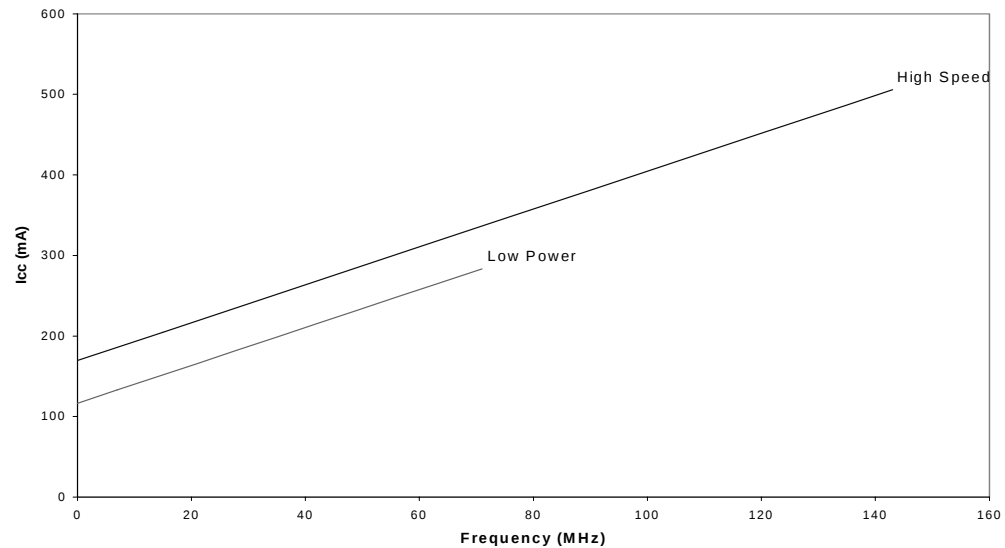
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
 $V_{CC} = 5.0V$ ,  $T_A = \text{Room Temperature}$

### CY37384



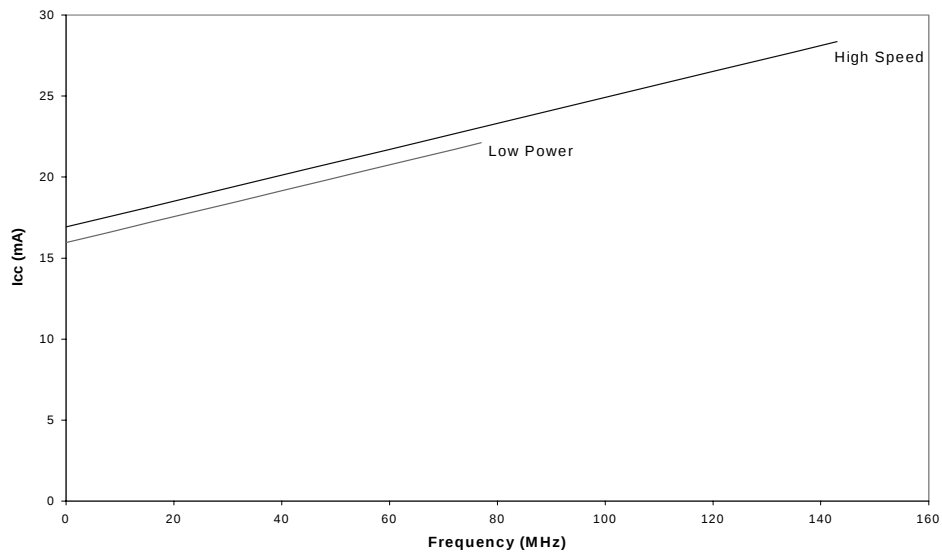
The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
 $V_{CC} = 5.0V$ ,  $T_A = \text{Room Temperature}$

## Typical 5.0V Power Consumption (continued) CY37512



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
V<sub>CC</sub> = 5.0V, T<sub>A</sub> = Room Temperature

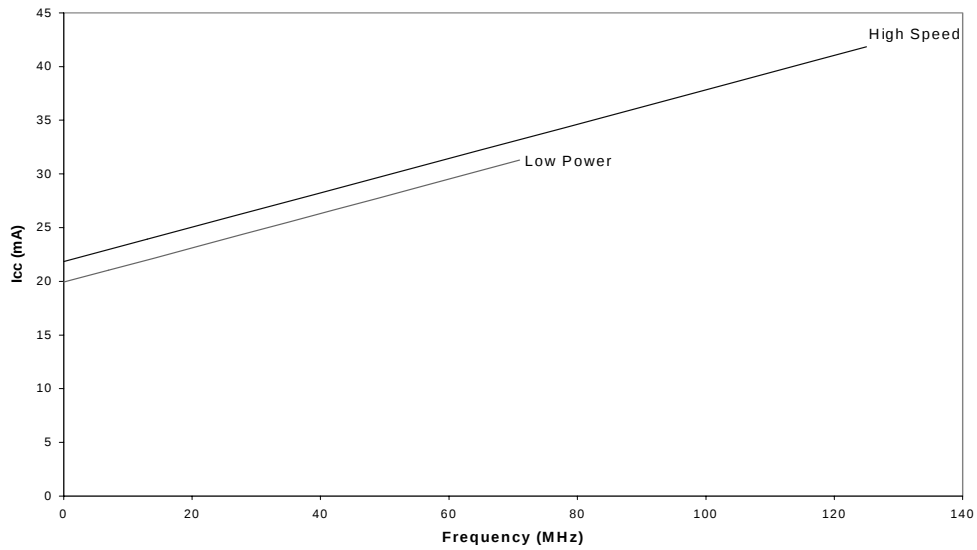
## Typical 3.3V Power Consumption CY37032V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
V<sub>CC</sub> = 3.3V, T<sub>A</sub> = Room Temperature

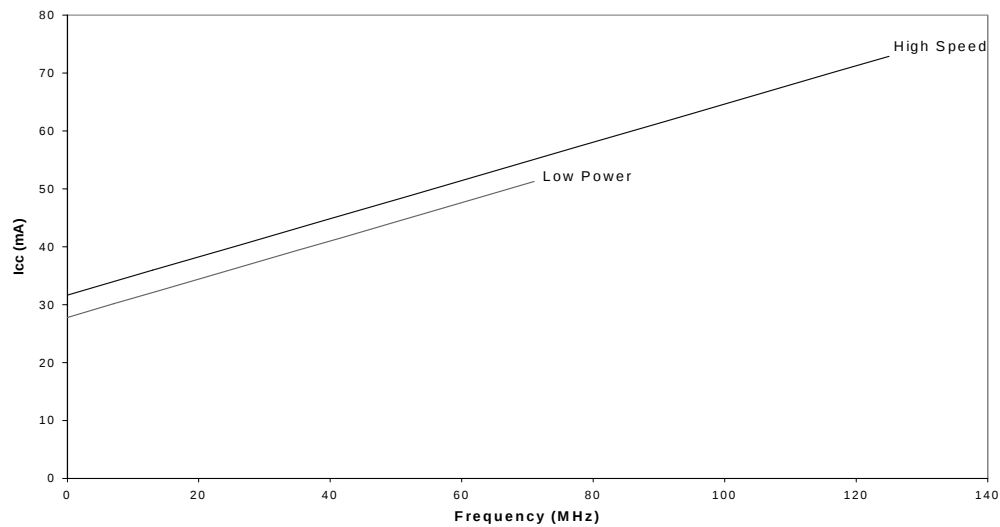
## Typical 3.3V Power Consumption (continued)

### CY37064V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
 $V_{CC} = 3.3V$ ,  $T_A = \text{Room Temperature}$

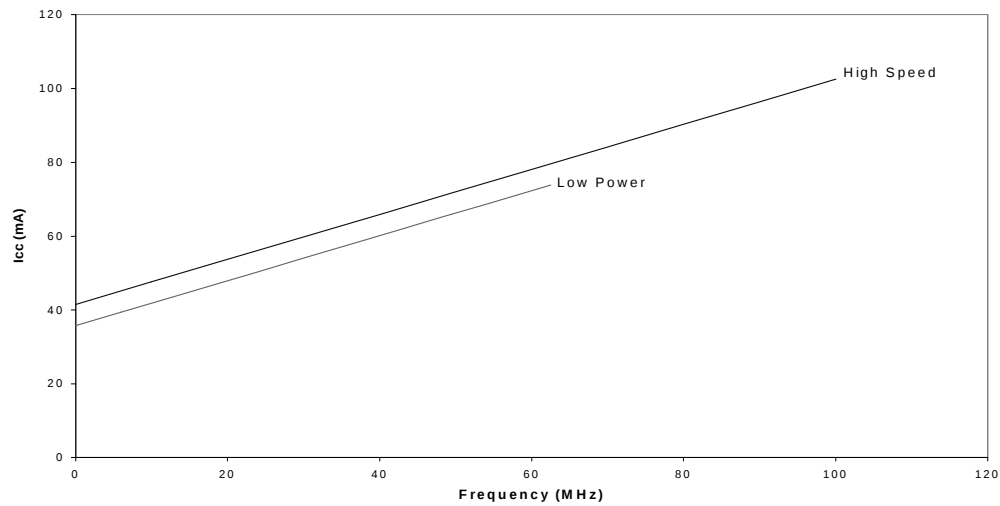
### CY37128V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
 $V_{CC} = 3.3V$ ,  $T_A = \text{Room Temperature}$

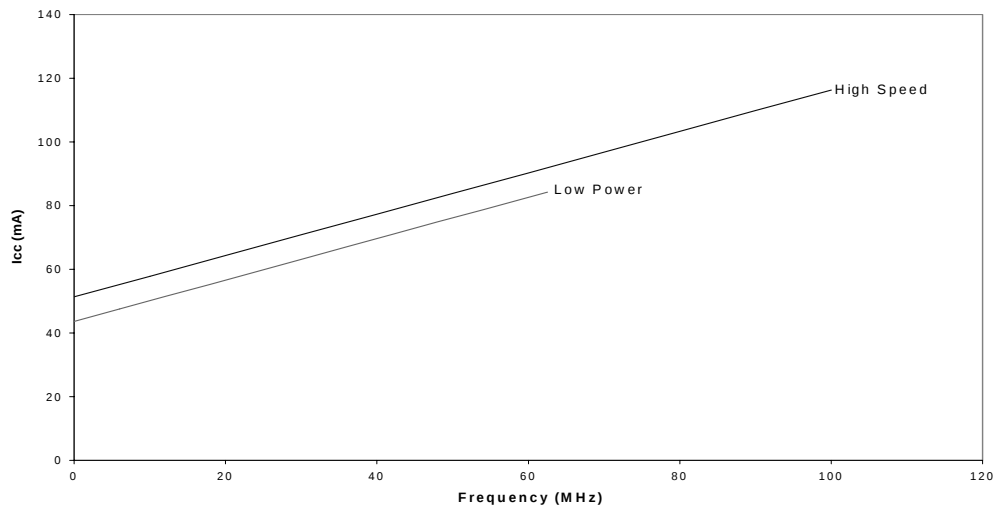
## Typical 3.3V Power Consumption (continued)

### CY37192V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
 $V_{CC} = 3.3V$ ,  $T_A = \text{Room Temperature}$

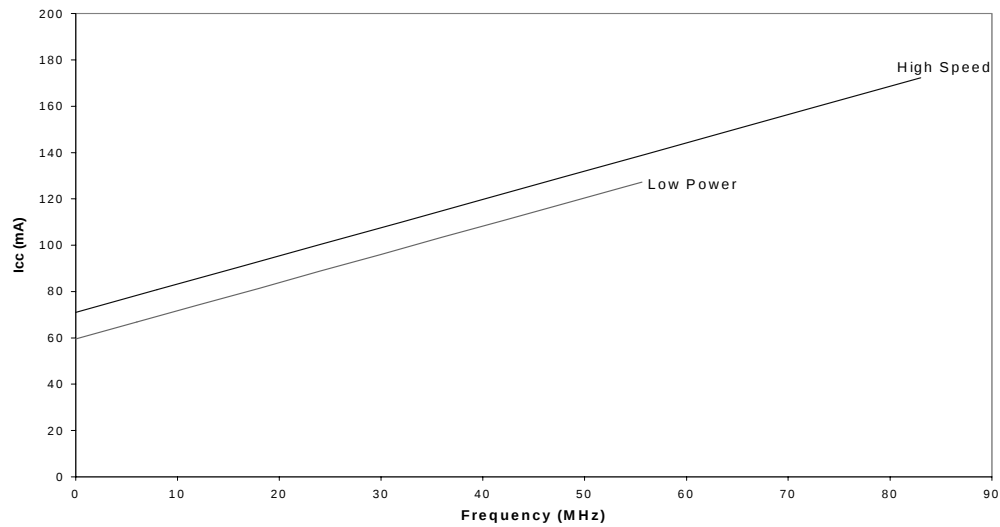
### CY37256V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
 $V_{CC} = 3.3V$ ,  $T_A = \text{Room Temperature}$

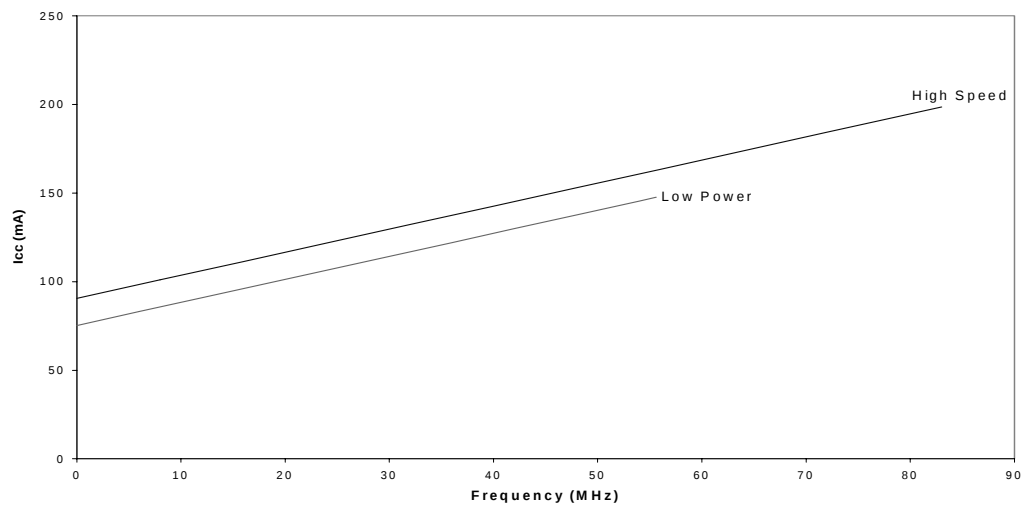
## Typical 3.3V Power Consumption (continued)

### CY37384V



The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
 $V_{CC} = 3.3V$ ,  $T_A = \text{Room Temperature}$

### CY37512V

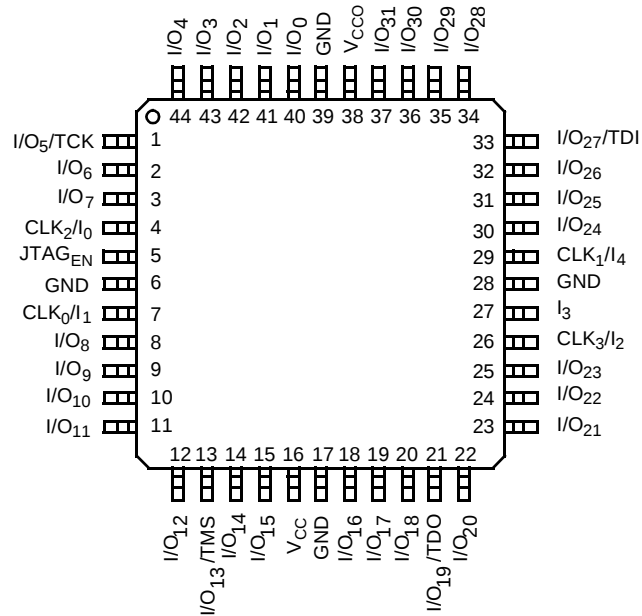


The typical pattern is a 16-bit up counter, per logic block, with outputs disabled.  
 $V_{CC} = 3.3V$ ,  $T_A = \text{Room Temperature}$

## Pin Configurations<sup>[20]</sup>

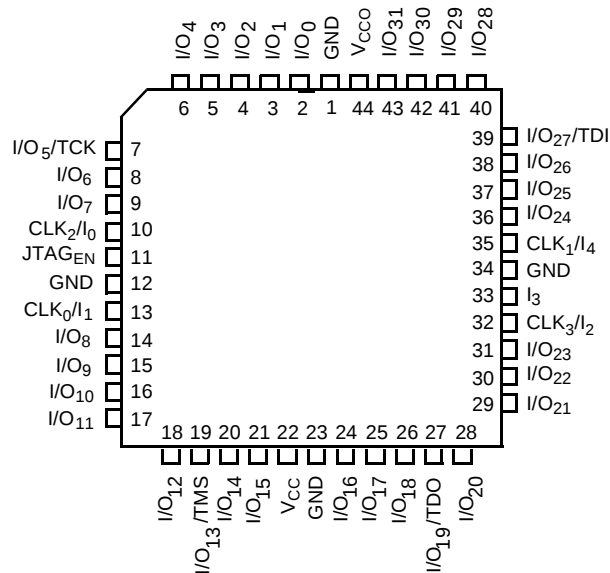
### 44-pin TQFP (A44)

#### Top View



### 44-pin PLCC (J67) / CLCC (Y67)

#### Top View



#### Note:

20. For 3.3V versions (Ultra37000V),  $V_{CCO} = V_{CC}$ .



## Pin Configurations<sup>[20]</sup> (continued)

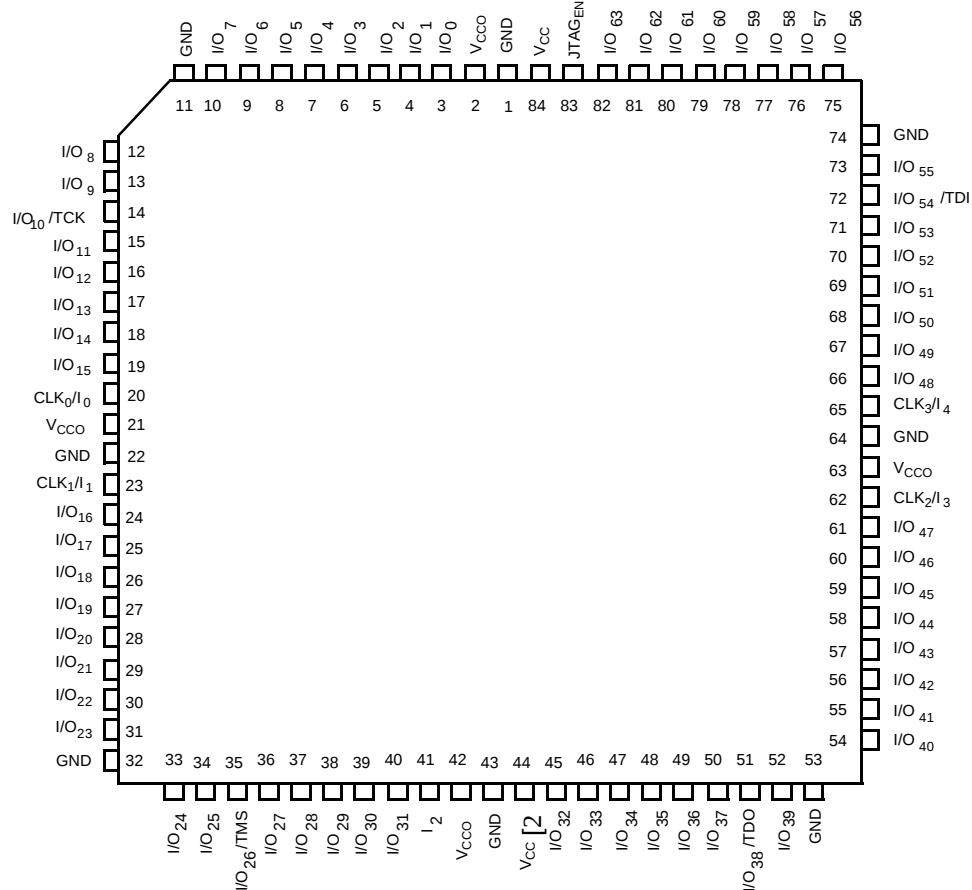
### 48-ball Fine-Pitch BGA (BA50)

#### Top View

|   | 1                                | 2                 | 3                 | 4                 | 5                 | 6                 | 7                 | 8                                |
|---|----------------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|----------------------------------|
| A | I/O <sub>5</sub><br>TCK          | V <sub>CC</sub>   | I/O <sub>3</sub>  | I/O <sub>1</sub>  | I/O <sub>31</sub> | I/O <sub>30</sub> | V <sub>CC</sub>   | I/O <sub>27</sub><br>TDI         |
| B | V <sub>CC</sub>                  | I/O <sub>4</sub>  | I/O <sub>2</sub>  | I/O <sub>0</sub>  | I/O <sub>29</sub> | I/O <sub>28</sub> | I/O <sub>26</sub> | CLK <sub>1</sub> /I <sub>4</sub> |
| C | CLK <sub>2</sub> /I <sub>0</sub> | I/O <sub>7</sub>  | I/O <sub>6</sub>  | GND               | GND               | I/O <sub>25</sub> | I/O <sub>24</sub> | I <sub>3</sub>                   |
| D | JTAG <sub>EN</sub>               | I/O <sub>8</sub>  | I/O <sub>9</sub>  | GND               | GND               | I/O <sub>22</sub> | I/O <sub>23</sub> | CLK <sub>3</sub> /I <sub>2</sub> |
| E | CLK <sub>0</sub> /I <sub>1</sub> | I/O <sub>12</sub> | I/O <sub>11</sub> | I/O <sub>10</sub> | I/O <sub>16</sub> | I/O <sub>20</sub> | I/O <sub>21</sub> | V <sub>CC</sub>                  |
| F | I/O <sub>13</sub><br>TMS         | V <sub>CC</sub>   | I/O <sub>14</sub> | I/O <sub>15</sub> | I/O <sub>17</sub> | I/O <sub>18</sub> | V <sub>CC</sub>   | I/O <sub>19</sub><br>TDO         |

### 84-lead PLCC (J83) / CLCC (Y84)

#### Top View



#### Note:

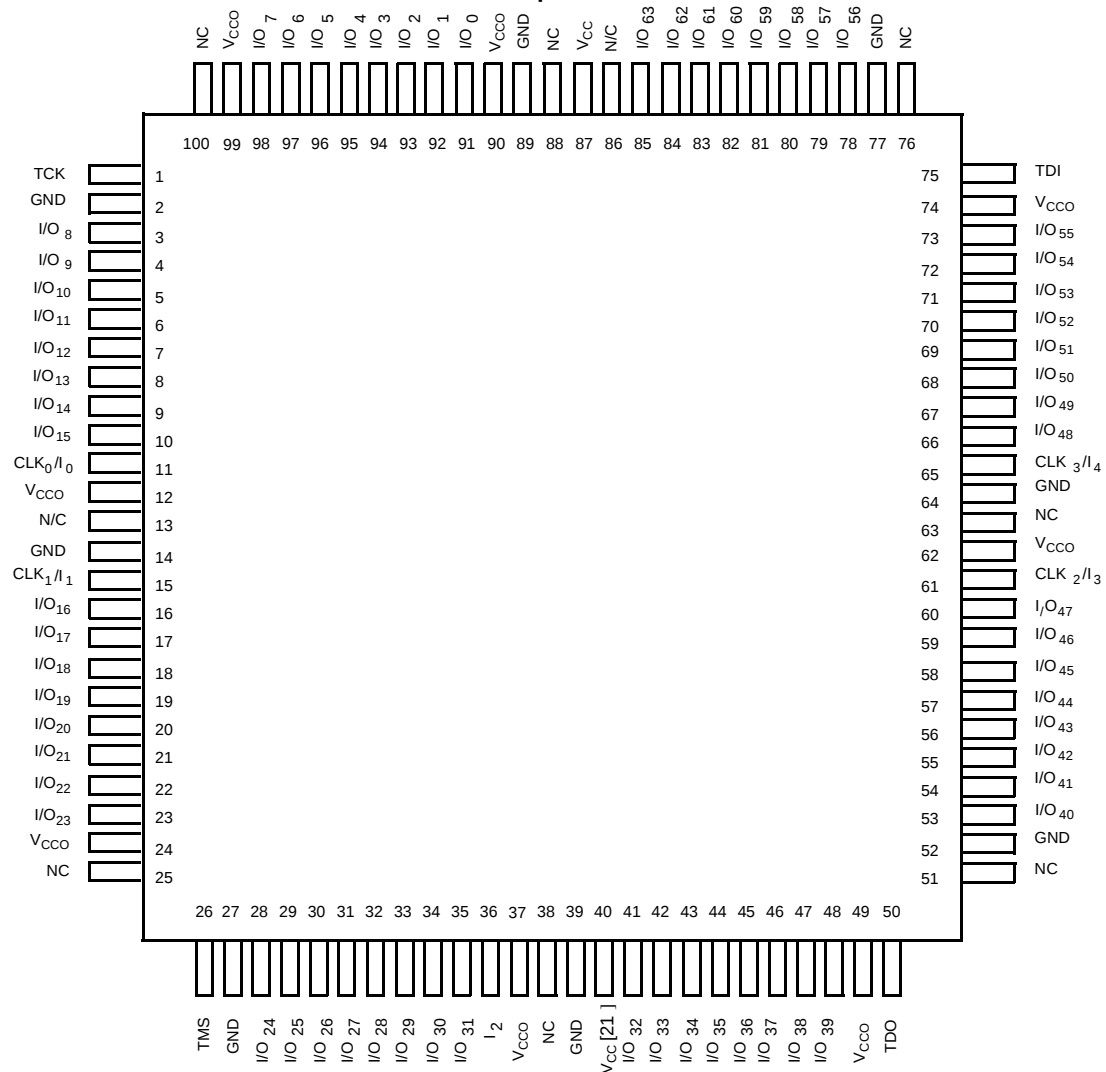
21. This pin is a N/C, but Cypress recommends that you connect it to V<sub>CC</sub> to ensure future compatibility.



## Pin Configurations<sup>[20]</sup> (continued)

### 100-lead TQFP (A100)

#### Top View





## Pin Configurations<sup>[20]</sup> (continued)

### 100-ball Fine-Pitch BGA (BB100) for CY37064V

#### Top View

|   | 1                 | 2                                    | 3                 | 4                 | 5                 | 6                 | 7                 | 8                 | 9                                    | 10                |
|---|-------------------|--------------------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|--------------------------------------|-------------------|
| A | NC                | NC                                   | I/O <sub>7</sub>  | I/O <sub>5</sub>  | I/O <sub>2</sub>  | I/O <sub>62</sub> | I/O <sub>60</sub> | I/O <sub>58</sub> | I/O <sub>57</sub>                    | I/O <sub>56</sub> |
| B | I/O <sub>9</sub>  | I/O <sub>8</sub>                     | I/O <sub>6</sub>  | I/O <sub>4</sub>  | I/O <sub>1</sub>  | I/O <sub>63</sub> | V <sub>CC</sub>   | I/O <sub>59</sub> | I/O <sub>55</sub>                    | NC                |
| C | I/O <sub>10</sub> | TCK                                  | V <sub>CC</sub>   | I/O <sub>3</sub>  | NC                | NC                | I/O <sub>61</sub> | V <sub>CC</sub>   | TDI                                  | I/O <sub>54</sub> |
| D | I/O <sub>11</sub> | NC                                   | I/O <sub>12</sub> | I/O <sub>13</sub> | I/O <sub>0</sub>  | NC                | I/O <sub>51</sub> | I/O <sub>52</sub> | CLK <sub>3</sub><br>/ I <sub>4</sub> | I/O <sub>53</sub> |
| E | I/O <sub>14</sub> | CLK <sub>0</sub><br>/ I <sub>0</sub> | I/O <sub>15</sub> | NC                | GND               | GND               | I/O <sub>48</sub> | I/O <sub>49</sub> | CLK <sub>2</sub><br>/ I <sub>3</sub> | I/O <sub>50</sub> |
| F | I/O <sub>17</sub> | NC                                   | NC                | I/O <sub>16</sub> | GND               | GND               | NC                | NC                | I <sub>2</sub>                       | I/O <sub>47</sub> |
| G | I/O <sub>22</sub> | CLK <sub>1</sub><br>/ I <sub>1</sub> | I/O <sub>21</sub> | I/O <sub>19</sub> | I/O <sub>18</sub> | I/O <sub>46</sub> | I/O <sub>45</sub> | I/O <sub>44</sub> | NC                                   | I/O <sub>43</sub> |
| H | I/O <sub>23</sub> | TMS                                  | V <sub>CC</sub>   | I/O <sub>20</sub> | NC                | I/O <sub>32</sub> | I/O <sub>42</sub> | V <sub>CC</sub>   | TDO                                  | I/O <sub>41</sub> |
| J | NC                | I/O <sub>26</sub>                    | I/O <sub>28</sub> | NC                | I/O <sub>31</sub> | I/O <sub>33</sub> | I/O <sub>35</sub> | I/O <sub>37</sub> | I/O <sub>39</sub>                    | I/O <sub>40</sub> |
| K | I/O <sub>24</sub> | I/O <sub>25</sub>                    | I/O <sub>27</sub> | I/O <sub>29</sub> | I/O <sub>30</sub> | I/O <sub>34</sub> | I/O <sub>36</sub> | I/O <sub>38</sub> | NC                                   | NC                |

### 100-ball Fine-Pitch BGA (BB100) for CY37128V

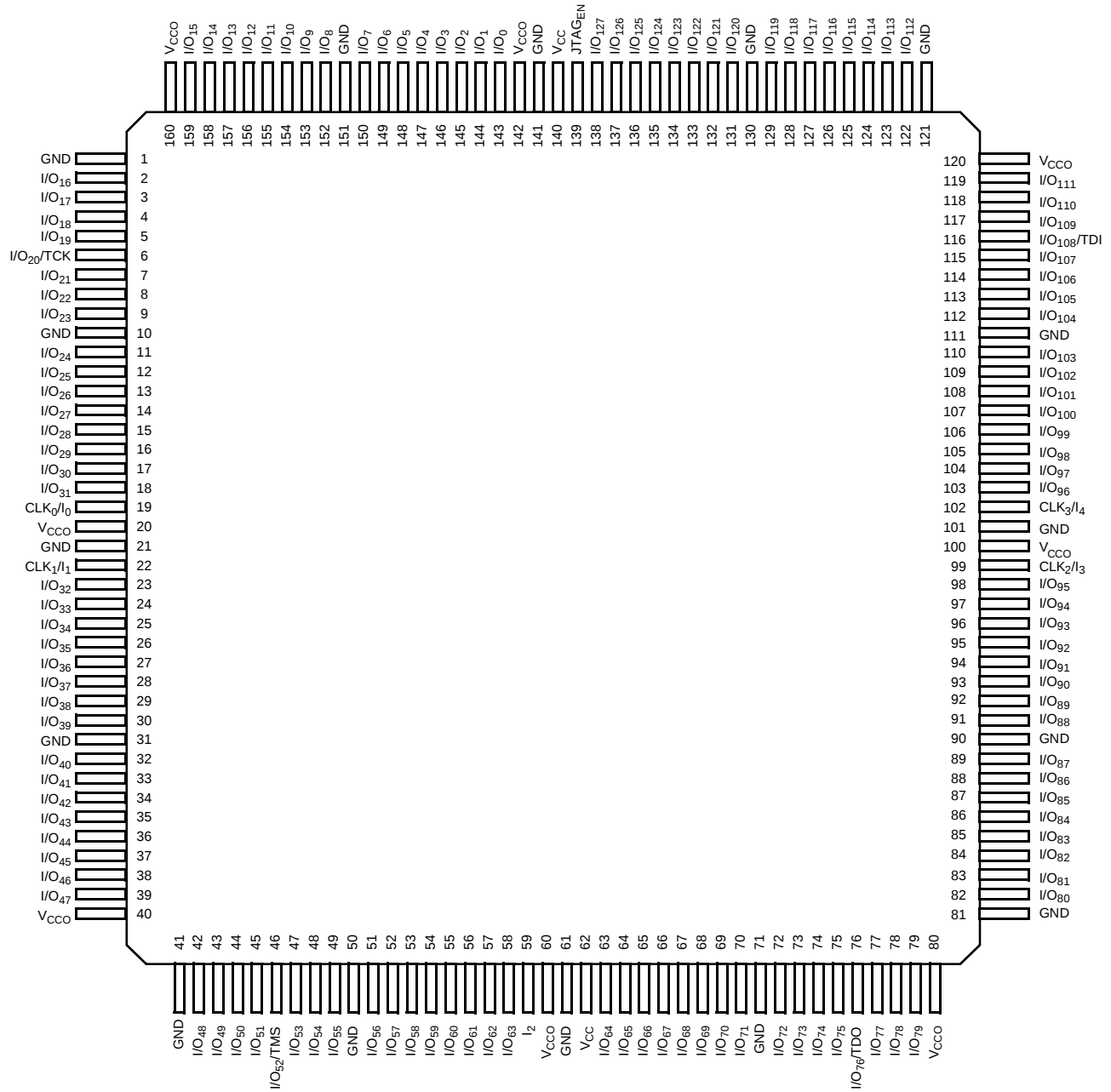
#### Top View

|   | 1                 | 2                                    | 3                 | 4                 | 5                 | 6                 | 7                 | 8                 | 9                                    | 10                |
|---|-------------------|--------------------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|--------------------------------------|-------------------|
| A | NC                | I/O <sub>9</sub>                     | I/O <sub>8</sub>  | I/O <sub>6</sub>  | I/O <sub>3</sub>  | I/O <sub>76</sub> | I/O <sub>74</sub> | I/O <sub>72</sub> | I/O <sub>71</sub>                    | I/O <sub>70</sub> |
| B | I/O <sub>11</sub> | I/O <sub>10</sub>                    | I/O <sub>7</sub>  | I/O <sub>5</sub>  | I/O <sub>2</sub>  | I/O <sub>77</sub> | V <sub>CC</sub>   | I/O <sub>73</sub> | I/O <sub>68</sub>                    | I/O <sub>69</sub> |
| C | I/O <sub>12</sub> | I/O <sub>13</sub><br>TCK             | V <sub>CC</sub>   | I/O <sub>4</sub>  | I/O <sub>1</sub>  | I/O <sub>78</sub> | I/O <sub>75</sub> | V <sub>CC</sub>   | I/O <sub>67</sub><br>TDI             | I/O <sub>66</sub> |
| D | I/O <sub>14</sub> | NC                                   | I/O <sub>15</sub> | I/O <sub>16</sub> | I/O <sub>0</sub>  | I/O <sub>79</sub> | I/O <sub>63</sub> | I/O <sub>64</sub> | CLK <sub>3</sub><br>/ I <sub>4</sub> | I/O <sub>65</sub> |
| E | I/O <sub>17</sub> | CLK <sub>0</sub><br>/ I <sub>0</sub> | I/O <sub>18</sub> | I/O <sub>19</sub> | GND               | GND               | I/O <sub>60</sub> | I/O <sub>61</sub> | CLK <sub>2</sub><br>/ I <sub>3</sub> | I/O <sub>62</sub> |
| F | I/O <sub>22</sub> | JTAG<br>EN                           | I/O <sub>21</sub> | I/O <sub>20</sub> | GND               | GND               | I/O <sub>59</sub> | I/O <sub>58</sub> | I <sub>2</sub>                       | I/O <sub>57</sub> |
| G | I/O <sub>27</sub> | CLK <sub>1</sub><br>/ I <sub>1</sub> | I/O <sub>26</sub> | I/O <sub>24</sub> | I/O <sub>23</sub> | I/O <sub>56</sub> | I/O <sub>55</sub> | I/O <sub>54</sub> | NC                                   | I/O <sub>53</sub> |
| H | I/O <sub>28</sub> | I/O <sub>33</sub><br>TMS             | V <sub>CC</sub>   | I/O <sub>25</sub> | I/O <sub>39</sub> | I/O <sub>40</sub> | I/O <sub>52</sub> | V <sub>CC</sub>   | I/O <sub>47</sub><br>TDO             | I/O <sub>51</sub> |
| J | I/O <sub>29</sub> | I/O <sub>32</sub>                    | I/O <sub>35</sub> | V <sub>CC</sub>   | I/O <sub>38</sub> | I/O <sub>41</sub> | I/O <sub>43</sub> | I/O <sub>45</sub> | I/O <sub>48</sub>                    | I/O <sub>50</sub> |
| K | I/O <sub>30</sub> | I/O <sub>31</sub>                    | I/O <sub>34</sub> | I/O <sub>36</sub> | I/O <sub>37</sub> | I/O <sub>42</sub> | I/O <sub>44</sub> | I/O <sub>46</sub> | I/O <sub>49</sub>                    | NC                |



## Pin Configurations<sup>[20]</sup> (continued)

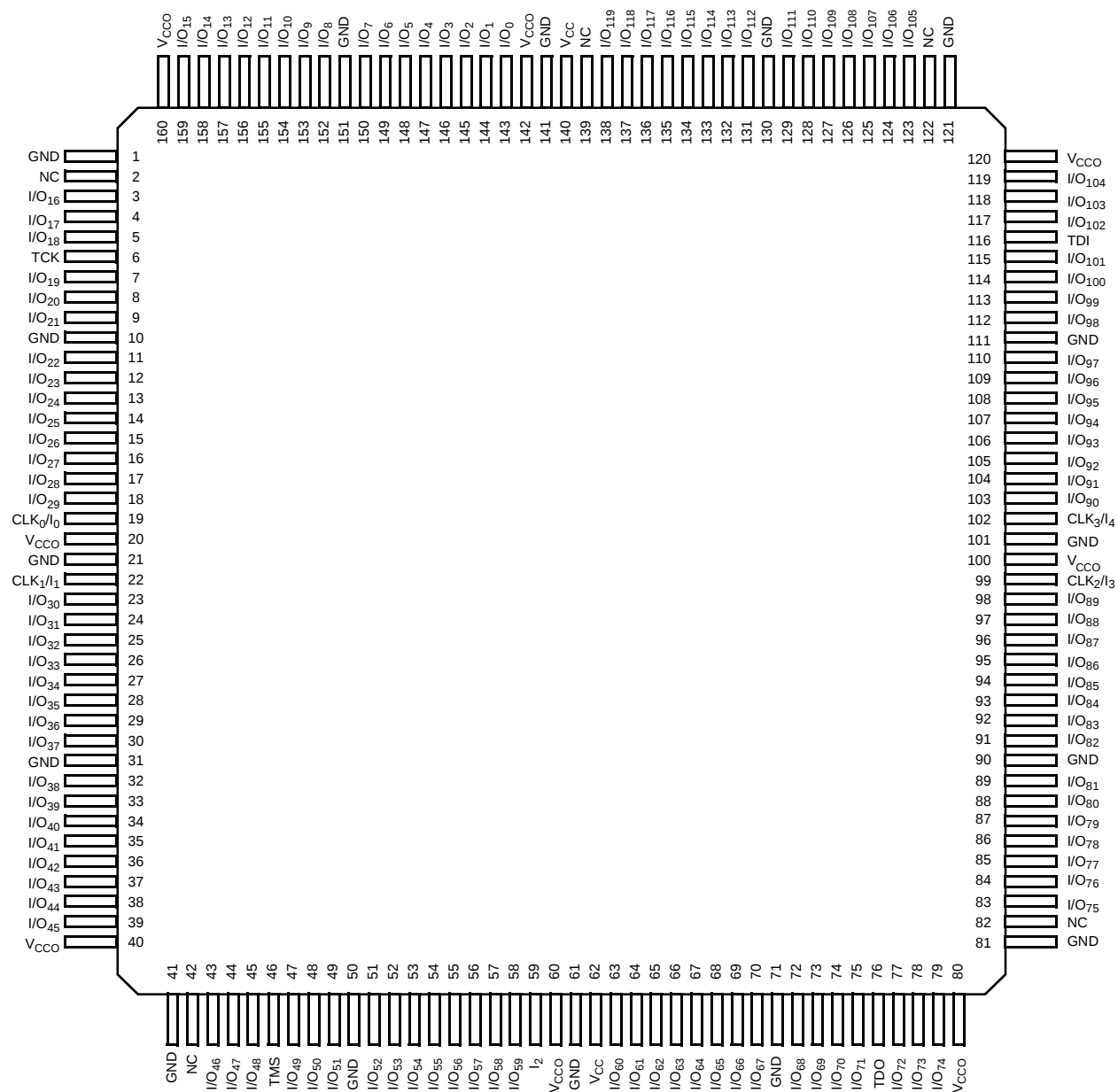
### 160-Lead TQFP (A160) / CQFP (U162) for CY37128(V) and CY37256(V) Top View





## Pin Configurations<sup>[20]</sup> (continued)

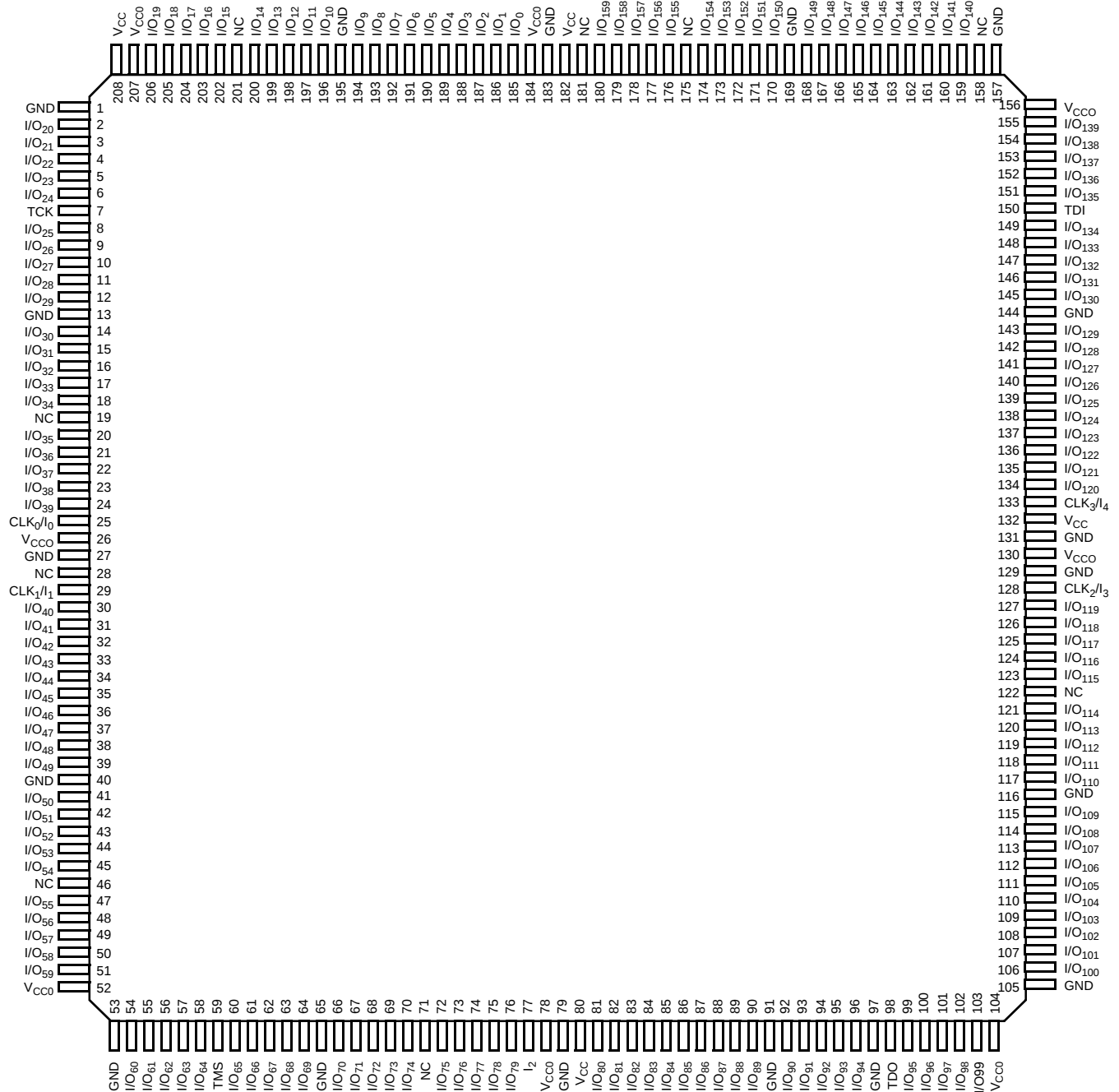
### 160-Lead TQFP (A160) for CY37192(V) Top View





## Pin Configurations<sup>[20]</sup> (continued)

### 208-Lead PQFP (N208) / CQFP (U208) Top View





## Pin Configurations<sup>[20]</sup> (continued)

### 256-Ball PBGA (BG256)

#### Top View

|   | 1                 | 2                                | 3                                | 4                 | 5                 | 6                 | 7                 | 8                 | 9                 | 10                 | 11                 | 12                 | 13                 | 14                 | 15                 | 16                 | 17                 | 18                               | 19                 | 20                 |   |
|---|-------------------|----------------------------------|----------------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|----------------------------------|--------------------|--------------------|---|
| A | GND               | I/O <sub>21</sub>                | NC                               | I/O <sub>16</sub> | I/O <sub>12</sub> | I/O <sub>9</sub>  | I/O <sub>7</sub>  | I/O <sub>4</sub>  | I/O <sub>0</sub>  | I/O <sub>190</sub> | I/O <sub>189</sub> | I/O <sub>186</sub> | I/O <sub>182</sub> | NC                 | I/O <sub>178</sub> | I/O <sub>175</sub> | NC                 | NC                               | I/O <sub>169</sub> | I/O <sub>168</sub> | A |
| B | I/O <sub>23</sub> | I/O <sub>20</sub>                | I/O <sub>19</sub>                | I/O <sub>18</sub> | I/O <sub>15</sub> | I/O <sub>11</sub> | I/O <sub>8</sub>  | I/O <sub>5</sub>  | I/O <sub>1</sub>  | I/O <sub>191</sub> | I/O <sub>187</sub> | I/O <sub>185</sub> | I/O <sub>181</sub> | NC                 | NC                 | I/O <sub>174</sub> | I/O <sub>171</sub> | I/O <sub>170</sub>               | NC                 | I/O <sub>166</sub> | B |
| C | NC                | NC                               | I/O <sub>22</sub>                | NC                | I/O <sub>17</sub> | I/O <sub>14</sub> | I/O <sub>10</sub> | I/O <sub>6</sub>  | I/O <sub>2</sub>  | NC                 | I/O <sub>188</sub> | I/O <sub>184</sub> | I/O <sub>180</sub> | I/O <sub>179</sub> | I/O <sub>176</sub> | I/O <sub>173</sub> | I/O <sub>172</sub> | I/O <sub>167</sub>               | I/O <sub>165</sub> | I/O <sub>162</sub> | C |
| D | I/O <sub>24</sub> | NC                               | NC                               | GND               | NC                | V <sub>CCO</sub>  | I/O <sub>13</sub> | GND               | I/O <sub>3</sub>  | NC                 | V <sub>CC</sub>    | I/O <sub>183</sub> | GND                | I/O <sub>177</sub> | V <sub>CCO</sub>   | NC                 | GND                | I/O <sub>164</sub>               | TDI                | I/O <sub>160</sub> | D |
| E | I/O <sub>27</sub> | I/O <sub>26</sub>                | I/O <sub>25</sub>                | NC                |                   |                   |                   |                   |                   |                    |                    |                    |                    |                    |                    |                    | I/O <sub>163</sub> | I/O <sub>161</sub>               | I/O <sub>159</sub> | I/O <sub>156</sub> | E |
| F | I/O <sub>30</sub> | TCK                              | I/O <sub>28</sub>                | V <sub>CCO</sub>  |                   |                   |                   |                   |                   |                    |                    |                    |                    |                    |                    |                    | V <sub>CCO</sub>   | I/O <sub>158</sub>               | NC                 | I/O <sub>154</sub> | F |
| G | I/O <sub>33</sub> | I/O <sub>32</sub>                | I/O <sub>31</sub>                | I/O <sub>29</sub> |                   |                   |                   |                   |                   |                    |                    |                    |                    |                    |                    |                    | I/O <sub>157</sub> | I/O <sub>155</sub>               | I/O <sub>153</sub> | I/O <sub>152</sub> | G |
| H | I/O <sub>35</sub> | NC                               | I/O <sub>34</sub>                | GND               |                   |                   |                   |                   |                   |                    |                    |                    |                    |                    |                    |                    | GND                | I/O <sub>151</sub>               | I/O <sub>150</sub> | I/O <sub>149</sub> | H |
| J | I/O <sub>39</sub> | I/O <sub>38</sub>                | I/O <sub>37</sub>                | I/O <sub>36</sub> |                   |                   |                   |                   |                   |                    |                    |                    |                    |                    |                    |                    | I/O <sub>148</sub> | I/O <sub>147</sub>               | I/O <sub>146</sub> | I/O <sub>145</sub> | J |
| K | I/O <sub>42</sub> | I/O <sub>40</sub>                | I/O <sub>41</sub>                | V <sub>CC</sub>   |                   |                   |                   |                   |                   |                    |                    |                    |                    |                    |                    |                    | I/O <sub>144</sub> | CLK <sub>3</sub> /I <sub>4</sub> | NC                 | NC                 | K |
| L | I/O <sub>43</sub> | I/O <sub>44</sub>                | I/O <sub>45</sub>                | I/O <sub>46</sub> |                   |                   |                   |                   |                   |                    |                    |                    |                    |                    |                    |                    | V <sub>CC</sub>    | CLK <sub>2</sub> /I <sub>3</sub> | I/O <sub>143</sub> | NC                 | L |
| M | I/O <sub>47</sub> | CLK <sub>0</sub> /I <sub>0</sub> | CLK <sub>1</sub> /I <sub>1</sub> | I/O <sub>48</sub> |                   |                   |                   |                   |                   |                    |                    |                    |                    |                    |                    |                    | I/O <sub>139</sub> | I/O <sub>140</sub>               | I/O <sub>141</sub> | I/O <sub>142</sub> | M |
| N | I/O <sub>49</sub> | I/O <sub>50</sub>                | I/O <sub>51</sub>                | GND               |                   |                   |                   |                   |                   |                    |                    |                    |                    |                    |                    |                    | GND                | I/O <sub>136</sub>               | I/O <sub>137</sub> | I/O <sub>138</sub> | N |
| P | I/O <sub>52</sub> | I/O <sub>53</sub>                | I/O <sub>55</sub>                | I/O <sub>58</sub> |                   |                   |                   |                   |                   |                    |                    |                    |                    |                    |                    |                    | I/O <sub>131</sub> | I/O <sub>133</sub>               | I/O <sub>134</sub> | I/O <sub>135</sub> | P |
| R | I/O <sub>54</sub> | I/O <sub>56</sub>                | I/O <sub>59</sub>                | V <sub>CCO</sub>  |                   |                   |                   |                   |                   |                    |                    |                    |                    |                    |                    |                    | V <sub>CCO</sub>   | I/O <sub>130</sub>               | NC                 | I/O <sub>132</sub> | R |
| T | I/O <sub>57</sub> | I/O <sub>60</sub>                | I/O <sub>62</sub>                | I/O <sub>65</sub> |                   |                   |                   |                   |                   |                    |                    |                    |                    |                    |                    |                    | I/O <sub>124</sub> | I/O <sub>127</sub>               | I/O <sub>128</sub> | I/O <sub>129</sub> | T |
| U | I/O <sub>61</sub> | I/O <sub>63</sub>                | I/O <sub>66</sub>                | GND               | I/O <sub>76</sub> | V <sub>CCO</sub>  | I/O <sub>82</sub> | GND               | I/O <sub>91</sub> | V <sub>CC</sub>    | I/O <sub>98</sub>  | I/O <sub>102</sub> | GND                | I/O <sub>112</sub> | V <sub>CCO</sub>   | NC                 | GND                | I/O <sub>123</sub>               | I/O <sub>122</sub> | I/O <sub>126</sub> | U |
| V | I/O <sub>64</sub> | I/O <sub>67</sub>                | I/O <sub>69</sub>                | I/O <sub>75</sub> | I/O <sub>78</sub> | I/O <sub>81</sub> | I/O <sub>85</sub> | I/O <sub>88</sub> | I/O <sub>92</sub> | I <sub>2</sub>     | I/O <sub>97</sub>  | I/O <sub>101</sub> | I/O <sub>105</sub> | I/O <sub>109</sub> | I/O <sub>113</sub> | TD0                | I/O <sub>114</sub> | I/O <sub>117</sub>               | I/O <sub>121</sub> | I/O <sub>125</sub> | V |
| W | I/O <sub>68</sub> | I/O <sub>70</sub>                | I/O <sub>72</sub>                | I/O <sub>74</sub> | I/O <sub>79</sub> | I/O <sub>83</sub> | I/O <sub>86</sub> | I/O <sub>89</sub> | I/O <sub>93</sub> | I/O <sub>95</sub>  | I/O <sub>96</sub>  | I/O <sub>100</sub> | I/O <sub>104</sub> | I/O <sub>107</sub> | I/O <sub>110</sub> | NC                 | NC                 | I/O <sub>115</sub>               | I/O <sub>118</sub> | I/O <sub>120</sub> | W |
| Y | I/O <sub>71</sub> | I/O <sub>73</sub>                | I/O <sub>77</sub>                | TMS               | I/O <sub>80</sub> | I/O <sub>84</sub> | I/O <sub>87</sub> | I/O <sub>90</sub> | I/O <sub>94</sub> | NC                 | NC                 | I/O <sub>99</sub>  | I/O <sub>103</sub> | I/O <sub>106</sub> | I/O <sub>108</sub> | I/O <sub>111</sub> | NC                 | NC                               | I/O <sub>116</sub> | I/O <sub>119</sub> | Y |
|   | 1                 | 2                                | 3                                | 4                 | 5                 | 6                 | 7                 | 8                 | 9                 | 10                 | 11                 | 12                 | 13                 | 14                 | 15                 | 16                 | 17                 | 18                               | 19                 | 20                 |   |



## Pin Configurations<sup>[20]</sup> (continued)

### 256-Ball Fine-Pitch BGA (BB256)

#### Top View

|   | 1                 | 2                 | 3                 | 4                 | 5                                    | 6                 | 7                 | 8                 | 9                              | 10                             | 11                             | 12                                    | 13                             | 14                             | 15                             | 16                             |
|---|-------------------|-------------------|-------------------|-------------------|--------------------------------------|-------------------|-------------------|-------------------|--------------------------------|--------------------------------|--------------------------------|---------------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
| A | GND               | GND               | I/O <sub>26</sub> | I/O <sub>24</sub> | I/O <sub>20</sub>                    | V <sub>CC</sub>   | I/O <sub>11</sub> | GND               | GND                            | I/O <sub>18</sub> <sub>6</sub> | V <sub>CC</sub>                | I/O <sub>17</sub> <sub>7</sub>        | I/O <sub>17</sub> <sub>2</sub> | I/O <sub>16</sub> <sub>7</sub> | GND                            | GND                            |
| B | GND               | I/O <sub>27</sub> | I/O <sub>25</sub> | I/O <sub>23</sub> | I/O <sub>19</sub>                    | I/O <sub>15</sub> | I/O <sub>10</sub> | GND               | GND                            | I/O <sub>18</sub> <sub>5</sub> | I/O <sub>18</sub> <sub>1</sub> | I/O <sub>17</sub> <sub>6</sub>        | I/O <sub>17</sub> <sub>1</sub> | I/O <sub>16</sub> <sub>6</sub> | I/O <sub>16</sub> <sub>5</sub> | GND                            |
| C | I/O <sub>29</sub> | I/O <sub>28</sub> | NC                | I/O <sub>22</sub> | I/O <sub>18</sub>                    | I/O <sub>14</sub> | I/O <sub>9</sub>  | I/O <sub>4</sub>  | I/O <sub>19</sub> <sub>1</sub> | I/O <sub>18</sub> <sub>4</sub> | I/O <sub>18</sub> <sub>0</sub> | I/O <sub>17</sub> <sub>5</sub>        | I/O <sub>17</sub> <sub>0</sub> | NC                             | I/O <sub>16</sub> <sub>3</sub> | I/O <sub>16</sub> <sub>4</sub> |
| D | I/O <sub>32</sub> | I/O <sub>31</sub> | I/O <sub>30</sub> | NC                | I/O <sub>17</sub>                    | I/O <sub>13</sub> | I/O <sub>8</sub>  | I/O <sub>3</sub>  | I/O <sub>19</sub> <sub>0</sub> | I/O <sub>18</sub> <sub>3</sub> | I/O <sub>17</sub> <sub>9</sub> | I/O <sub>17</sub> <sub>4</sub>        | I/O <sub>16</sub> <sub>9</sub> | I/O <sub>16</sub> <sub>0</sub> | I/O <sub>16</sub> <sub>1</sub> | I/O <sub>16</sub> <sub>2</sub> |
| E | I/O <sub>35</sub> | I/O <sub>34</sub> | I/O <sub>33</sub> | I/O <sub>21</sub> | I/O <sub>16</sub>                    | I/O <sub>12</sub> | I/O <sub>7</sub>  | I/O <sub>2</sub>  | I/O <sub>18</sub> <sub>9</sub> | V <sub>CC</sub>                | I/O <sub>17</sub> <sub>8</sub> | I/O <sub>17</sub> <sub>3</sub>        | I/O <sub>16</sub> <sub>8</sub> | I/O <sub>15</sub> <sub>7</sub> | I/O <sub>15</sub> <sub>8</sub> | I/O <sub>15</sub> <sub>9</sub> |
| F | V <sub>CC</sub>   | I/O <sub>38</sub> | I/O <sub>37</sub> | I/O <sub>36</sub> | TCK                                  | V <sub>CC</sub>   | I/O <sub>6</sub>  | I/O <sub>1</sub>  | I/O <sub>18</sub> <sub>8</sub> | I/O <sub>18</sub> <sub>2</sub> | V <sub>CC</sub>                | TDI                                   | I/O <sub>15</sub> <sub>4</sub> | I/O <sub>15</sub> <sub>5</sub> | I/O <sub>15</sub> <sub>6</sub> | V <sub>CC</sub>                |
| G | I/O <sub>43</sub> | I/O <sub>42</sub> | I/O <sub>41</sub> | I/O <sub>40</sub> | V <sub>CC</sub>                      | I/O <sub>39</sub> | I/O <sub>5</sub>  | I/O <sub>0</sub>  | I/O <sub>18</sub> <sub>7</sub> | I/O <sub>14</sub> <sub>8</sub> | I/O <sub>14</sub> <sub>9</sub> | CLK <sub>3</sub><br>I/O <sub>14</sub> | I/O <sub>15</sub> <sub>0</sub> | I/O <sub>15</sub> <sub>1</sub> | I/O <sub>15</sub> <sub>2</sub> | I/O <sub>15</sub> <sub>3</sub> |
| H | GND               | GND               | I/O <sub>47</sub> | I/O <sub>46</sub> | CLK <sub>0</sub><br>I/O <sub>4</sub> | I/O <sub>45</sub> | I/O <sub>44</sub> | GND               | GND                            | I/O <sub>14</sub> <sub>4</sub> | I/O <sub>14</sub> <sub>5</sub> | CLK <sub>2</sub><br>I/O <sub>14</sub> | I/O <sub>14</sub> <sub>6</sub> | I/O <sub>14</sub> <sub>7</sub> | GND                            | GND                            |
| J | GND               | GND               | I/O <sub>51</sub> | I/O <sub>50</sub> | NC                                   | I/O <sub>49</sub> | I/O <sub>48</sub> | GND               | GND                            | I/O <sub>14</sub> <sub>0</sub> | I/O <sub>14</sub> <sub>1</sub> | I <sub>2</sub>                        | I/O <sub>14</sub> <sub>2</sub> | I/O <sub>14</sub> <sub>3</sub> | GND                            | GND                            |
| K | I/O <sub>57</sub> | I/O <sub>56</sub> | I/O <sub>55</sub> | I/O <sub>54</sub> | CLK <sub>1</sub><br>I/O <sub>1</sub> | I/O <sub>53</sub> | I/O <sub>52</sub> | I/O <sub>91</sub> | I/O <sub>96</sub>              | I/O <sub>10</sub> <sub>1</sub> | I/O <sub>13</sub> <sub>5</sub> | V <sub>CC</sub>                       | I/O <sub>13</sub> <sub>6</sub> | I/O <sub>13</sub> <sub>7</sub> | I/O <sub>13</sub> <sub>8</sub> | I/O <sub>13</sub> <sub>9</sub> |
| L | V <sub>CC</sub>   | I/O <sub>60</sub> | I/O <sub>59</sub> | I/O <sub>58</sub> | TMS                                  | V <sub>CC</sub>   | I/O <sub>86</sub> | I/O <sub>92</sub> | I/O <sub>97</sub>              | I/O <sub>10</sub> <sub>2</sub> | V <sub>CC</sub>                | TDO                                   | I/O <sub>13</sub> <sub>2</sub> | I/O <sub>13</sub> <sub>3</sub> | I/O <sub>13</sub> <sub>4</sub> | V <sub>CC</sub>                |
| M | I/O <sub>63</sub> | I/O <sub>62</sub> | I/O <sub>61</sub> | I/O <sub>72</sub> | I/O <sub>77</sub>                    | I/O <sub>82</sub> | V <sub>CC</sub>   | I/O <sub>93</sub> | I/O <sub>98</sub>              | I/O <sub>10</sub> <sub>3</sub> | I/O <sub>10</sub> <sub>8</sub> | I/O <sub>11</sub> <sub>2</sub>        | I/O <sub>11</sub> <sub>7</sub> | I/O <sub>12</sub> <sub>9</sub> | I/O <sub>13</sub> <sub>0</sub> | I/O <sub>13</sub> <sub>1</sub> |
| N | I/O <sub>66</sub> | I/O <sub>65</sub> | I/O <sub>64</sub> | I/O <sub>73</sub> | I/O <sub>78</sub>                    | I/O <sub>83</sub> | I/O <sub>87</sub> | I/O <sub>94</sub> | I/O <sub>99</sub>              | I/O <sub>10</sub> <sub>4</sub> | I/O <sub>10</sub> <sub>9</sub> | I/O <sub>11</sub> <sub>3</sub>        | NC                             | I/O <sub>12</sub> <sub>6</sub> | I/O <sub>12</sub> <sub>7</sub> | I/O <sub>12</sub> <sub>8</sub> |
| P | I/O <sub>68</sub> | I/O <sub>67</sub> | NC                | I/O <sub>74</sub> | I/O <sub>79</sub>                    | I/O <sub>84</sub> | I/O <sub>88</sub> | I/O <sub>95</sub> | I/O <sub>10</sub> <sub>0</sub> | I/O <sub>10</sub> <sub>5</sub> | I/O <sub>11</sub> <sub>0</sub> | I/O <sub>11</sub> <sub>4</sub>        | I/O <sub>11</sub> <sub>8</sub> | NC                             | I/O <sub>12</sub> <sub>4</sub> | I/O <sub>12</sub> <sub>5</sub> |
| R | GND               | I/O <sub>69</sub> | I/O <sub>70</sub> | I/O <sub>75</sub> | I/O <sub>80</sub>                    | I/O <sub>85</sub> | I/O <sub>89</sub> | GND               | GND                            | I/O <sub>10</sub> <sub>6</sub> | I/O <sub>11</sub> <sub>1</sub> | I/O <sub>11</sub> <sub>5</sub>        | I/O <sub>11</sub> <sub>9</sub> | I/O <sub>12</sub> <sub>1</sub> | I/O <sub>12</sub> <sub>3</sub> | GND                            |
| T | GND               | GND               | I/O <sub>71</sub> | I/O <sub>76</sub> | I/O <sub>81</sub>                    | V <sub>CC</sub>   | I/O <sub>90</sub> | GND               | GND                            | I/O <sub>10</sub> <sub>7</sub> | V <sub>CC</sub>                | I/O <sub>11</sub> <sub>6</sub>        | I/O <sub>12</sub> <sub>0</sub> | I/O <sub>12</sub> <sub>2</sub> | GND                            | GND                            |



## Pin Configurations<sup>[20]</sup> (continued)

### 352-Lead BGA (BG352)

#### Top View

|    | 1                  | 2                 | 3                  | 4                  | 5                  | 6                  | 7                  | 8                  | 9                  | 10                 | 11                 | 12                 | 13                 | 14                 | 15                 | 16                 | 17                 | 18                 | 19                 | 20                 | 21                 | 22                 | 23                 | 24                 | 25                 | 26                 |
|----|--------------------|-------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| A  | GND                | GND               | I/O <sub>19</sub>  | I/O <sub>15</sub>  | I/O <sub>13</sub>  | I/O <sub>34</sub>  | I/O <sub>31</sub>  | I/O <sub>28</sub>  | I/O <sub>25</sub>  | I/O <sub>10</sub>  | I/O <sub>7</sub>   | I/O <sub>4</sub>   | I/O <sub>1</sub>   | I/O <sub>263</sub> | I/O <sub>260</sub> | I/O <sub>257</sub> | I/O <sub>254</sub> | I/O <sub>239</sub> | I/O <sub>237</sub> | I/O <sub>232</sub> | I/O <sub>229</sub> | I/O <sub>250</sub> | I/O <sub>248</sub> | I/O <sub>244</sub> | GND                | GND                |
| B  | GND                | NC                | I/O <sub>18</sub>  | I/O <sub>17</sub>  | I/O <sub>14</sub>  | I/O <sub>35</sub>  | I/O <sub>32</sub>  | I/O <sub>29</sub>  | I/O <sub>26</sub>  | I/O <sub>11</sub>  | I/O <sub>8</sub>   | I/O <sub>5</sub>   | I/O <sub>2</sub>   | V <sub>CC</sub>    | I/O <sub>261</sub> | I/O <sub>258</sub> | I/O <sub>255</sub> | I/O <sub>252</sub> | I/O <sub>234</sub> | I/O <sub>231</sub> | I/O <sub>228</sub> | I/O <sub>249</sub> | I/O <sub>246</sub> | I/O <sub>245</sub> | I/O <sub>240</sub> | GND                |
| C  | I/O <sub>23</sub>  | I/O <sub>38</sub> | I/O <sub>37</sub>  | I/O <sub>16</sub>  | I/O <sub>12</sub>  | I/O <sub>33</sub>  | I/O <sub>30</sub>  | I/O <sub>27</sub>  | I/O <sub>24</sub>  | I/O <sub>9</sub>   | I/O <sub>6</sub>   | I/O <sub>3</sub>   | I/O <sub>0</sub>   | I/O <sub>262</sub> | I/O <sub>259</sub> | I/O <sub>256</sub> | I/O <sub>253</sub> | I/O <sub>238</sub> | I/O <sub>235</sub> | I/O <sub>233</sub> | I/O <sub>230</sub> | I/O <sub>251</sub> | I/O <sub>247</sub> | I/O <sub>225</sub> | I/O <sub>224</sub> | I/O <sub>227</sub> |
| D  | I/O <sub>39</sub>  | I/O <sub>40</sub> | I/O <sub>36</sub>  | NC                 | NC                 | I/O <sub>21</sub>  | I/O <sub>20</sub>  | V <sub>CCO</sub>   | V <sub>CCO</sub>   | NC                 | GND                | GND                | V <sub>CCO</sub>   | V <sub>CCO</sub>   | GND                | GND                | NC                 | V <sub>CCO</sub>   | V <sub>CCO</sub>   | I/O <sub>236</sub> | I/O <sub>243</sub> | NC                 | NC                 | I/O <sub>226</sub> | I/O <sub>222</sub> | I/O <sub>223</sub> |
| E  | I/O <sub>42</sub>  | TCK               | I/O <sub>41</sub>  | NC                 |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | NC                 | TDI                | I/O <sub>221</sub> | I/O <sub>220</sub> |
| F  | I/O <sub>45</sub>  | I/O <sub>44</sub> | I/O <sub>43</sub>  | I/O <sub>22</sub>  |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | I/O <sub>242</sub> | I/O <sub>219</sub> | I/O <sub>218</sub> | I/O <sub>217</sub> |
| G  | I/O <sub>48</sub>  | I/O <sub>47</sub> | I/O <sub>46</sub>  | I/O <sub>63</sub>  |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | I/O <sub>241</sub> | I/O <sub>216</sub> | I/O <sub>215</sub> | I/O <sub>214</sub> |
| H  | I/O <sub>49</sub>  | I/O <sub>50</sub> | I/O <sub>51</sub>  | V <sub>CCO</sub>   |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | V <sub>CCO</sub>   | I/O <sub>211</sub> | I/O <sub>212</sub> | I/O <sub>213</sub> |
| J  | I/O <sub>52</sub>  | I/O <sub>53</sub> | I/O <sub>54</sub>  | V <sub>CCO</sub>   |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | V <sub>CCO</sub>   | I/O <sub>208</sub> | I/O <sub>209</sub> | I/O <sub>210</sub> |
| K  | I/O <sub>55</sub>  | I/O <sub>56</sub> | I/O <sub>57</sub>  | NC                 |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | NC                 | I/O <sub>205</sub> | I/O <sub>206</sub> | I/O <sub>207</sub> |
| L  | I/O                | I/O <sub>59</sub> | I/O <sub>58</sub>  | GND                |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | GND                | I/O <sub>204</sub> | I/O <sub>197</sub> | I/O <sub>197</sub> |
| M  | I/O <sub>61</sub>  | I/O <sub>60</sub> | I/O <sub>61</sub>  | GND                |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | GND                | I/O <sub>203</sub> | I/O <sub>202</sub> | I/O <sub>202</sub> |
| N  | I/O <sub>64</sub>  | V <sub>CC</sub>   | I/O <sub>62</sub>  | V <sub>CCO</sub>   |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | V <sub>CCO</sub>   | I/O <sub>201</sub> | I/O <sub>200</sub> | I/O <sub>199</sub> |
| P  | I/O <sub>65</sub>  | I/O <sub>66</sub> | I/O <sub>67</sub>  | V <sub>CCO</sub>   |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | V <sub>CCO</sub>   | I/O <sub>196</sub> | V <sub>CC</sub>    | I/O <sub>198</sub> |
| R  | I/O <sub>68</sub>  | I/O <sub>69</sub> | I/O <sub>70</sub>  | GND                |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | GND                | I/O <sub>193</sub> | I/O <sub>194</sub> | I/O <sub>195</sub> |
| T  | I/O <sub>71</sub>  | I/O <sub>84</sub> | I/O <sub>85</sub>  | GND                |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | GND                | I/O <sub>178</sub> | I/O <sub>179</sub> | I/O <sub>192</sub> |
| U  | I/O <sub>88</sub>  | I/O <sub>87</sub> | I/O <sub>86</sub>  | NC                 |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | NC                 | I/O <sub>177</sub> | I/O <sub>176</sub> | I/O <sub>175</sub> |
| V  | I/O <sub>91</sub>  | I/O <sub>90</sub> | I/O <sub>89</sub>  | V <sub>CCO</sub>   |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | V <sub>CCO</sub>   | I/O <sub>174</sub> | I/O <sub>173</sub> | I/O <sub>172</sub> |
| W  | I/O <sub>94</sub>  | I/O <sub>93</sub> | I/O <sub>92</sub>  | V <sub>CCO</sub>   |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | V <sub>CCO</sub>   | I/O <sub>171</sub> | I/O <sub>170</sub> | I/O <sub>169</sub> |
| Y  | I/O <sub>95</sub>  | I/O <sub>72</sub> | I/O <sub>73</sub>  | I/O <sub>110</sub> |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | I/O <sub>153</sub> | I/O <sub>190</sub> | I/O <sub>191</sub> | I/O <sub>168</sub> |
| AA | I/O <sub>74</sub>  | I/O <sub>75</sub> | I/O <sub>76</sub>  | I/O <sub>111</sub> |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | I/O <sub>152</sub> | I/O <sub>187</sub> | I/O <sub>188</sub> | I/O <sub>189</sub> |
| AB | I/O <sub>77</sub>  | I/O <sub>78</sub> | I/O <sub>79</sub>  | NC                 |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    | NC                 | I/O <sub>184</sub> | I/O <sub>185</sub> | I/O <sub>186</sub> |
| AC | I/O <sub>81</sub>  | I/O <sub>80</sub> | I/O <sub>108</sub> | NC                 | NC                 | I/O <sub>112</sub> | I/O <sub>113</sub> | V <sub>CCO</sub>   | V <sub>CCO</sub>   | NC                 | GND                | GND                | V <sub>CCO</sub>   | V <sub>CCO</sub>   | GND                | GND                | NC                 | V <sub>CCO</sub>   | V <sub>CCO</sub>   | I/O <sub>150</sub> | I/O <sub>151</sub> | NC                 | NC                 | I/O <sub>155</sub> | I/O <sub>183</sub> | I/O <sub>182</sub> |
| AD | I/O <sub>109</sub> | I/O <sub>82</sub> | I/O <sub>83</sub>  | I/O <sub>117</sub> | I/O <sub>97</sub>  | I/O <sub>100</sub> | I/O <sub>102</sub> | I/O <sub>105</sub> | I/O <sub>120</sub> | I/O <sub>123</sub> | I/O <sub>126</sub> | I/O <sub>129</sub> | I/O <sub>12</sub>  | I/O <sub>133</sub> | I/O <sub>136</sub> | I/O <sub>139</sub> | I/O <sub>142</sub> | I/O <sub>157</sub> | I/O <sub>159</sub> | I/O <sub>161</sub> | I/O <sub>163</sub> | I/O <sub>166</sub> | I/O <sub>146</sub> | I/O <sub>180</sub> | I/O <sub>181</sub> | I/O <sub>154</sub> |
| AE | GND                | NC                | I/O <sub>115</sub> | I/O <sub>116</sub> | I/O <sub>119</sub> | I/O <sub>98</sub>  | I/O <sub>101</sub> | I/O <sub>103</sub> | I/O <sub>106</sub> | I/O <sub>121</sub> | I/O <sub>124</sub> | I/O <sub>127</sub> | V <sub>CC</sub>    | I/O <sub>130</sub> | I/O <sub>134</sub> | I/O <sub>137</sub> | I/O <sub>140</sub> | I/O <sub>143</sub> | I/O <sub>160</sub> | I/O <sub>162</sub> | I/O <sub>165</sub> | I/O <sub>144</sub> | I/O <sub>147</sub> | I/O <sub>148</sub> | NC                 | GND                |
| AF | GND                | GND               | I/O <sub>114</sub> | I/O <sub>118</sub> | I/O <sub>96</sub>  | I/O <sub>99</sub>  | TMS                | I/O <sub>104</sub> | I/O <sub>107</sub> | I/O <sub>122</sub> | I/O <sub>125</sub> | I/O <sub>128</sub> | I/O <sub>131</sub> | I/O <sub>132</sub> | I/O <sub>135</sub> | I/O <sub>138</sub> | I/O <sub>141</sub> | I/O <sub>156</sub> | I/O <sub>158</sub> | TDO                | I/O <sub>164</sub> | I/O <sub>167</sub> | I/O <sub>145</sub> | I/O <sub>149</sub> | GND                | GND                |



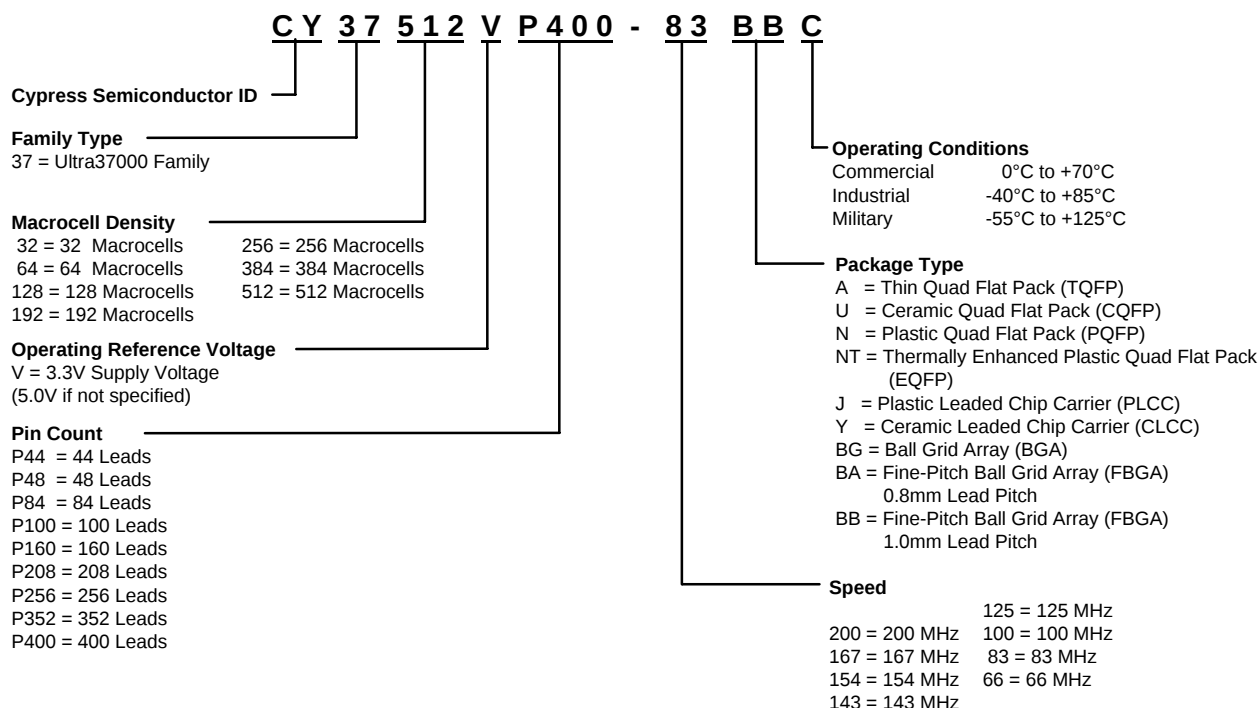
## Pin Configurations<sup>[20]</sup> (continued)

### 400-Ball Fine-Pitch BGA (BB400)

#### Top View

|   |                   |                   |                                |                                |                                |                                |                                  |                                |                                |                                |                                |                                |                                |                                  |                                |                                |                                |                                |                                |                                |
|---|-------------------|-------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|----------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|----------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
| A | GND               | GND               | NC                             | I/O <sub>17</sub>              | I/O <sub>16</sub>              | I/O <sub>14</sub>              | I/O <sub>29</sub>                | V <sub>CC</sub>                | I/O <sub>11</sub>              | GND                            | GND                            | I/O <sub>25</sub> <sub>7</sub> | V <sub>CC</sub>                | I/O <sub>23</sub> <sub>9</sub>   | I/O <sub>23</sub> <sub>3</sub> | I/O <sub>23</sub> <sub>2</sub> | I/O <sub>23</sub> <sub>0</sub> | NC                             | GND                            | GND                            |
| B | GND               | GND               | GND                            | NC                             | I/O <sub>15</sub>              | I/O <sub>13</sub>              | I/O <sub>28</sub>                | V <sub>CC</sub>                | I/O <sub>10</sub>              | GND                            | GND                            | I/O <sub>25</sub> <sub>6</sub> | V <sub>CC</sub>                | I/O <sub>23</sub> <sub>8</sub>   | I/O <sub>23</sub> <sub>1</sub> | I/O <sub>22</sub> <sub>9</sub> | NC                             | GND                            | GND                            | GND                            |
| C | NC                | GND               | GND                            | GND                            | I/O <sub>20</sub>              | I/O <sub>12</sub>              | I/O <sub>27</sub>                | V <sub>CC</sub>                | I/O <sub>9</sub>               | GND                            | GND                            | I/O <sub>25</sub> <sub>5</sub> | V <sub>CC</sub>                | I/O <sub>23</sub> <sub>7</sub>   | I/O <sub>22</sub> <sub>8</sub> | I/O <sub>24</sub> <sub>5</sub> | GND                            | GND                            | GND                            | NC                             |
| D | I/O <sub>44</sub> | NC                | GND                            | I/O <sub>21</sub>              | I/O <sub>19</sub>              | I/O <sub>18</sub>              | I/O <sub>26</sub>                | I/O <sub>25</sub>              | I/O <sub>8</sub>               | GND                            | GND                            | I/O <sub>25</sub> <sub>4</sub> | I/O <sub>23</sub> <sub>5</sub> | I/O <sub>23</sub> <sub>6</sub>   | I/O <sub>25</sub> <sub>1</sub> | I/O <sub>24</sub> <sub>4</sub> | I/O <sub>24</sub> <sub>3</sub> | GND                            | NC                             | I/O <sub>22</sub> <sub>7</sub> |
| E | I/O <sub>46</sub> | I/O <sub>43</sub> | I/O <sub>23</sub>              | I/O <sub>22</sub>              | NC                             | I/O <sub>35</sub>              | I/O <sub>34</sub>                | I/O <sub>24</sub>              | I/O <sub>7</sub>               | I/O <sub>4</sub>               | I/O <sub>26</sub> <sub>3</sub> | I/O <sub>25</sub> <sub>3</sub> | I/O <sub>23</sub> <sub>4</sub> | I/O <sub>25</sub> <sub>0</sub>   | I/O <sub>24</sub> <sub>8</sub> | NC                             | I/O <sub>24</sub> <sub>1</sub> | I/O <sub>24</sub> <sub>2</sub> | I/O <sub>22</sub> <sub>5</sub> | I/O <sub>22</sub> <sub>6</sub> |
| F | I/O <sub>47</sub> | I/O <sub>45</sub> | I/O <sub>42</sub>              | I/O <sub>41</sub>              | I/O <sub>40</sub>              | NC                             | I/O <sub>33</sub>                | I/O <sub>32</sub>              | I/O <sub>6</sub>               | I/O <sub>3</sub>               | I/O <sub>26</sub> <sub>2</sub> | I/O <sub>25</sub> <sub>2</sub> | I/O <sub>24</sub> <sub>9</sub> | I/O <sub>24</sub> <sub>7</sub>   | I/O <sub>22</sub> <sub>0</sub> | I/O <sub>22</sub> <sub>1</sub> | I/O <sub>24</sub> <sub>0</sub> | I/O <sub>22</sub> <sub>2</sub> | I/O <sub>22</sub> <sub>3</sub> | I/O <sub>22</sub> <sub>4</sub> |
| G | I/O <sub>53</sub> | I/O <sub>52</sub> | I/O <sub>51</sub>              | I/O <sub>50</sub>              | I/O <sub>39</sub>              | I/O <sub>38</sub>              | I/O <sub>37</sub>                | I/O <sub>31</sub>              | I/O <sub>5</sub>               | I/O <sub>2</sub>               | I/O <sub>26</sub> <sub>1</sub> | V <sub>CC</sub>                | I/O <sub>24</sub> <sub>6</sub> | I/O <sub>21</sub> <sub>7</sub>   | I/O <sub>21</sub> <sub>8</sub> | I/O <sub>21</sub> <sub>9</sub> | I/O <sub>21</sub> <sub>2</sub> | I/O <sub>21</sub> <sub>3</sub> | I/O <sub>21</sub> <sub>4</sub> | I/O <sub>21</sub> <sub>5</sub> |
| H | V <sub>CC</sub>   | V <sub>CC</sub>   | V <sub>CC</sub>                | I/O <sub>49</sub>              | I/O <sub>48</sub>              | I/O <sub>36</sub>              | TCK                              | V <sub>CC</sub>                | I/O <sub>30</sub>              | I/O <sub>1</sub>               | I/O <sub>25</sub> <sub>9</sub> | I/O <sub>26</sub> <sub>0</sub> | V <sub>CC</sub>                | TDI                              | I/O <sub>21</sub> <sub>6</sub> | I/O <sub>21</sub> <sub>0</sub> | I/O <sub>21</sub> <sub>1</sub> | V <sub>CC</sub>                | V <sub>CC</sub>                | V <sub>CC</sub>                |
| J | I/O <sub>59</sub> | I/O <sub>58</sub> | I/O <sub>57</sub>              | I/O <sub>56</sub>              | I/O <sub>55</sub>              | I/O <sub>54</sub>              | V <sub>CC</sub>                  | I/O <sub>62</sub>              | I/O <sub>60</sub>              | I/O <sub>0</sub>               | I/O <sub>25</sub> <sub>8</sub> | I/O <sub>20</sub> <sub>2</sub> | I/O <sub>20</sub> <sub>3</sub> | CLK <sub>3</sub> /I <sub>4</sub> | I/O <sub>20</sub> <sub>4</sub> | I/O <sub>20</sub> <sub>5</sub> | I/O <sub>20</sub> <sub>6</sub> | I/O <sub>20</sub> <sub>7</sub> | I/O <sub>20</sub> <sub>8</sub> | I/O <sub>20</sub> <sub>9</sub> |
| K | GND               | GND               | GND                            | GND                            | I/O <sub>65</sub>              | I/O <sub>64</sub>              | CLK <sub>0</sub> /I <sub>0</sub> | I/O <sub>63</sub>              | I/O <sub>61</sub>              | GND                            | GND                            | I/O <sub>19</sub> <sub>8</sub> | I/O <sub>19</sub> <sub>9</sub> | CLK <sub>2</sub> /I <sub>3</sub> | I/O <sub>20</sub> <sub>0</sub> | I/O <sub>20</sub> <sub>1</sub> | GND                            | GND                            | GND                            | GND                            |
| L | GND               | GND               | GND                            | GND                            | I/O <sub>69</sub>              | I/O <sub>68</sub>              | NC                               | I/O <sub>67</sub>              | I/O <sub>66</sub>              | GND                            | GND                            | I/O <sub>19</sub> <sub>3</sub> | I/O <sub>19</sub> <sub>5</sub> | I <sub>2</sub>                   | I/O <sub>19</sub> <sub>6</sub> | I/O <sub>19</sub> <sub>7</sub> | GND                            | GND                            | GND                            | GND                            |
| M | I/O <sub>89</sub> | I/O <sub>88</sub> | I/O <sub>87</sub>              | I/O <sub>86</sub>              | I/O <sub>85</sub>              | I/O <sub>84</sub>              | CLK <sub>1</sub> /I <sub>1</sub> | I/O <sub>71</sub>              | I/O <sub>70</sub>              | I/O <sub>12</sub> <sub>6</sub> | I/O <sub>13</sub> <sub>2</sub> | I/O <sub>19</sub> <sub>2</sub> | I/O <sub>19</sub> <sub>4</sub> | V <sub>CC</sub>                  | I/O <sub>17</sub> <sub>4</sub> | I/O <sub>17</sub> <sub>5</sub> | I/O <sub>17</sub> <sub>6</sub> | I/O <sub>17</sub> <sub>7</sub> | I/O <sub>17</sub> <sub>8</sub> | I/O <sub>17</sub> <sub>9</sub> |
| N | V <sub>CC</sub>   | V <sub>CC</sub>   | V <sub>CC</sub>                | I/O <sub>91</sub>              | I/O <sub>90</sub>              | I/O <sub>72</sub>              | TMS                              | V <sub>CC</sub>                | I/O <sub>12</sub> <sub>8</sub> | I/O <sub>12</sub> <sub>7</sub> | I/O <sub>13</sub> <sub>3</sub> | I/O <sub>16</sub> <sub>2</sub> | V <sub>CC</sub>                | TDO                              | I/O <sub>18</sub> <sub>0</sub> | I/O <sub>16</sub> <sub>8</sub> | I/O <sub>16</sub> <sub>9</sub> | V <sub>CC</sub>                | V <sub>CC</sub>                | V <sub>CC</sub>                |
| P | I/O <sub>95</sub> | I/O <sub>94</sub> | I/O <sub>93</sub>              | I/O <sub>92</sub>              | I/O <sub>75</sub>              | I/O <sub>74</sub>              | I/O <sub>73</sub>                | I/O <sub>11</sub> <sub>4</sub> | V <sub>CC</sub>                | I/O <sub>12</sub> <sub>9</sub> | I/O <sub>13</sub> <sub>4</sub> | I/O <sub>13</sub> <sub>7</sub> | I/O <sub>16</sub> <sub>3</sub> | I/O <sub>18</sub> <sub>1</sub>   | I/O <sub>18</sub> <sub>2</sub> | I/O <sub>18</sub> <sub>3</sub> | I/O <sub>17</sub> <sub>0</sub> | I/O <sub>17</sub> <sub>1</sub> | I/O <sub>17</sub> <sub>2</sub> | I/O <sub>17</sub> <sub>3</sub> |
| R | I/O <sub>80</sub> | I/O <sub>79</sub> | I/O <sub>78</sub>              | I/O <sub>10</sub> <sub>8</sub> | I/O <sub>77</sub>              | I/O <sub>76</sub>              | I/O <sub>11</sub> <sub>5</sub>   | I/O <sub>11</sub> <sub>7</sub> | I/O <sub>12</sub> <sub>0</sub> | I/O <sub>13</sub> <sub>0</sub> | I/O <sub>13</sub> <sub>5</sub> | I/O <sub>13</sub> <sub>8</sub> | I/O <sub>16</sub> <sub>4</sub> | I/O <sub>16</sub> <sub>5</sub>   | NC                             | I/O <sub>18</sub> <sub>4</sub> | I/O <sub>18</sub> <sub>5</sub> | I/O <sub>18</sub> <sub>6</sub> | I/O <sub>18</sub> <sub>9</sub> | I/O <sub>19</sub> <sub>1</sub> |
| T | I/O <sub>82</sub> | I/O <sub>81</sub> | I/O <sub>11</sub> <sub>0</sub> | I/O <sub>10</sub> <sub>9</sub> | NC                             | I/O <sub>11</sub> <sub>6</sub> | I/O <sub>11</sub> <sub>8</sub>   | I/O <sub>10</sub> <sub>2</sub> | I/O <sub>12</sub> <sub>1</sub> | I/O <sub>13</sub> <sub>1</sub> | I/O <sub>13</sub> <sub>6</sub> | I/O <sub>13</sub> <sub>9</sub> | I/O <sub>15</sub> <sub>6</sub> | I/O <sub>16</sub> <sub>6</sub>   | I/O <sub>16</sub> <sub>7</sub> | NC                             | I/O <sub>15</sub> <sub>4</sub> | I/O <sub>15</sub> <sub>5</sub> | I/O <sub>18</sub> <sub>7</sub> | I/O <sub>19</sub> <sub>0</sub> |
| U | I/O <sub>83</sub> | NC                | GND                            | I/O <sub>11</sub> <sub>1</sub> | I/O <sub>11</sub> <sub>2</sub> | I/O <sub>11</sub> <sub>9</sub> | I/O <sub>10</sub> <sub>4</sub>   | I/O <sub>10</sub> <sub>3</sub> | I/O <sub>12</sub> <sub>2</sub> | GND                            | GND                            | I/O <sub>14</sub> <sub>0</sub> | I/O <sub>15</sub> <sub>7</sub> | I/O <sub>15</sub> <sub>8</sub>   | I/O <sub>15</sub> <sub>0</sub> | I/O <sub>15</sub> <sub>1</sub> | I/O <sub>15</sub> <sub>3</sub> | GND                            | NC                             | I/O <sub>18</sub> <sub>8</sub> |
| V | NC                | GND               | GND                            | GND                            | I/O <sub>11</sub> <sub>3</sub> | I/O <sub>96</sub>              | I/O <sub>10</sub> <sub>5</sub>   | V <sub>CC</sub>                | I/O <sub>12</sub> <sub>3</sub> | GND                            | GND                            | I/O <sub>14</sub> <sub>1</sub> | V <sub>CC</sub>                | I/O <sub>15</sub> <sub>9</sub>   | I/O <sub>1</sub> <sub>44</sub> | I/O <sub>15</sub> <sub>2</sub> | GND                            | GND                            | GND                            | NC                             |
| W | GND               | GND               | GND                            | NC                             | I/O <sub>97</sub>              | I/O <sub>99</sub>              | I/O <sub>10</sub> <sub>6</sub>   | V <sub>CC</sub>                | I/O <sub>12</sub> <sub>4</sub> | GND                            | GND                            | I/O <sub>14</sub> <sub>2</sub> | V <sub>CC</sub>                | I/O <sub>16</sub> <sub>0</sub>   | I/O <sub>14</sub> <sub>5</sub> | I/O <sub>14</sub> <sub>7</sub> | NC                             | GND                            | GND                            | GND                            |
| Y | GND               | GND               | NC                             | I/O <sub>98</sub>              | I/O <sub>10</sub> <sub>0</sub> | I/O <sub>10</sub> <sub>1</sub> | I/O <sub>10</sub> <sub>7</sub>   | V <sub>CC</sub>                | I/O <sub>12</sub> <sub>5</sub> | GND                            | GND                            | I/O <sub>14</sub> <sub>3</sub> | V <sub>CC</sub>                | I/O <sub>16</sub> <sub>1</sub>   | I/O <sub>14</sub> <sub>6</sub> | I/O <sub>14</sub> <sub>8</sub> | I/O <sub>14</sub> <sub>9</sub> | NC                             | GND                            | GND                            |

## Ordering Information



## 5.0V Ordering Information

| Macro-cells | Speed (MHz) | Ordering Code     | Package Name | Package Type                        | Operating Range |
|-------------|-------------|-------------------|--------------|-------------------------------------|-----------------|
| 32          | 200         | CY37032P44-200AC  | A44          | 44-Lead Thin Quad Flat Pack         | Commercial      |
|             |             | CY37032P44-200JC  | J67          | 44-Lead Plastic Leaded Chip Carrier |                 |
|             | 154         | CY37032P44-154AC  | A44          | 44-Lead Thin Quad Flat Pack         | Commercial      |
|             |             | CY37032P44-154JC  | J67          | 44-Lead Plastic Leaded Chip Carrier |                 |
|             |             | CY37032P44-154AI  | A44          | 44-Lead Thin Quad Flat Pack         | Industrial      |
|             |             | CY37032P44-154JI  | J67          | 44-Lead Plastic Leaded Chip Carrier |                 |
|             | 125         | CY37032P44-125AC  | A44          | 44-Lead Thin Quad Flat Pack         | Commercial      |
|             |             | CY37032P44-125JC  | J67          | 44-Lead Plastic Leaded Chip Carrier |                 |
|             |             | CY37032P44-125AI  | A44          | 44-Lead Thin Quad Flat Pack         | Industrial      |
|             |             | CY37032P44-125JI  | J67          | 44-Lead Plastic Leaded Chip Carrier |                 |
| 64          | 200         | CY37064P44-200AC  | A44          | 44-Lead Thin Quad Flat Pack         | Commercial      |
|             |             | CY37064P44-200JC  | J67          | 44-Lead Plastic Leaded Chip Carrier |                 |
|             |             | CY37064P84-200JC  | J83          | 84-Lead Plastic Leaded Chip Carrier |                 |
|             |             | CY37064P100-200AC | A100         | 100-Lead Thin Quad Flat Pack        |                 |



## 5.0V Ordering Information (continued)

| Macro-cells | Speed (MHz) | Ordering Code     | Package Name | Package Type                          | Operating Range |
|-------------|-------------|-------------------|--------------|---------------------------------------|-----------------|
| 64          | 154         | CY37064P44-154AC  | A44          | 44-Lead Thin Quad Flat Pack           | Commercial      |
|             |             | CY37064P44-154JC  | J67          | 44-Lead Plastic Leaded Chip Carrier   |                 |
|             |             | CY37064P84-154JC  | J83          | 84-Lead Plastic Leaded Chip Carrier   |                 |
|             |             | CY37064P100-154AC | A100         | 100-Lead Thin Quad Flat Pack          |                 |
|             |             | CY37064P44-154AI  | A44          | 44-Lead Thin Quad Flat Pack           | Industrial      |
|             |             | CY37064P44-154JI  | J67          | 44-Lead Plastic Leaded Chip Carrier   |                 |
|             |             | CY37064P84-154JI  | J83          | 84-Lead Plastic Leaded Chip Carrier   |                 |
|             |             | CY37064P100-154AI | A100         | 100-Lead Thin Quad Flat Pack          |                 |
|             |             | 5962-9951902QYA   | Y67          | 44-Lead Ceramic Leadless Chip Carrier | Military        |
|             | 125         | CY37064P44-125AC  | A44          | 44-Lead Thin Quad Flat Pack           | Commercial      |
|             |             | CY37064P44-125JC  | J67          | 44-Lead Plastic Leaded Chip Carrier   |                 |
|             |             | CY37064P84-125JC  | J83          | 84-Lead Plastic Leaded Chip Carrier   |                 |
|             |             | CY37064P100-125AC | A100         | 100-Lead Thin Quad Flat Pack          |                 |
|             |             | CY37064P44-125AI  | A44          | 44-Lead Thin Quad Flat Pack           | Industrial      |
|             |             | CY37064P44-125JI  | J67          | 44-Lead Plastic Leaded Chip Carrier   |                 |
|             |             | CY37064P84-125JI  | J83          | 84-Lead Plastic Leaded Chip Carrier   |                 |
|             |             | CY37064P100-125AI | A100         | 100-Lead Thin Quad Flat Pack          |                 |
|             |             | 5962-9951901QYA   | Y67          | 44-Lead Ceramic Leadless Chip Carrier | Military        |
| 128         | 167         | CY37128P84-167JC  | J83          | 84-Lead Plastic Leaded Chip Carrier   | Commercial      |
|             |             | CY37128P100-167AC | A100         | 100-Lead Thin Quad Flat Pack          |                 |
|             |             | CY37128P160-167AC | A160         | 160-Lead Thin Quad Flat Pack          |                 |
|             | 125         | CY37128P84-125JC  | J83          | 84-Lead Plastic Leaded Chip Carrier   | Commercial      |
|             |             | CY37128P100-125AC | A100         | 100-Lead Thin Quad Flat Pack          |                 |
|             |             | CY37128P160-125AC | A160         | 160-Lead Thin Quad Flat Pack          |                 |
|             |             | CY37128P84-125JI  | J83          | 84-Lead Plastic Leaded Chip Carrier   | Industrial      |
|             |             | CY37128P100-125AI | A100         | 100-Lead Thin Quad Flat Pack          |                 |
|             |             | CY37128P160-125AI | A160         | 160-Lead Thin Quad Flat Pack          |                 |
|             |             | 5962-9952102QYA   | Y84          | 84-Lead Ceramic Leaded Chip Carrier   | Military        |
|             | 100         | CY37128P84-100JC  | J83          | 84-Lead Plastic Leaded Chip Carrier   | Commercial      |
|             |             | CY37128P100-100AC | A100         | 100-Lead Thin Quad Flat Pack          |                 |
|             |             | CY37128P160-100AC | A160         | 160-Lead Thin Quad Flat Pack          |                 |
|             |             | CY37128P84-100JI  | J83          | 84-Lead Plastic Leaded Chip Carrier   | Industrial      |
|             |             | CY37128P100-100AI | A100         | 100-Lead Thin Quad Flat Pack          |                 |
|             |             | CY37128P160-100AI | A160         | 160-Lead Thin Quad Flat Pack          |                 |
|             |             | 5962-9952101QYA   | Y84          | 84-Lead Ceramic Leaded Chip Carrier   | Military        |
| 192         | 154         | CY37192P160-154AC | A160         | 160-Lead Thin Quad Flat Pack          | Commercial      |
|             | 125         | CY37192P160-125AC | A160         | 160-Lead Thin Quad Flat Pack          | Commercial      |
|             |             | CY37192P160-125AI | A160         | 160-Lead Thin Quad Flat Pack          | Industrial      |
|             | 83          | CY37192P160-83AC  | A160         | 160-Lead Thin Quad Flat Pack          | Commercial      |
|             |             | CY37192P160-83AI  | A160         | 160-Lead Thin Quad Flat Pack          | Industrial      |



## 5.0V Ordering Information (continued)

| Macro-cells | Speed (MHz) | Ordering Code      | Package Name | Package Type                    | Operating Range |
|-------------|-------------|--------------------|--------------|---------------------------------|-----------------|
| 256         | 154         | CY37256P160-154AC  | A160         | 160-Lead Thin Quad Flat Pack    | Commercial      |
|             |             | CY37256P208-154NC  | N208         | 208-Lead Plastic Quad Flat Pack |                 |
|             |             | CY37256P256-154BGC | BG256        | 256-Lead Ball Grid Array        |                 |
|             | 125         | CY37256P160-125AC  | A160         | 160-Lead Thin Quad Flat Pack    | Commercial      |
|             |             | CY37256P208-125NC  | N208         | 208-Lead Plastic Quad Flat Pack |                 |
|             |             | CY37256P256-125BGC | BG256        | 256-Lead Ball Grid Array        |                 |
|             |             | CY37256P160-125AI  | A160         | 160-Lead Thin Quad Flat Pack    | Industrial      |
|             |             | CY37256P208-125NI  | N208         | 208-Lead Plastic Quad Flat Pack |                 |
|             |             | CY37256P256-125BGI | BG256        | 256-Lead Ball Grid Array        |                 |
|             |             | 5962-9952302QZC    | U162         | 160-Lead Ceramic Quad Flat Pack | Military        |
|             | 83          | CY37256P160-83AC   | A160         | 160-Lead Thin Quad Flat Pack    | Commercial      |
|             |             | CY37256P208-83NC   | N208         | 208-Lead Plastic Quad Flat Pack |                 |
|             |             | CY37256P256-83BGC  | BG256        | 256-Lead Ball Grid Array        |                 |
|             |             | CY37256P160-83AI   | A160         | 160-Lead Thin Quad Flat Pack    | Industrial      |
|             |             | CY37256P208-83NI   | N208         | 208-Lead Plastic Quad Flat Pack |                 |
|             |             | CY37256P256-83BGI  | BG256        | 256-Lead Ball Grid Array        |                 |
|             |             | 5962-9952301QZC    | U162         | 160-Lead Ceramic Quad Flat Pack | Military        |
| 384         | 125         | CY37384P208-125NC  | N208         | 208-Lead Plastic Quad Flat Pack | Commercial      |
|             |             | CY37384P256-125BGC | BG256        | 256-Lead Ball Grid Array        |                 |
|             | 83          | CY37384P208-83NC   | N208         | 208-Lead Plastic Quad Flat Pack | Commercial      |
|             |             | CY37384P256-83BGC  | BG256        | 256-Lead Ball Grid Array        |                 |
|             |             | CY37384P208-83NI   | N208         | 208-Lead Plastic Quad Flat Pack | Industrial      |
|             |             | CY37384P256-83BGI  | BG256        | 256-Lead Ball Grid Array        |                 |
| 512         | 125         | CY37512P208-125NC  | N208         | 208-Lead Plastic Quad Flat Pack | Commercial      |
|             |             | CY37512P256-125BGC | BG256        | 256-Lead Ball Grid Array        |                 |
|             |             | CY37512P352-125BGC | BG352        | 352-Lead Ball Grid Array        |                 |
|             | 100         | CY37512P208-100NC  | N208         | 208-Lead Plastic Quad Flat Pack | Commercial      |
|             |             | CY37512P256-100BGC | BG256        | 256-Lead Ball Grid Array        |                 |
|             |             | CY37512P352-100BGC | BG352        | 352-Lead Ball Grid Array        |                 |
|             |             | CY37512P208-100NI  | N208         | 208-Lead Plastic Quad Flat Pack | Industrial      |
|             |             | CY37512P256-100BGI | BG256        | 256-Lead Ball Grid Array        |                 |
|             |             | CY37512P352-100BGI | BG352        | 352-Lead Ball Grid Array        |                 |
|             |             | 5962-9952502QZC    | U208         | 208-Lead Ceramic Quad Flat Pack | Military        |
|             | 83          | CY37512P208-83NC   | N208         | 208-Lead Plastic Quad Flat Pack | Commercial      |
|             |             | CY37512P256-83BGC  | BG256        | 256-Lead Ball Grid Array        |                 |
|             |             | CY37512P352-83BGC  | BG352        | 352-Lead Ball Grid Array        |                 |
|             |             | CY37512P208-83NI   | N208         | 208-Lead Plastic Quad Flat Pack | Industrial      |
|             |             | CY37512P256-83BGI  | BG256        | 256-Lead Ball Grid Array        |                 |
|             |             | CY37512P352-83BGI  | BG352        | 352-Lead Ball Grid Array        |                 |
|             |             | 5962-9952501QZC    | U208         | 208-Lead Ceramic Quad Flat Pack | Military        |

**3.3V Ordering Information**

| Macro-cells | Speed (MHz) | Ordering Code       | Package Name | Package Type                        | Operating Range |
|-------------|-------------|---------------------|--------------|-------------------------------------|-----------------|
| 32          | 143         | CY37032VP44-143AC   | A44          | 44-Lead Thin Quad Flat Pack         | Commercial      |
|             |             | CY37032VP48-143BAC  | BA50         | 48-Lead Fine Pitch Ball Grid Array  |                 |
|             | 100         | CY37032VP44-100AC   | A44          | 44-Lead Thin Quad Flat Pack         | Commercial      |
|             |             | CY37032VP48-100BAC  | BA50         | 48-Lead Fine Pitch Ball Grid Array  |                 |
|             |             | CY37032VP44-100AI   | A44          | 44-Lead Thin Quad Flat Pack         | Industrial      |
|             |             | CY37032VP48-100BAI  | BA50         | 48-Lead Fine Pitch Ball Grid Array  |                 |
| 64          | 143         | CY37064VP44-143AC   | A44          | 44-Lead Thin Quad Flatpack          | Commercial      |
|             |             | CY37064VP48-143BAC  | BA50         | 48-Lead Fine-Pitch Ball Grid Array  |                 |
|             |             | CY37064VP100-143AC  | A100         | 100-Lead Thin Quad Flatpack         |                 |
|             |             | CY37064VP100-143BBC | BB100        | 100-Lead Fine-Pitch Ball Grid Array |                 |
|             | 100         | CY37064VP44-100AC   | A44          | 44-Lead Thin Quad Flatpack          | Commercial      |
|             |             | CY37064VP48-100BAC  | BA50         | 48-Lead Fine-Pitch Ball Grid Array  |                 |
|             |             | CY37064VP100-100AC  | A100         | 100-Lead Thin Quad Flatpack         |                 |
|             |             | CY37064VP100-100BBC | BB100        | 100-Lead Fine-Pitch Ball Grid Array |                 |
|             |             | CY37064VP44-100AI   | A44          | 44-Lead Thin Quad Flatpack          | Industrial      |
|             |             | CY37064VP48-100BAI  | BA50         | 48-Lead Fine-Pitch Ball Grid Array  |                 |
|             |             | CY37064VP100-100BBI | BB100        | 100-Lead Fine-Pitch Ball Grid Array |                 |
|             |             | CY37064VP100-100AI  | A100         | 100-Lead Thin Quad Flatpack         |                 |
|             |             | 5962-9952001QYA     | Y67          | 44-Lead Ceramic Leaded Chip Carrier | Military        |
| 128         | 125         | CY37128VP100-125AC  | A100         | 100-Lead Thin Quad Flat Pack        | Commercial      |
|             |             | CY37128VP100-125BBC | BB100        | 100-Lead Fine-Pitch Ball Grid Array |                 |
|             |             | CY37128VP160-125AC  | A160         | 160-Lead Thin Quad Flat Pack        |                 |
|             | 83          | CY37128VP100-83AC   | A100         | 100-Lead Thin Quad Flat Pack        | Commercial      |
|             |             | CY37128VP100-83BBC  | BB100        | 100-Lead Fine-Pitch Ball Grid Array |                 |
|             |             | CY37128VP160-83AC   | A160         | 160-Lead Thin Quad Flat Pack        |                 |
|             |             | CY37128VP100-83AI   | A100         | 100-Lead Thin Quad Flat Pack        | Industrial      |
|             |             | CY37128VP100-83BBI  | BB100        | 100-Lead Fine-Pitch Ball Grid Array |                 |
|             |             | CY37128VP160-83AI   | A160         | 160-Lead Thin Quad Flat Pack        |                 |
|             |             | 5962-9952201QYA     | Y84          | 84-Lead Ceramic Leaded Chip Carrier | Military        |
| 192         | 100         | CY37192VP160-100AC  | A160         | 160-Lead Thin Quad Flat Pack        | Commercial      |
|             | 66          | CY37192VP160-66AC   | A160         | 160-Lead Thin Quad Flat Pack        | Commercial      |
|             |             | CY37192VP160-66AI   | A160         | 160-Lead Thin Quad Flat Pack        | Industrial      |

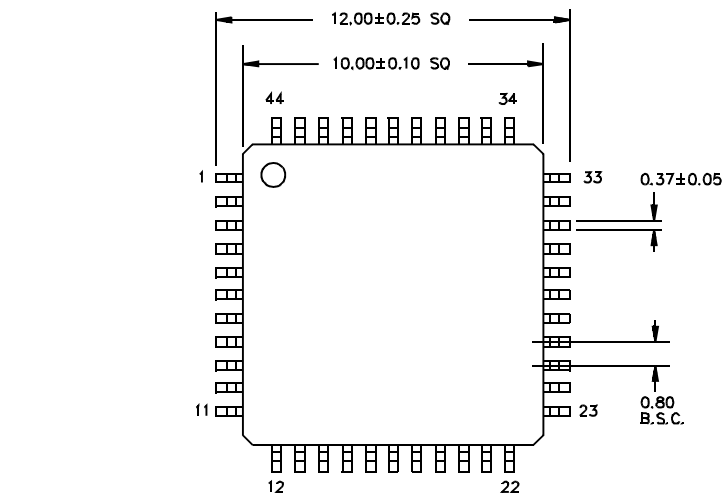


## 3.3V Ordering Information (continued)

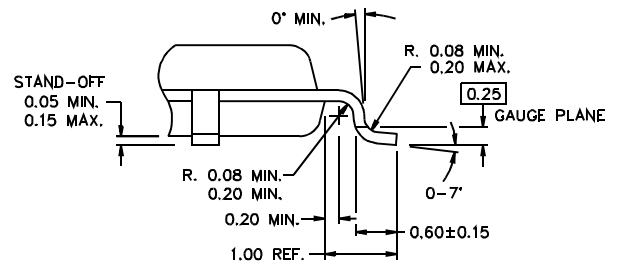
| Macro-cells | Speed (MHz) | Ordering Code       | Package Name | Package Type                        | Operating Range |
|-------------|-------------|---------------------|--------------|-------------------------------------|-----------------|
| 256         | 100         | CY37256VP160-100AC  | A160         | 160-Lead Thin Quad Flat Pack        | Commercial      |
|             |             | CY37256VP208-100NC  | N208         | 208-Lead Plastic Quad Flat Pack     |                 |
|             |             | CY37256VP256-100BGC | BG256        | 256-Lead Ball Grid Array            |                 |
|             |             | CY37256VP256-100BBC | BB256        | 256-Lead Fine-Pitch Ball Grid Array |                 |
|             | 66          | CY37256VP160-66AC   | A160         | 160-Lead Thin Quad Flat Pack        | Commercial      |
|             |             | CY37256VP208-66NC   | N208         | 208-Lead Plastic Quad Flat Pack     |                 |
|             |             | CY37256VP256-66BGC  | BG256        | 256-Lead Ball Grid Array            |                 |
|             |             | CY37256VP256-66BBC  | BB256        | 256-Lead Fine-Pitch Ball Grid Array |                 |
|             |             | CY37256VP160-66AI   | A160         | 160-Lead Thin Quad Flat Pack        | Industrial      |
|             |             | CY37256VP256-66BGI  | BG256        | 256-Lead Ball Grid Array            |                 |
|             |             | CY37256VP256-66BBI  | BB256        | 256-Lead Fine-Pitch Ball Grid Array |                 |
|             |             | 5962-9952401QZC     | U162         | 160-Lead Ceramic Quad Flat Pack     | Military        |
| 384         | 83          | CY37384VP208-83NC   | N208         | 208-Lead Plastic Quad Flat Pack     | Commercial      |
|             |             | CY37384VP256-83BGC  | BG256        | 256-Lead Ball Grid Array            |                 |
|             | 66          | CY37384VP208-66NC   | N208         | 208-Lead Plastic Quad Flat Pack     | Commercial      |
|             |             | CY37384VP256-66BGC  | BG256        | 256-Lead Ball Grid Array            |                 |
|             |             | CY37384VP208-66NI   | N208         | 208-Lead Plastic Quad Flat Pack     | Industrial      |
|             |             | CY37384VP256-66BGI  | BG256        | 256-Lead Ball Grid Array            |                 |
| 512         | 83          | CY37512VP208-83NC   | N208         | 208-Lead Plastic Quad Flat Pack     | Commercial      |
|             |             | CY37512VP256-83BGC  | BG256        | 256-Lead Ball Grid Array            |                 |
|             |             | CY37512VP352-83BGC  | BG352        | 352-Lead Ball Grid Array            |                 |
|             |             | CY37512VP400-83BBC  | BB400        | 400-Lead Fine-Pitch Ball Grid Array |                 |
|             | 66          | CY37512VP208-66NC   | N208         | 208-Lead Plastic Quad Flat Pack     | Commercial      |
|             |             | CY37512VP256-66BGC  | BG256        | 256-Lead Ball Grid Array            |                 |
|             |             | CY37512VP352-66BGC  | BG352        | 352-Lead Ball Grid Array            |                 |
|             |             | CY37512VP400-66BBC  | BB400        | 400-Lead Fine-Pitch Ball Grid Array |                 |
|             |             | CY37512VP208-66NI   | N208         | 208-Lead Plastic Quad Flat Pack     | Industrial      |
|             |             | CY37512VP256-66BGI  | BG256        | 256-Lead Ball Grid Array            |                 |
|             |             | CY37512VP352-66BGI  | BG352        | 352-Lead Ball Grid Array            |                 |
|             |             | CY37512VP400-66BBI  | BB400        | 400-Lead Fine-Pitch Ball Grid Array |                 |
|             |             | 5962-9952601QZC     | U208         | 208-Lead Ceramic Quad Flat Pack     | Military        |

## Package Diagrams

### 44-lead Thin Plastic Quad Flat Pack A44

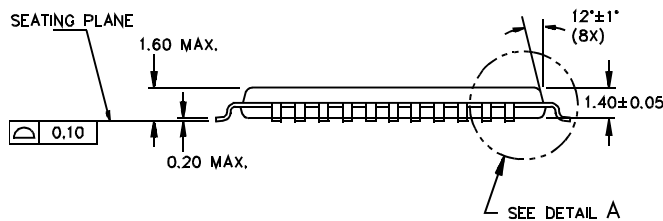


DIMENSIONS ARE IN MILLIMETERS



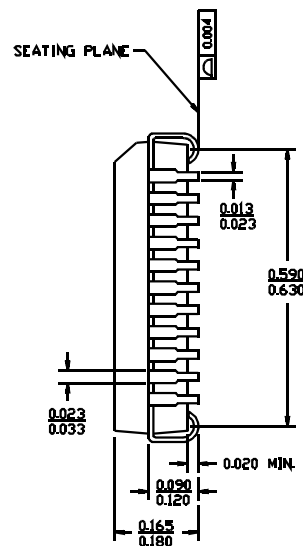
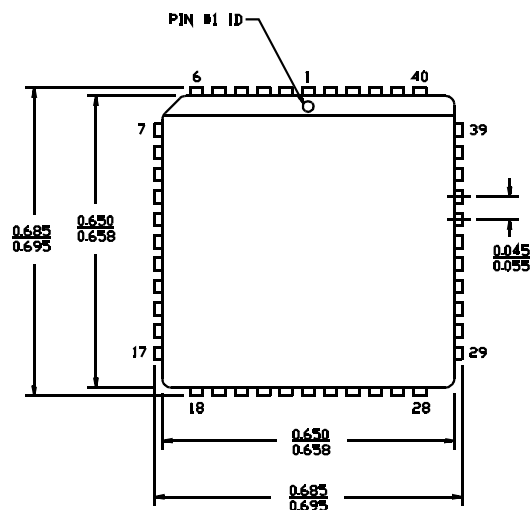
DETAIL A

51-85064-\*B



### 44-Lead Plastic Leaded Chip Carrier J67

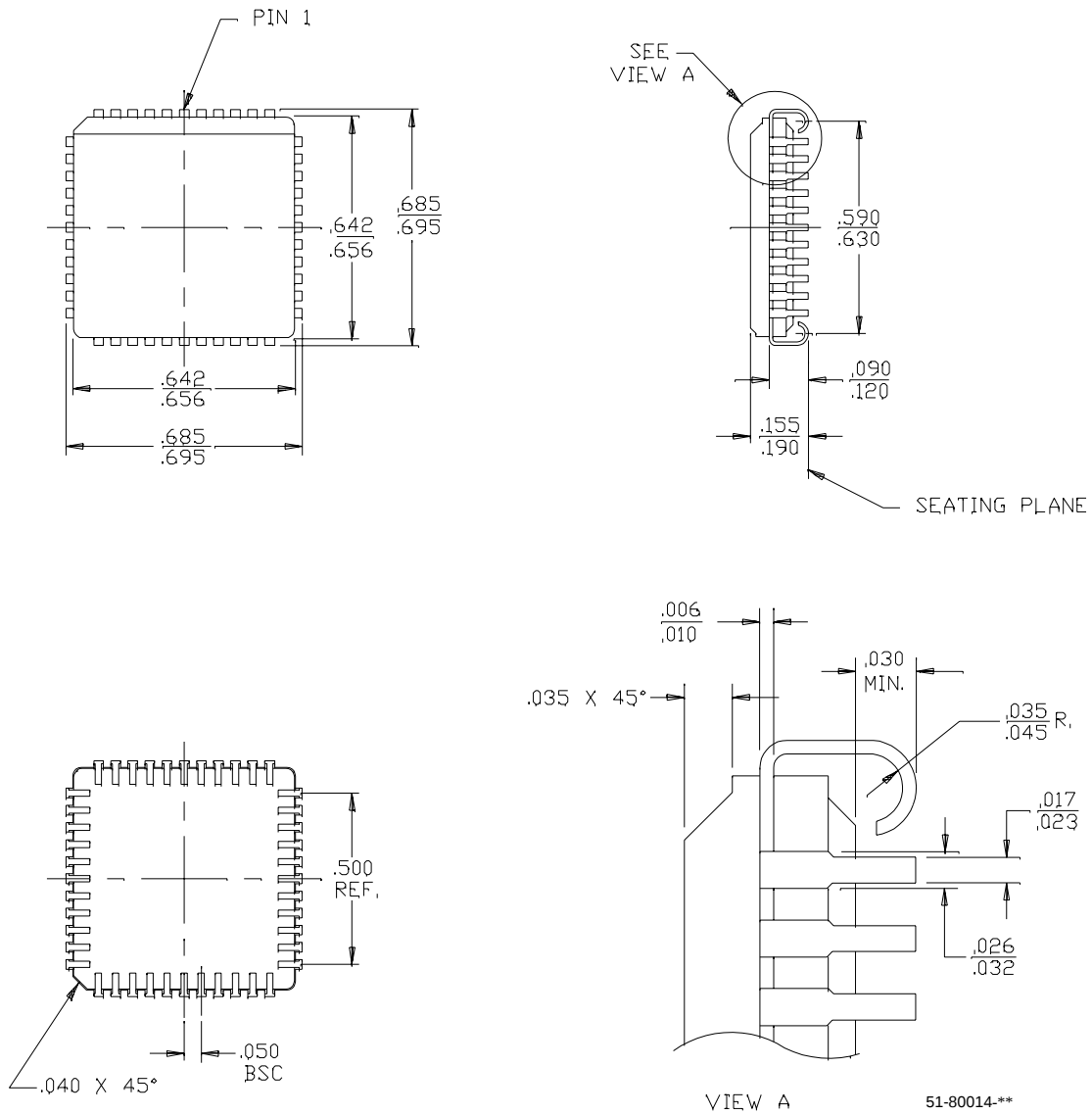
DIMENSIONS IN INCHES MIN. MAX.



51-85003-\*A

## Package Diagrams (continued)

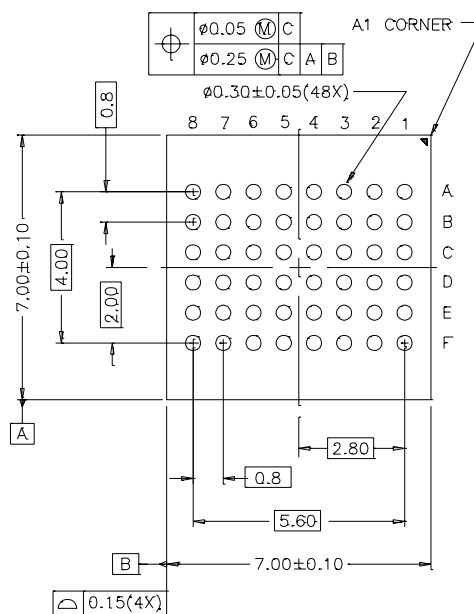
### 44-Pin Ceramic Leaded Chip Carrier Y67





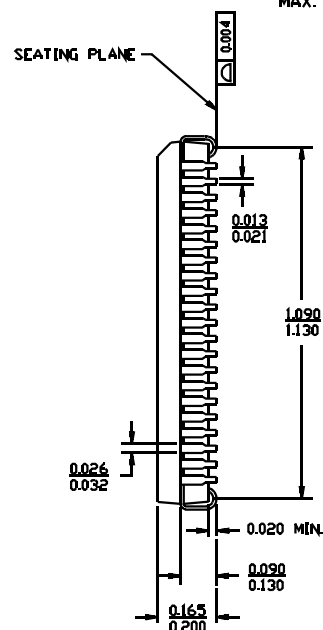
**48-Ball (7.0 mm x 7.0 mm x 1.2 mm, 0.80 pitch) Thin BGA BA48D**

BOTTOM VIEW



51-85109-\*C

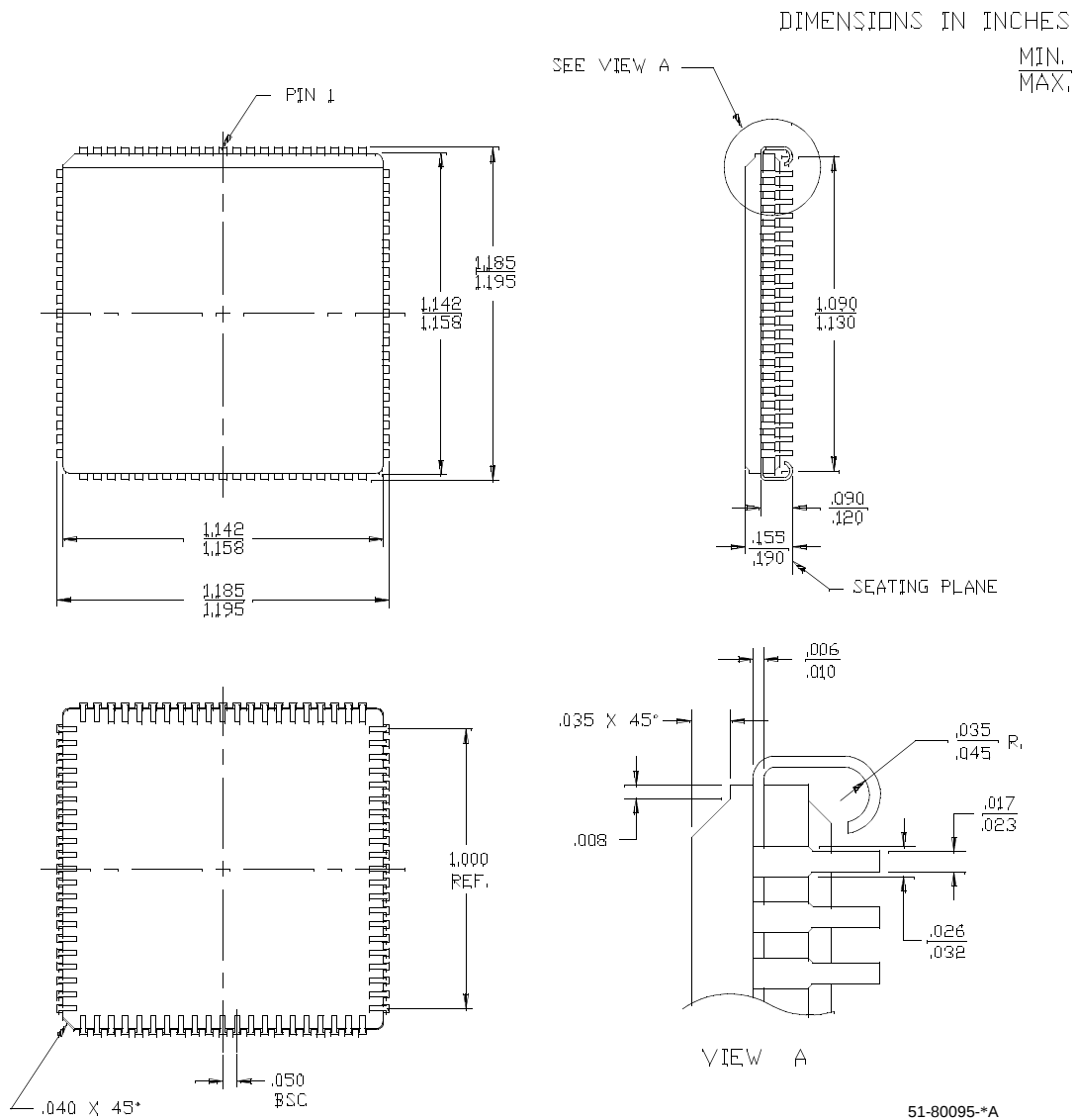
| DIMENSIONS IN INCHES |  | MIN. | MAX. |
|----------------------|--|------|------|
|----------------------|--|------|------|



51-85006-\*A

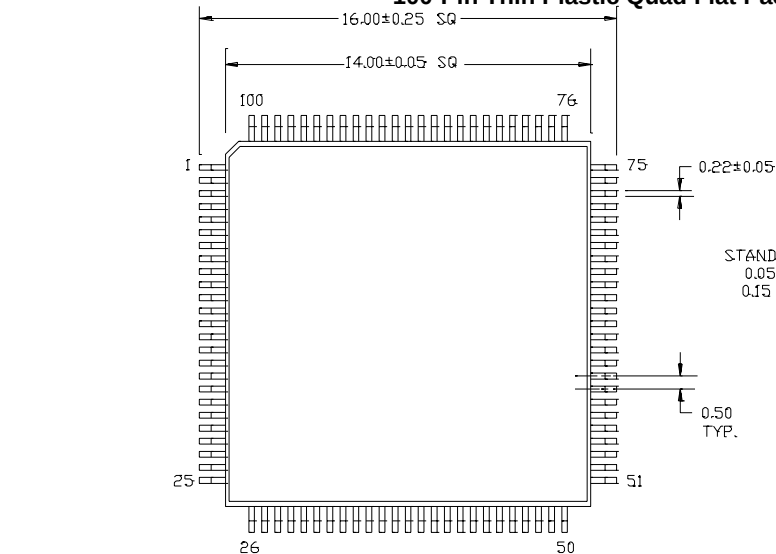
## Package Diagrams (continued)

### 84-Pin Ceramic Leaded Chip Carrier Y84

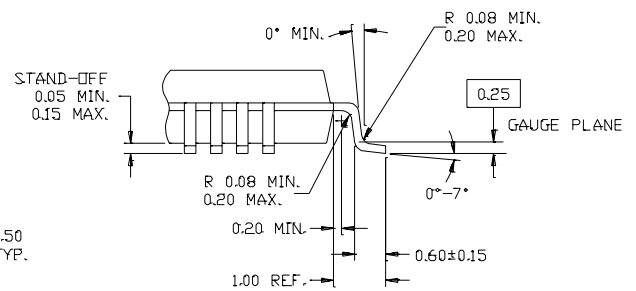


## Package Diagrams (continued)

**100-Pin Thin Plastic Quad Flat Pack (TQFP) A100**

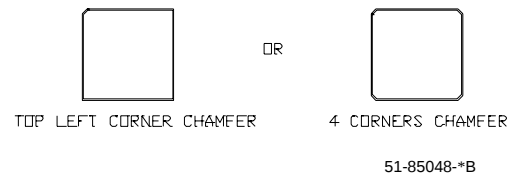
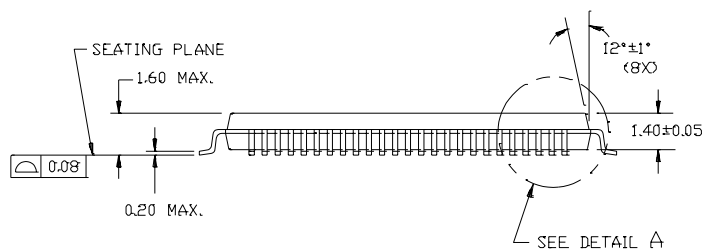


DIMENSIONS ARE IN MILLIMETERS.



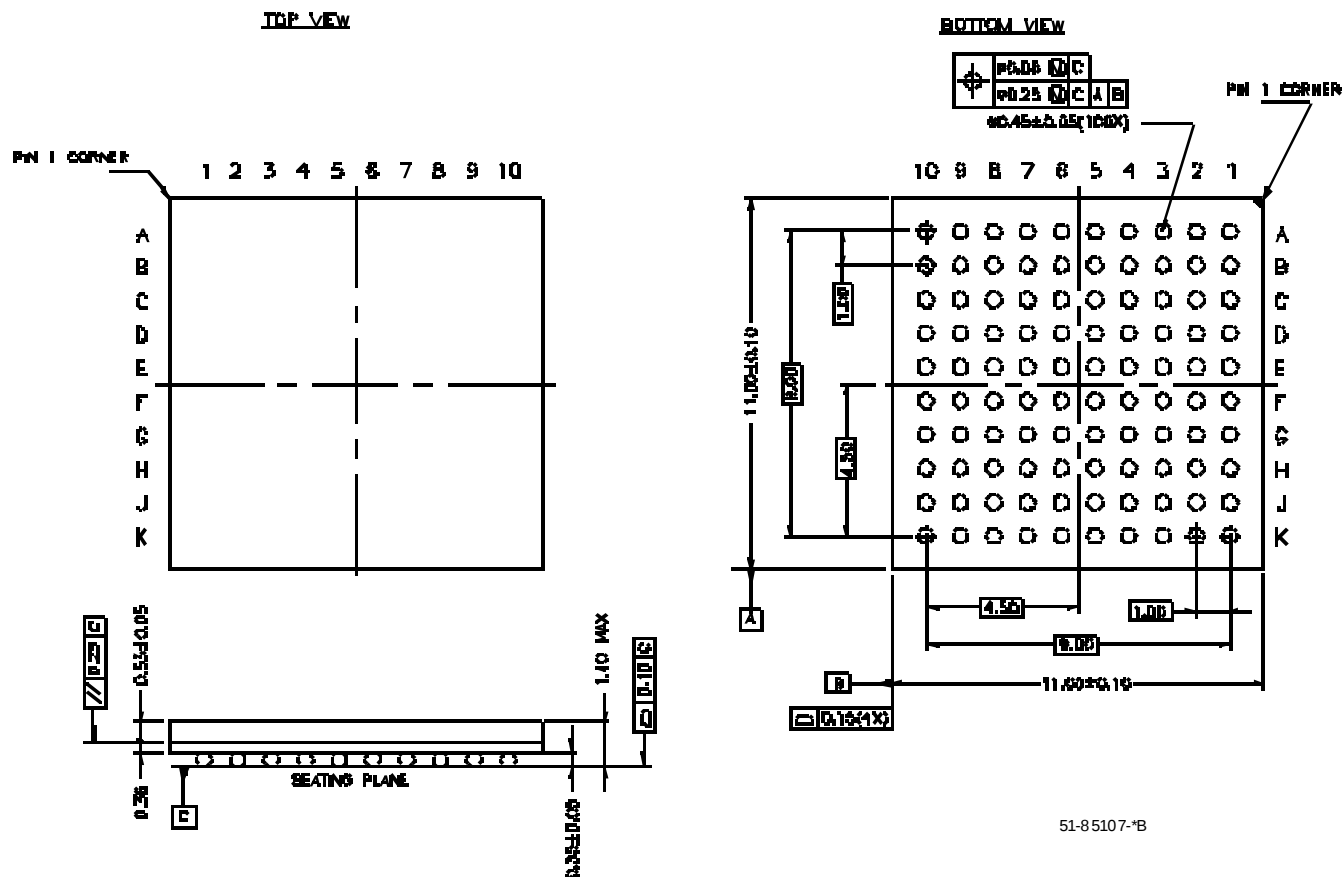
DETAIL A

NOTE: PKG. CAN HAVE



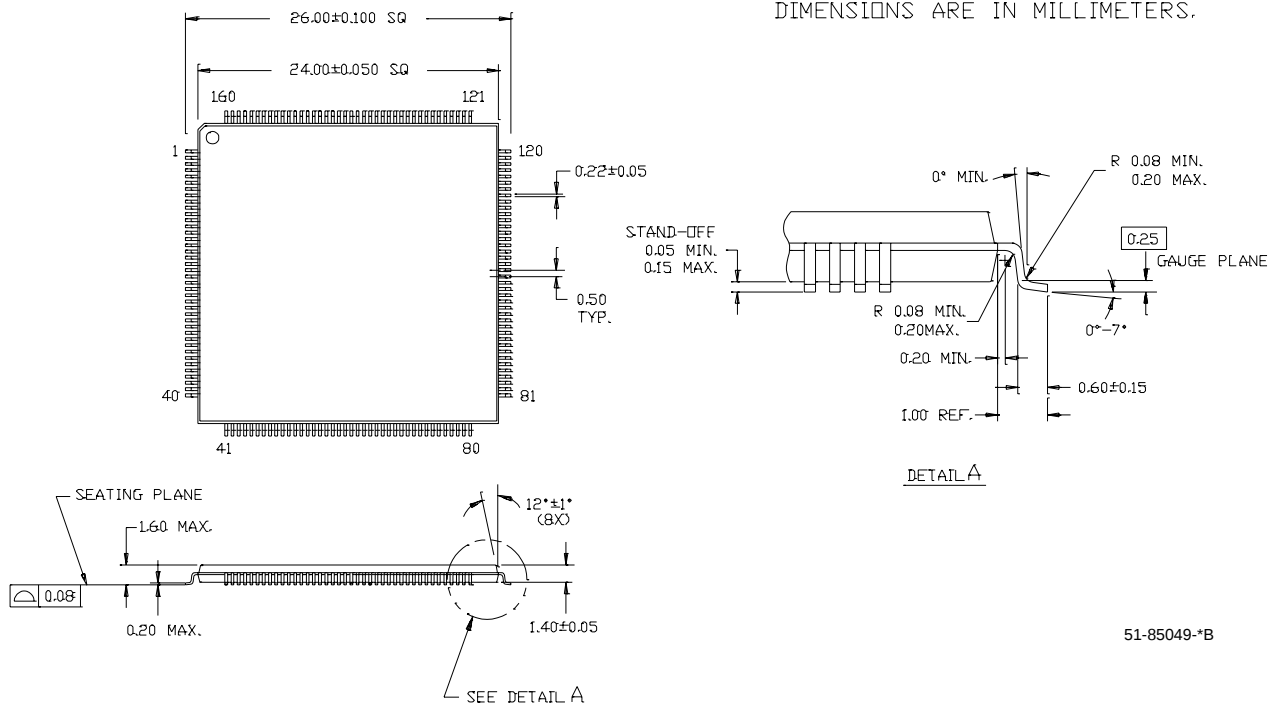
Package Diagrams (continued)

100-Ball Thin Ball Grid Array (11 x 11 x 1.4 mm) BB100



## Package Diagrams (continued)

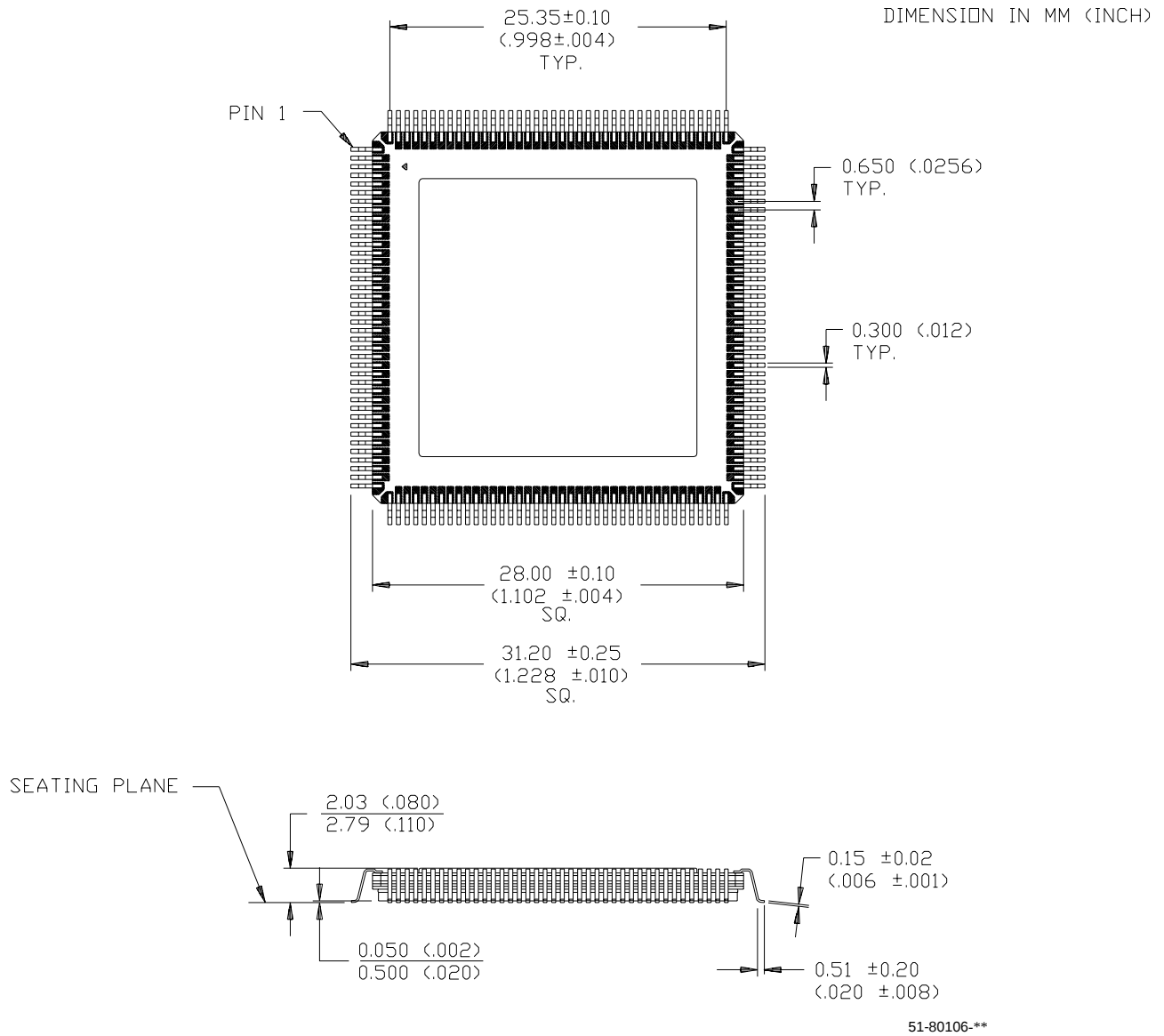
### 160-Pin Thin Plastic Quad Flat Pack (24 x 24 x 1.4 mm) (TQFP) A160



51-85049-\*B

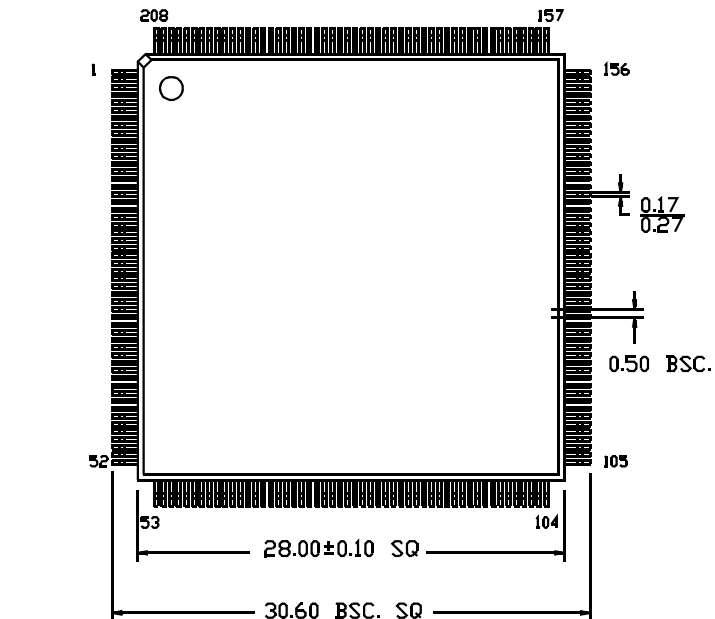
## Package Diagrams (continued)

### 160-Lead Ceramic Quad Flatpack (Cavity Up) U162

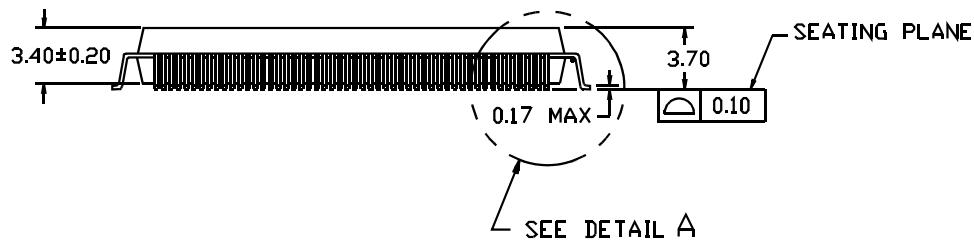
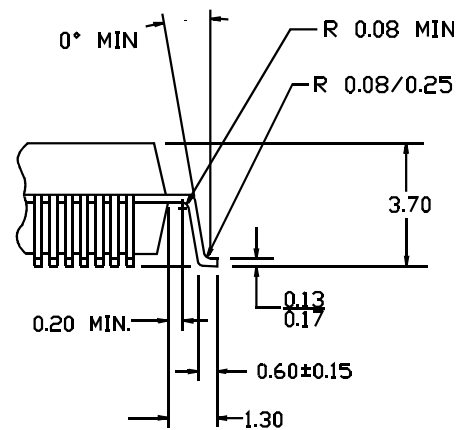


Package Diagrams (continued)

208-Lead Plastic Quad Flatpack N208



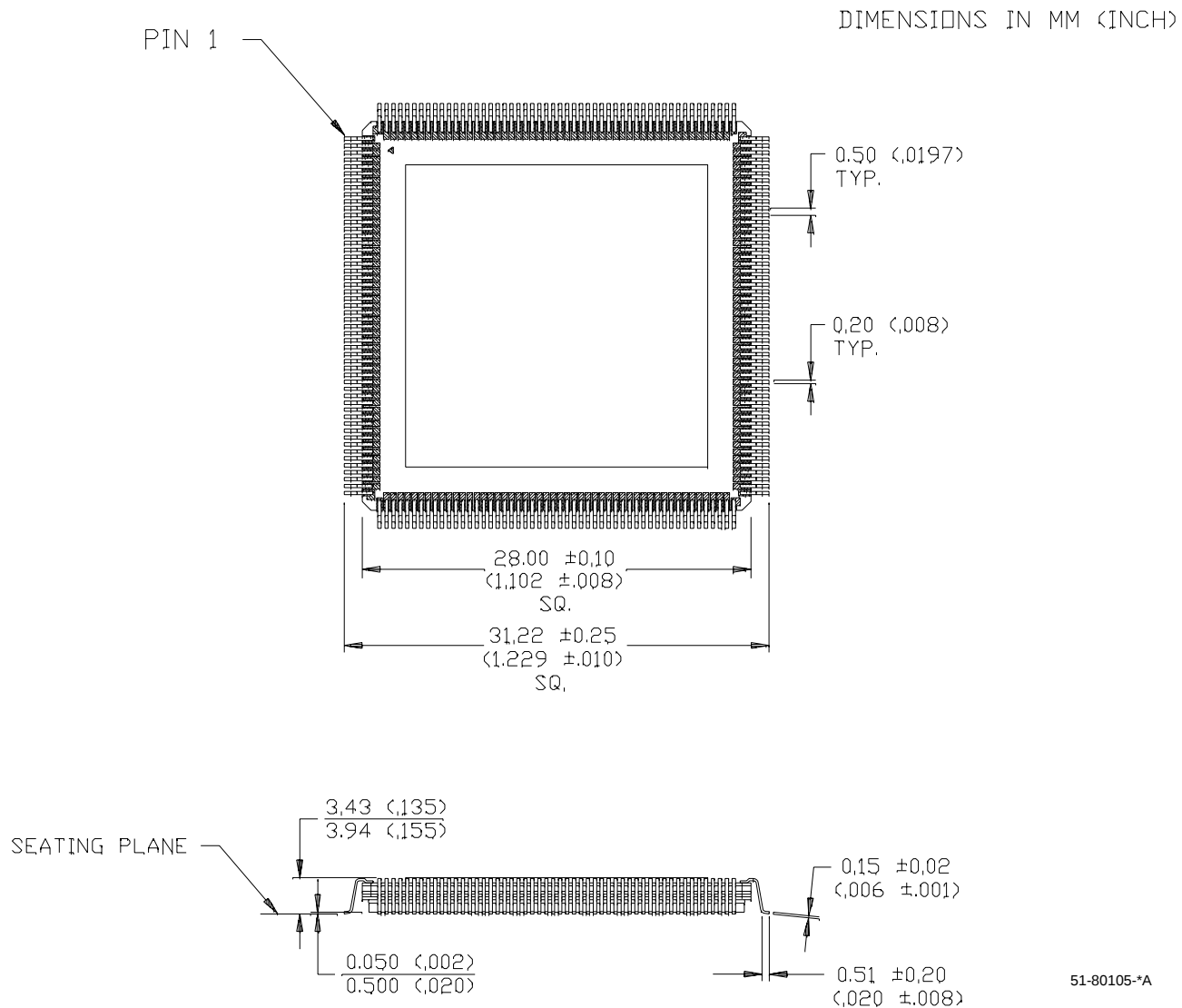
DIMENSIONS ARE IN MILLIMETERS

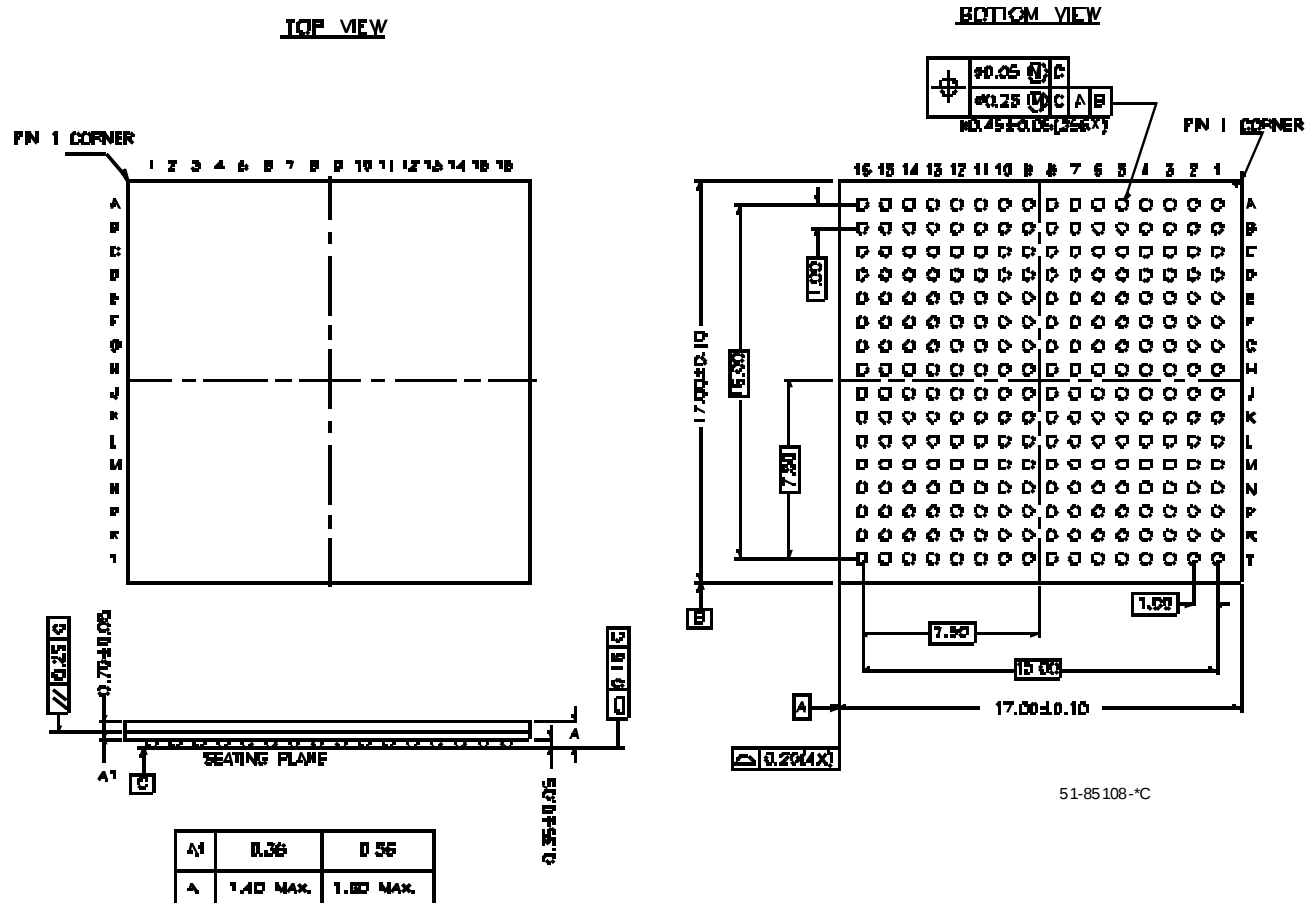


51-85069-\*B

## Package Diagrams (continued)

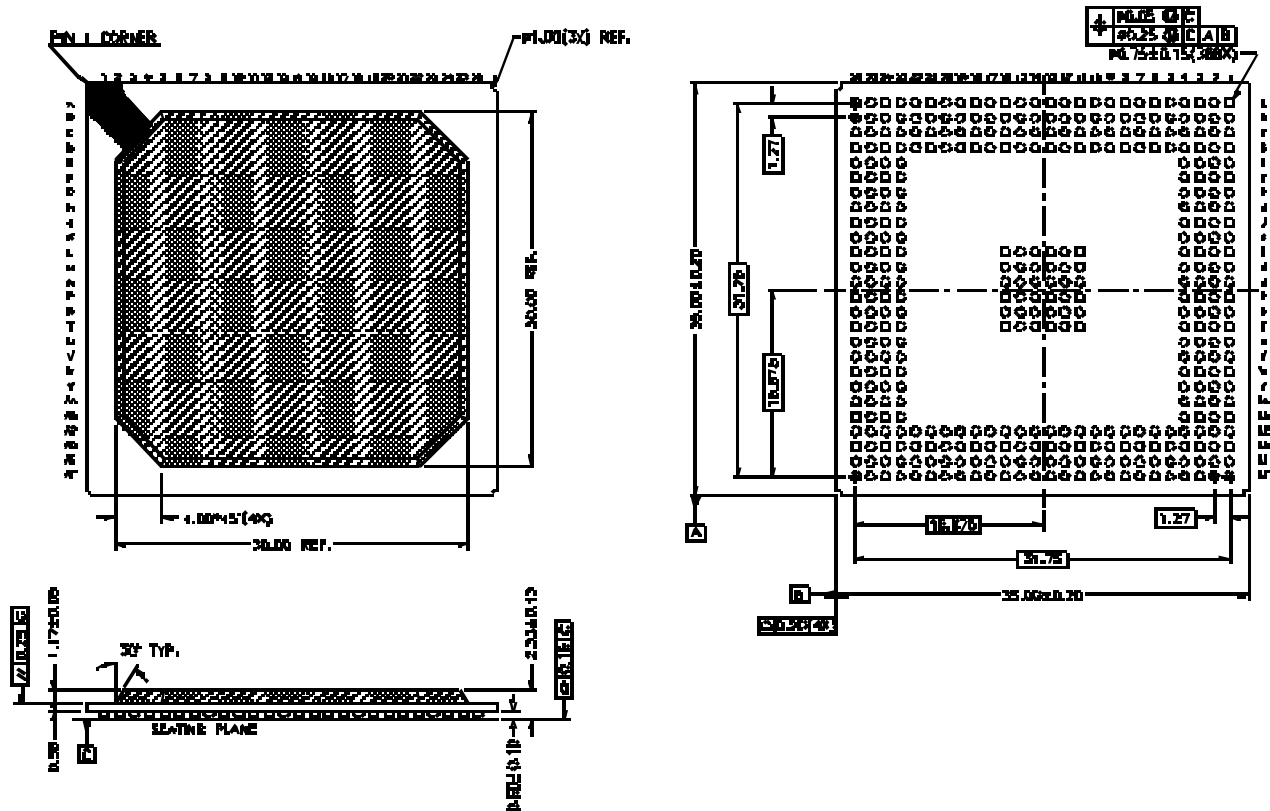
### 208-Lead Ceramic Quad Flatpack (Cavity Up) U208



**Package Diagrams (continued)**
**256-Ball FBGA (17 x 17 mm) BB256**


## Package Diagrams (continued)

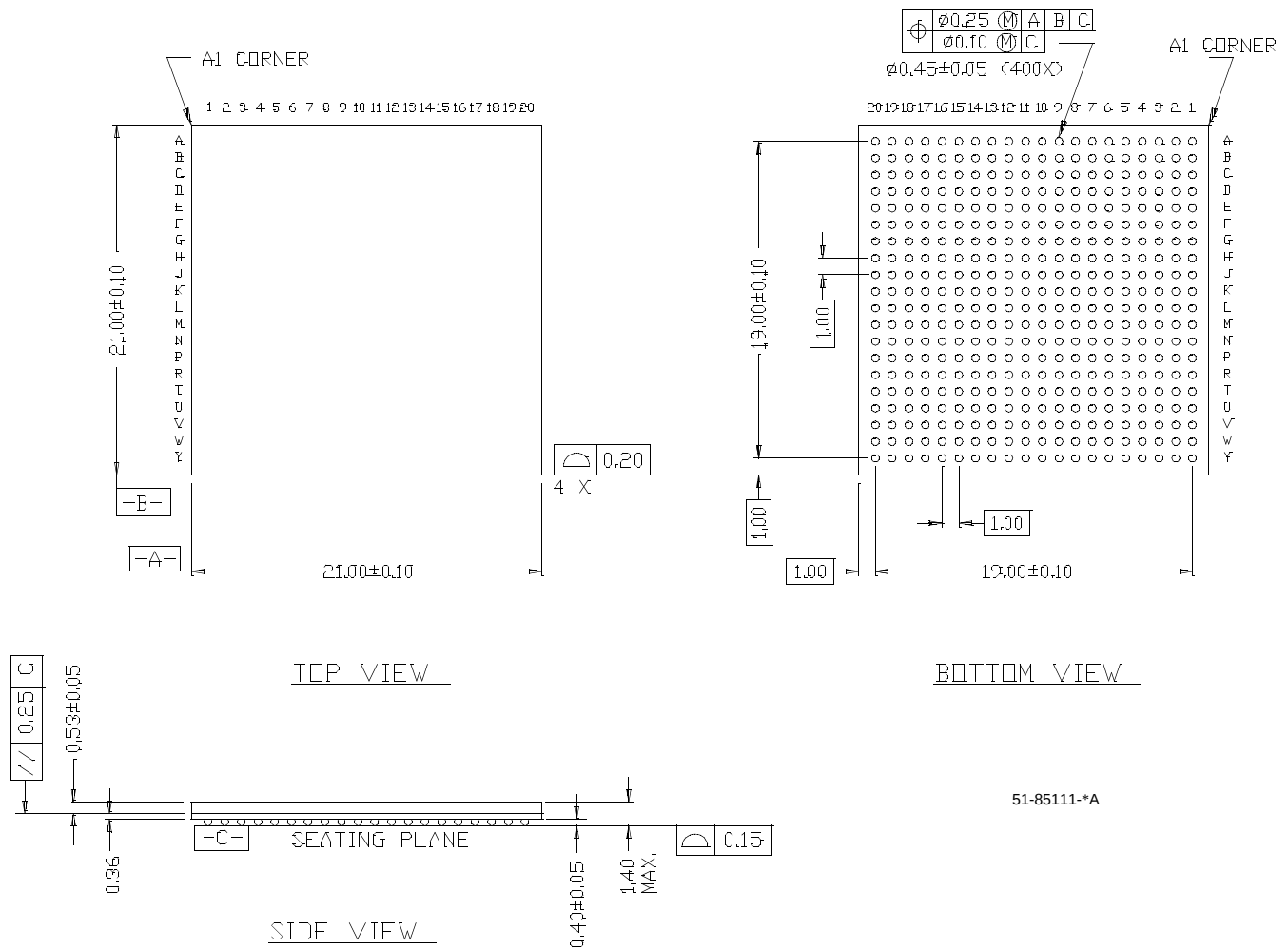
### 388-Lead PBGA (35 x 35 x 2.33 mm) BG388



51-85103-°C

## Package Diagrams (continued)

### 400-Ball FBGA (21 x 21 x 1.4 mm) BB400



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**Addendum****3.3V Operating Range****(CY37064VP100-143AC, CY37064VP100-143BBC, CY37064VP44-143AC, CY37064VP48-143BAC)**

| Range      | Ambient Temperature <sup>[2]</sup> | Junction Temperature | V <sub>CC</sub> |
|------------|------------------------------------|----------------------|-----------------|
| Commercial | 0°C to +70°C                       | 0°C to +90°C         | 3.3V ± 0.16V    |



## Document History Page

| Document Title: Ultra37000 CPLD Family 5V, 3.3V, ISR™ High-Performance CPLDs<br>Document Number: 38-03007 |         |            |                 |                                                                                                                                                                                                                                                                                                           |
|-----------------------------------------------------------------------------------------------------------|---------|------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REV.                                                                                                      | ECN NO. | Issue Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                                     |
| **                                                                                                        | 106272  | 04/18/01   | SZV             | Change from Spec number: 38-00475 to 38-03007                                                                                                                                                                                                                                                             |
| *A                                                                                                        | 124942  | 03/21/03   | OOR             | Updated 3.3V V <sub>CC</sub> requirements for –144 speeds<br>Added an Addendum                                                                                                                                                                                                                            |
| *B                                                                                                        | 126262  | 05/09/03   | TEH             | Changed pinout for CY37128V BB100 package                                                                                                                                                                                                                                                                 |
| *C                                                                                                        | 128125  | 07/16/03   | HOM             | Obsoleted following 3.3V PLCC packaged devices:<br>CY37032VP44-143JC<br>CY37032VP44-100JC<br>CY37032VP44-100JI<br>CY37064VP44-143JC<br>CY37064VP84-143JC<br>CY37064VP44-100JC<br>CY37064VP84-100JC<br>CY37064VP44-100JI<br>CY37064VP84-100JI<br>CY37128VP84-125JC<br>CY37128VP84-83JC<br>CY37128VP84-83JI |